MULTISCALE TRANSIENT THERMAL ANALYSIS OF MICROELECTRONICS

Electronics COOLING

SEPTEMBER 2015
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FEATURE

HEATSINK GEOMETRY TOPOLOGY

An Additive Design Methodology for Identification

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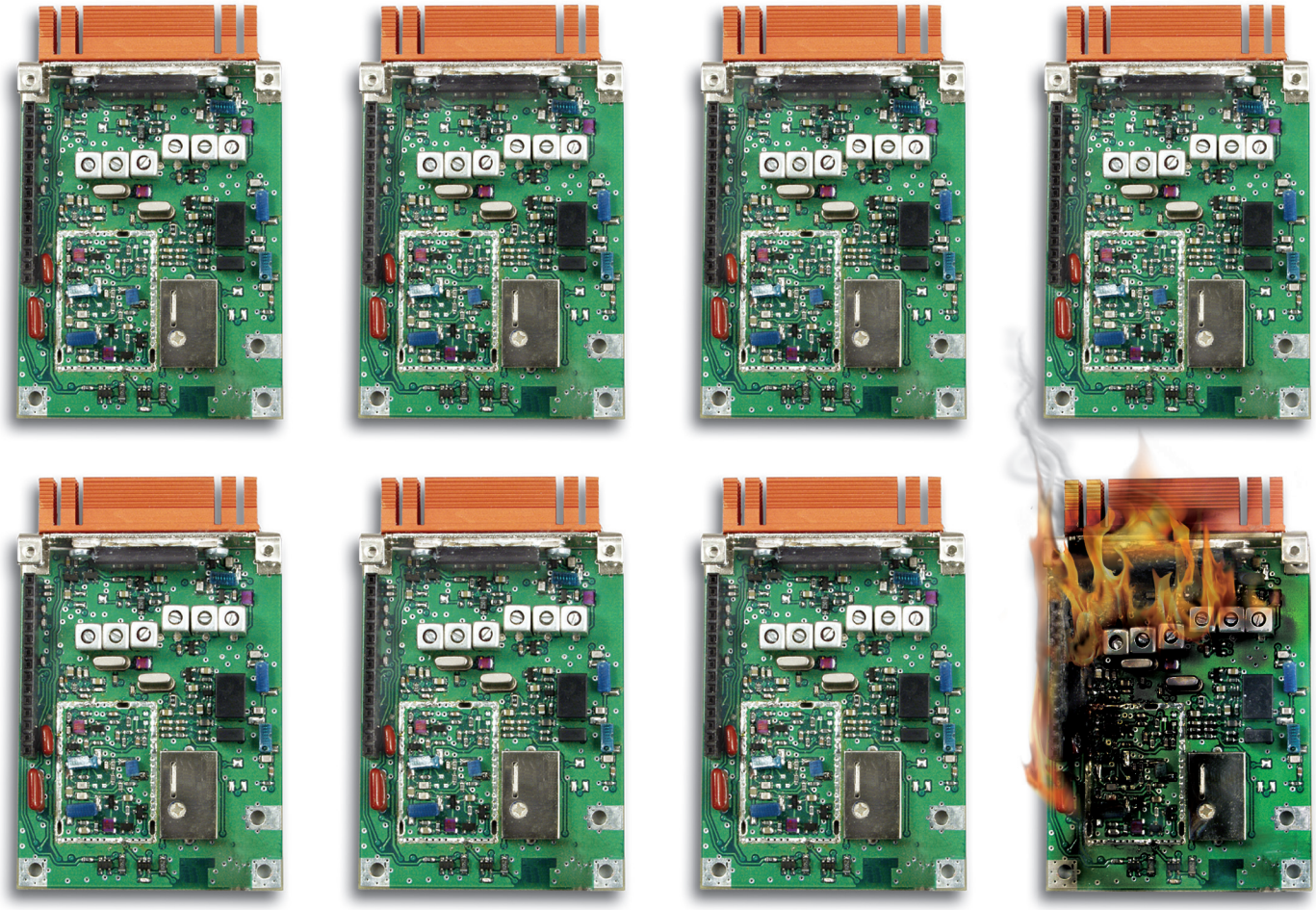

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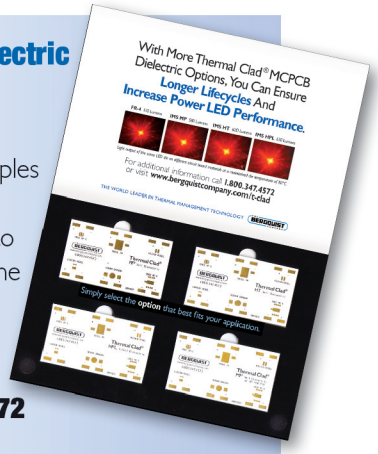

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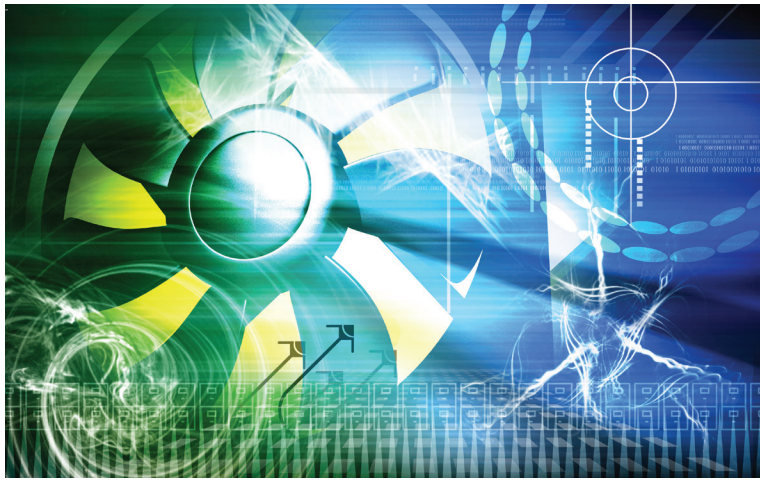

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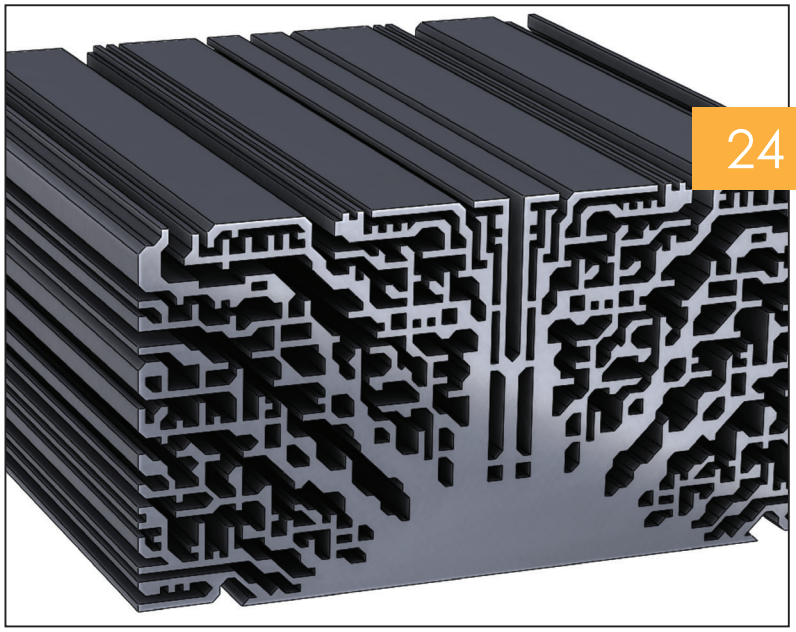

Editorial

Are Graduate Engineers being Effectively Educated for Today's Workplace?

Peter Rodgers, Editor-in-Chief, September 2015

CONTINUING the June Editorial [1] theme, which discussed the societal aspects of enticing today's youth into pursuing a career in the engineering profession, this editorial explores if the capabilities of today's young engineering graduate are being effectively harnessed upon graduation. Otherwise said, is the educational experiences of today's engineering graduates in sync with employer and industry expectations.

As a university professor, my greatest time sink is neither teaching nor research, but undertaking departmental duties for its baccalaureate program accreditation. Using a Shakespearean quote, to convey how I may feel at times about this task, "Though this be madness, yet there is method in't." The time and efforts invested towards accreditation should be ultimately rewarded when a young graduate finds the opportunity to apply his/her acquired knowledge, skills and competences upon employment. To achieve this, a structured and ever-evolving engineering education is required. The effectiveness of engineering education is typically continuously assessed and improved through external accreditation by bodies such as ABET [2], a widely recognized U.S. and international accreditor of engineering university programs. For an ABET-accredited engineering program, eight general criteria (Criterion 1 to 8) that encompass assessment of the student, faculty, program, and institution are required to be met. Criterion 3, student learning outcomes (SLOs), assesses what students are expected to know and be able to do by the time of graduation. The level of achievement of eleven sub-criteria, SLOs 3(a) to 3(k), is monitored to achieve Criterion 3. Accreditation provides confidence to students, employers, and society that the engineering program meets a high quality standard to produce graduates prepared to enter a global workforce.

One of the most effective venues to assess SLOs 3(a) to 3(k) is through a Senior-level "Capstone Design" course. In this course, engineering students work in teams to design, build, and test prototypes having real world applications, incorporating engineering standards and multiple realistic constraints. Typically at the end of this course, students showcase their efforts at a "Senior Design Expo," which in many instances doubles as a job fair.

In the context of the above educational approach, are our young graduates getting the opportunity to fully apply the knowledge, skills, and competences acquired through education in today's engineering workplace? Rather than approaching this concern as a rhetorical question, let's explore a concerning answer.

Firstly, rather than the majority of graduates being feted, a recent U.S. employer survey [3] judge them to be ill-prepared for today's workplace. Only 25% of employers felt that recent graduates are well prepared in critical thinking and analytic reasoning, written and oral communication, complex problem solving, innovation and creativity, and applying knowledge and skills to real world settings. On the other hand, students were found to feel far more prepared (i.e., above 60%) in these key areas. Based on the same survey, employers strongly endorsed broad and project-based learning as the best preparation for career opportunity and long-term success. How can the above disconnect between the employer's and graduate's perception of his/her capabilities be addressed? Is the Capstone Design experience, which develops and assesses the level of achievement of most key educational criteria, inadequately conceived or utilized?

For the electronics thermal management community, employers should realize that opportunities exist to contribute to undergraduate education through involvement in Capstone Design activities. In the long term, this could assist to better sync young graduates' and employers' expectations.

Electronics Cooling recognizes that continued education is extremely important. This year, we announce a unique opportunity to learn for all engineers in the thermal management field - *Thermal Live.* This is a brand new, free online event that will take place Oct. 6-8, 2015, and will offer webinars and roundtables on thermal management topics. Please join us for this special event. Visit www.thermallive2015.com for more information.

References

[1] Guenin, B., 2015, "Editorial: The Joy of Engineering," *ElectronicsCooling*, June, pp. 1.
[2] ABET, http://www.abet.org/, last retrieved August 26, 2015.

Electronics COOLING

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PUBLISHED BY
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THERMAL LIVE 2015

October 6-8, 2015 - www.thermallive2015.com

Thermal Live™ is a brand new concept in education and networking in thermal management - a FREE 3-day online event for electronics and mechanical engineers to learn the latest in thermal management techniques and topics. Produced by Electronics Cooling® magazine, and launching in October 2015 for the first time, Thermal Live™ features live webinars, roundtables, whitepapers, and videos ... and there is no cost to attend!

TECHNICAL PROGRAM

DAY 1 - TUESDAY . OCTOBER 6

KEYNOTE SPEAKER

Oct. 7, 11:00 a.m. – 11:45 a.m. (EDT)

WEBINAR

celsia™ Making Hot Technology Cooler

A Practical Guide to Using Two-Phase Heat Sinks

Oct. 6, 12:15 p.m. – 1:00 p.m. (EDT)

OVERVIEW

Overview: Two-phase devices are incredible heat conductors and significantly boost heat sink performance. We'll present a practical guide to using both heat pipes and vapor chambers: similarities, differences, operating parameters, mounting options, common mistakes, best uses, examples, and performance modeling.

SPEAKER

George Meyer is a thermal industry veteran with over three decades experience in electronics thermal management. He currently serves as CEO/CTO of Celsia Technologies. Mr. Meyer has been instrumental in establishing Asian operations, developing new technologies, key customer relationships, managing the product portfolio, and growing sales into the computer, telecommunications, networking, LED lighting, medical, laser and military markets. He holds over 70 patents in heat sinks and heat pipe technologies.

DAY 1 CONTINUED

ROUNDTABLE

BERGQUIST Henkel

Liquid Dispensed Thermal Interface Materials (TIMs)

Oct. 6, 1:30 p.m. – 2:15 p.m. (EDT)

OVERVIEW

This roundtable will discuss how effective thermal management is key to ensuring consistent long-term performance and reliability in electronic devices. With an increasing variety of electronic applications demanding smaller packaging, higher power, and lower cost, the need for innovative high performance, low cost thermal solutions continues to grow.

While there are many pad-form solutions available on the market, ever-increasing customer costs inherent with designing, documenting, shipping, storing, managing and assembling a multitude of die-cut parts in varying sizes continues to challenge design engineers. Join a panel of thermal management experts during this roundtable, where they will discuss how high performance liquids with unique characteristics are designed to improve overall thermal performance and reliability for thermal engineers.

Moderator:
Mark Amberg Market Manager -

Mark Amberg has been with The Bergquist Company, now a division of Henkel AE, for 18 years. He has held the roles of Automotive Market Manager and Automotive Business Development Manager for the last ten years.

Liquid Dispensed TIMs Roundtable information continued on next page

DAY 1 CONTINUED

Liquid Dispensed TIMs Roundtable information continued from previous page

Panelists:

Lonnie Helgeson

Lonnie Helgeson Product Line Manager - Lonnie Helgeson is the Product Line Manager overseeing the Gap Filler product line for Henkel. His responsibilities include the identification and prioritization of strategic business opportunities to enhance the Liquid Thermal Interface Materials (TIMs) portfolio. With over thirty years of experience in the high tech market, he offers great insight in this fast paced globally competitive marketplace.

Ryan Verhulst

Ryan Verhulst Scientist Engineer - Ryan Verhulst is a Research & Development engineer working on thermal interface materials. He has been with Henkel (formerly Bergquist) for 8 years. His education is in material science and he has experience working with ceramic powders, adhesives and sealants, and a wide variety of polymer chemistries.

John Timmerman

John Timmerman Senior Scientist Engineer - John is a senior research engineer with Henkel, whose main focus is high performance thermal interface materials, thermally conductive adhesives, and EMI absorbing materials. He has been with Henkel for 8 years and graduated from the University of Washington in 2003 with a Ph.D. in chemical engineering, where he researched thermal cycling of composite materials.

Tom Harris

Tom Harris Field Applications Engineer - Tom Harris uses his Process Engineering, Automation and Customer Service Experience to assist Henkel AEH customers implement and troubleshoot Automated Liquid TIM Dispensing in their manufacturing processes. He also directs Henkel's Dispense Alliance Program, and Automated Dispensing Technical Knowledge-base. He holds a Six Sigma Green Belt as well as an M.B.A. and B.S. in Engineering.

WEBINAR

Honeywell

Thermal Management Challenges, Requirements and Solutions for the Electronics Industry

Oct. 6, 2:45 p.m. – 3:30 p.m. (EDT)

OVERVIEW

This webinar will discuss the key thermal properties involved in TIM decision-making, the challenging thermal requirements of key applications, a comparison of solutions available to the marketplace, and the promise of next-generation PCMs designed to meet the constantly changing demands of the electronics industry.

SPEAKER

Glenn M. Mitchell, Ph.D is the Director of Technology for Honeywell Electronic Materials. He has a Ph.D. in Analytical Chemistry from Drexel University,. His focus is new molecule and process development and optimization for the electronics, semiconductor, and solar industries. His areas of expertise is ultra-trace impurity analysis and analytical method development, advanced statistical analysis and chemometrics, etch, deposition, and more.

DAY 2 - WEDNESDAY . OCTOBER 7

WEBINAR

AAVID THERMALLOY

Small Form Factor Cooling with Jet Air Mover Technology

Oct. 7, 12:15 p.m. – 1:00 p.m. (EDT)

OVERVIEW

Jet Cooling Technology has far reaching implications on small form factor design. These novel air movers increase the design space, flexibility and performance of a wide range of products, from consumer handhelds to LEDs to outdoor telecom.

SPEAKER

Lee Jones joined Aavid-Thermalloy in the summer of 2014. As part of the team at Nuventix, Lee led technical and product development efforts to create the world's most compact and reliable turbulent air coolers. His role was an inside-outside one spanning SynJet engineering and customer product and advanced development teams to tailor SynJet solutions that would enable breakthrough products for customers. At Aavid he performs a similar role leading the product management efforts of SynJet development globally. Lee has a Bachelor's Degree in Mechanical Engineering from Rochester Institute of Technology, and a Master's Degree in Mechanical Engineering from The University of Texas at Austin.

ROUNDTABLE

phononic

Extending Moore's Law through Innovative Active Cooling

Oct. 7, 1:30 p.m. – 2:15 p.m. (EDT)

OVERVIEW

This roundtable will be a discussion with thermal engineers, hardware designers, and architects on the merits of passive fan assists, water cooling, and variable assist active cooling as it pertains to high density electronics. Specifically, the discussion will focus on the pros and cons of different approaches to electronics cooling and the impact on system performance from component temperature control, form factors, power consumption and cost trade-offs. Attendees will gain an understanding of the most recent advances in electronics cooling, including the ability to use active heat pumps based on thermoelectric devices, to provide superior cooling performance while minimizing the aggregate capex and opex costs.

SPEAKER

Chris Caylor is the Technical Director of the Electronics Cooling Business Unit at Phononic. He earned his Ph.D. in Chemistry from the University of California at Berkeley. He is an engineering, research and product leader with over 10+ years in managing engineering programs and teams. Chris also has 6+ years experience in winning and managing government programs from diverse sources such as DoD, DoE and DARPA.

DAY 2 CONTINUED

WEBINAR

wakefield-vette

RichardsonRFPD
An Arrow Company

Liquid Cooling – Practical Guidelines to Design & Manufacture

Oct. 7, 2:45 p.m. – 3:30 p.m. (EDT)

OVERVIEW

Industry trends continue to produce smaller footprints with higher power densities. In some cases, Liquid Cooling is the answer for cooling your application. This discussion will go over the basic design and structure of several standard and custom liquid cooling solutions while highlighting the manufacturing process most appropriate for your application.

SPEAKER

Mark Pelillo is the Director of Engineering at Wakefield-Vette. Mark has been in the electronics cooling design industry for over 25 years and has been a pivotal part in introducing new technologies to the marketplace. Mark earned his engineering degree at Clarkson University. Mark has been with Wakefield-Vette since 2005, where he leads the engineering team. This team supports existing customer challenges, while researching and introducing new technologies to market. Mark's vast experience not only with design but in manufacturing, allows Wakefield-Vette's customers to improve their thermal performance while simplifying the manufacturing steps to meet specifications.

WEBINAR

DOW CORNING

IMAGINE: Drawing Out Heat, Leaving in Performance and Reliability

Oct. 7, 4:00 p.m. – 4:45 p.m. (EDT)

OVERVIEW

In this webinar, attendees will be able to see key milestones in the evolution of thermal interface materials that help ensure today's electronics performance and reliability. They will also be able to learn about proven, effective thermal management solutions for basic devices to complex electronics architectures and get expert insights on best practices and material types to meet specific design objectives. Attendees will discover how advanced thermal management solutions make game-changing differences in a diverse range of industries and will see brief case studies of electronics applications with thermal management excellence.

DAY 3 - THURSDAY . OCTOBER 8

WEBINAR

GRAFTech International

High Temperature TIM for Power Modules that Eliminates Pump-out and Dry-out Failures

Oct. 8, 11:00 a.m. – 11:45 a.m. (EDT)

OVERVIEW

In this webinar, attendees will learn about developed compressible graphite foils to provide a high reliability, high temperature (over 200°C) TIM that addresses the thermal demands and out-of-flatness issues of large high power switching modules. This new material will eliminate the compromise between thermal performance, maximum operating temperature, reliability, cost, and ease of installation. Unlike any other graphite or soft metal TIMs that provide compression of less than 10%, HITHERM™ HT-C3200 compressible graphite pads have a nominal starting thickness of 200 microns and compress down to 50 microns at 100 PSI (~700 kPa) reducing the total thermal resistance between the two surfaces while eliminating pump-out and dry out failures common with greases and phase change materials.

SPEAKER

Prashanth Subramanian - As the manager of the New Product Development group at Graftech International, a world leader in graphite material science, Prashanth is responsible for the development and commercialization of solutions to the consumerelectronics and Thermal Interface for high powered device markets. Prashanth worked at SUMCO USA in the Development Engineering group providing solutions to the high-voltage device market. Prashanth holds a degree in Electronics Engineering from Shivaji University (India) and a M.B.A. from The Ohio State University.

WEBINAR

Mentor Graphics

PCB Design Strategies in Handheld Devices

Oct. 8, 12:15 p.m. – 1:00 p.m. (EDT)

OVERVIEW

This presentation reviews factors influencing thermal design in consumer handheld devices from touch temperature const raints, dissipating heat effectively from high power density components, tight tolerance geometry, through to varying power modes from user operation. Thermal management studies ideally allow accurate, rapid, physical modeling to make decisions on materials, components and layout beside power control feedback to achieve performance & target lifetime with reduced testing requirements. Simulation methods are discussed and closer integration with both electronic and industrial design functions as part of overall product development.

PCB Design Strategies Webinar information continued on next page

DAY 3 CONTINUED

PCB Design Strategies Webinar information continued from previous page

SPEAKER

John Wilson joined Mentor Graphics Corporation, Mechanical Analysis Division (formerly Flomerics Ltd) after receiving his BS and MS in Mechanical Engineering from the University of Colorado at Denver. Since joining in 1999, John has worked on or managed more than 70 thermal and airflow design projects. His modeling and design knowledge range from component level to Data Centers, heat sink optimization and compact model development. John has extensive experience in IC package level test and analysis correlation through his work at Mentor Graphics' Fremont based Thermal Test Facility. Currently John serves as an Electronics Product Specialist..

Mentor Graphics is a company that enables companies to develop better electronic products faster and more cost-effectively. Their innovative products and solutions help engineers conquer design challenges in the increasingly complex worlds of board and chip design.

DAY 3 CONTINUED

WEBINAR

MATERION

Composite Metal Heat Spreaders in Handheld Electronics Design

Oct. 8, 1:30 p.m. – 2:15 p.m. (EDT)

OVERVIEW

This webinar will discuss how omposite metal solutions provide design opportunities for improved heat spreading and mechanical rigidity in space-constrained consumer devices. Utilizing composites in the design of structural components allows existing device features, such as frames and EMI shields, to dissipate thermal loads from high power heat sources without the need for secondary heat spreaders. Design considerations and materials performance properties are discussed with an eye toward cooler, stiffer devices.

SPEAKER

Aaron Vodnick joined Materion in 2012. He eads global market and product development initiatives for composite metal systems, specifically unconventional thermal and structural materials for consumer devices. Aaron has a Bachelor's Degree in Materials Engineering from the University of Minnesota Twin Cities, and a Ph.D. in Materials Engineering from Cornell University.

www.thermallive2015.com

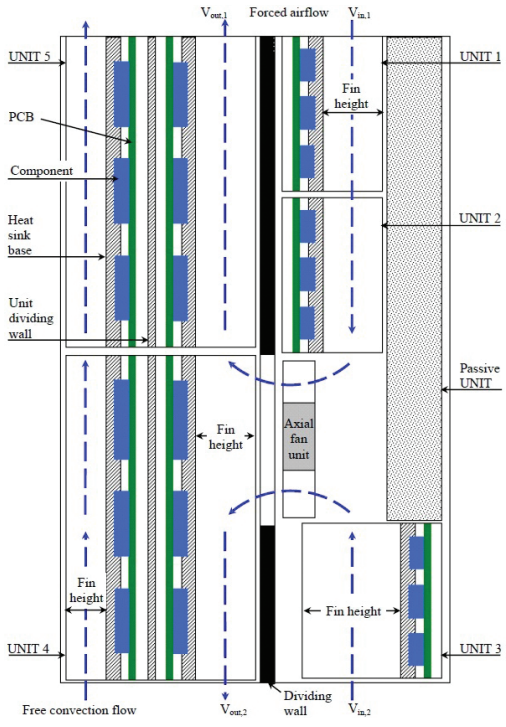
Numerical Modeling without Supporting Experimentation

Peter Rodgers
Editor

FAN MODELLING is one of the most critical aspects of the analysis of forced-air-cooled systems. Lasance [1] summarized the challenges of modeling air movers such as fans and key factors that need to be taken into consideration. Such factors include the need to model the fan hub, and to account for the swirl velocity coefficient.

In addition to the above challenges, Grimes et al. [2] found that vendor fan performance characteristic curves published in manufacturer catalogs can typically be only approximately reproduced by clients under standard conditions, although vendor data is supposed to be generated in accordance with BS Standard 848. This standard specifies an acceptable uncertainty of ± 2 % for all measurements of fan flow.

Furthermore, the potential adverse influence of the operating environment on fan curve performance is often overlooked in numerical work, and is the focus of this article. Constricted installation spaces in electronic systems can result in significant fan performance losses [3-5], as illustrated in for example [3]. To demonstrate the potential significance of this oversight, the results of a computational fluid dynamics (CFD) benchmark undertaken for a mock-



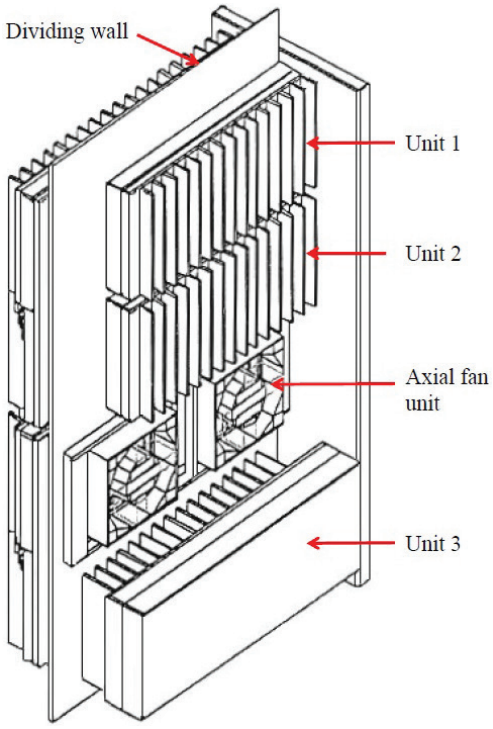


Figure 1: System geometry and internal airflow patterns.

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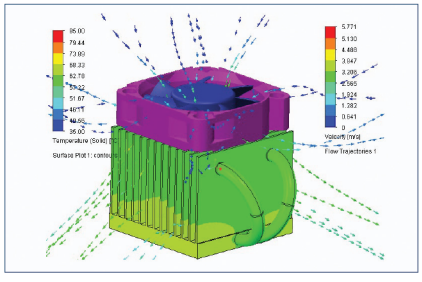

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System cooling configuration	Fan location and operational mode	Airflow configuration
A	• Axial fan unit mounted within the enclosure, but unpowered	All heat sinks are passively cooled, with air entering the enclosure through Units 3 and 4 heat sinks, and vertically exhausting through Units 1 and 5 heat sinks.
B	• Axial fan unit mounted 50 mm beneath the enclosure (Units 3 and 4) • Fan operated in blowing mode	Forced air enters through Unit 3 heat sink and Unit 4 right-hand side heat sink, and exhausts directly through Unit 1 heat sink and Unit 5 right-hand side heat sink. Unit 4 and Unit 5 left-hand side heat sinks are passively cooled.
C	• Axial fan unit mounted within the enclosure, and powered • Fan operated in sucking mode	Units 1, 2 and 3 heat sinks, and Units 4 and 5 right-hand side heat sinks, are cooled by forced convection. Units 4 and 5 left-hand side heat sinks are passively cooled. In forced convection cooling, air is drawn into the enclosure through Units 1 (Vin_1) and 3 (Vin_2) heat sinks, and exhausts through Units 4 (Vout_2) and 5 (Vout_1) heat sinks.

*Note: The geometry of cooling configurations A, B and C is shown in Figure 1.

Table 1 : System cooling configurations.

up telecommunication system to assess the accuracy of fan curve modeling is presented.

As shown in *Figure 1*, the system is comprised of five mock-up heat dissipation units (designated as Units 1 to 5), each having a printed circuit board (PCB) assembly mounted to a heat sink. PCB heat dissipation was experimentally simulated using board-mounted resistors. Units 1, 2, and 3 are comprised of a single PCB-heat sink assembly, whereas Units 4 and 5 both have two PCBs separately mounted to heat sinks.

Three system cooling configurations are considered, that are summarized in Table 1. Note that cooling configuration C could be considered as a poor thermal design in terms of fan location, but serves here to illustrate modeling challenges.

For cooling configuration C, the influence of the restricted environment on fan performance requires to be considered. In the absence of a physical prototype, the fan performance curve was obtained from the vendor and was generated in accordance with BS Standard 848. In addition, the influence of a single 200 mm x 200 mm flat plate obstruction mounted at varying distances from the fan, ranging from 10 mm to far field, on either the pressure or suction side, as illustrated in *Figure 2*, is assessed. As expected [3], the suction side is found to be more sensitive to the presence of an obstruction than the pressure side.

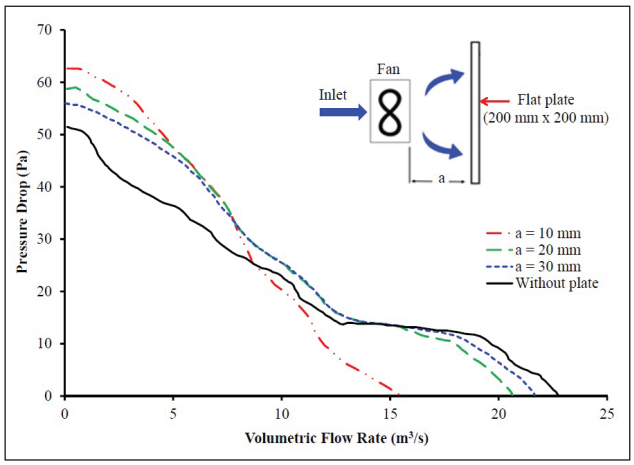
The airflows entering and exiting the system enclosure were measured using hot wire anemometry to determine fan flow rate. Operating temperature was measured in steady state conditions at selected locations, and the electrical power dissipated as heat by each unit was also measured. These latter two measurements combined permitted the calculation of the unit thermal resistance.

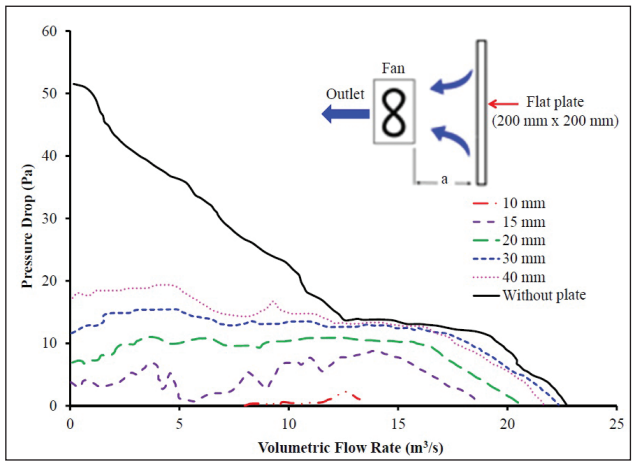
A complete system level CFD model was constructed using an industry standard software for each of the three enclosure cooling configurations in Table 1, and was validated for individual units using experimental measurements conducted in wind tunnel and still air enclosures. For each of the three enclosure cooling configurations, the model predictive accuracy is assessed in terms of the measured heat sink thermal resistance and fan flow rate.

As shown by the results presented in Table 2, very good agreement was found between numerical predictions and measurements for cooling configurations A and B. However significant discrepancies in heat sink thermal resistance exist for configuration C, which is attributed to inaccurate prediction of the fan airflow rate.

SUMMARY

This article illustrates that without supporting measurements, predicting complex system thermal performance is a challenge because of the non-availability of accurate fan flow modeling data, applicable to the system geometry and cooling configuration under analysis. The accuracy of the CFD software itself is unlikely to be a significant source of error in this instance.





Note: a = separation distance between fan and flat plate obstruction.

Figure 2: Measured change in axial fan performance characteristic curve caused by the flat plate obstruction.

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System cooling configuration	Finding
A	Predicted heat sink thermal resistances are within 10% of measurement.
B	Predicted fan flow rate and heat sink thermal resistance are both within 10% of measurement
C	• 55% discrepancy between predicted fan airflow using nominal vendor fan curve and measurement exists • 40% discrepancy between predicted fan airflow using suction side fan curve and measurement for a = 30 mm exists • Approximately 20% to 30% discrepancy between predicted heat sink thermal resistance and measurement exists

Table 2: Discrepancy in unit thermal resistance between numerical predictions and measurements.

Effective Heat Spreading Angle

Dirk Schweitzer
Infineon Technologies

INTRODUCTION

TO ACCURATELY COMPUTE THE THERMAL RESISTANCE of a layered structure, such as the Junction-to-Case thermal resistance of a power semiconductor, the heat spreading inside the structure has to be considered. The calculation of the spreading resistance is not a trivial problem [1] and analytical solutions exist only for extremely simple geometries. Using Finite Element Analysis (FEA) the heat spreading and resulting temperature distribution can be accurately computed. But for a quick and simple analysis of the spreading resistance the thermal engineer has to resort to rules of thumb such as the 45° spreading angle [2, 3], or to approximation formulas which can be found in literature [1, 4]. This article presents an alternative approach, namely the concept of the effective heat spreading angle [5].

EFFECTIVE HEAT SPREADING PROFILE

To explain this concept we consider a silicon chip on a copper (Cu) leadframe as shown in figure 1. A power of P_H = 10 W is dissipated homogeneously on an active area of 1.0×1.0 mm² on the 3.0×3.0 mm² chip whereas the bottom temperature of the leadframe is kept constant (ideal cooling).

Monitoring the local heat flux density $p(x)$ from the center of the die surface to the center of the bottom surface (x being the distance from the heat source), *Figure 2*, we notice that the heat flux density drops continuously from initially 10 W/mm² to about 1 W/mm² at the bottom. Obviously the heat spreading is the reason for the decreasing heat flux density. If the cross sectional area of the heat flow path was constant the heat flux density would also remain constant throughout the structure. Since the variation of the heat flux density is closely related to the amount of heat spreading the obvious idea was to derive a measure for the spreading angle from the derivative dp/dx of the heat flux density.

For simplification we shall assume that the heat flux is homogenously distributed over each cross section $A(x)$ of the heat flow path (which is not the case in reality). At each position x the product of cross-sectional area $A(x)$ and heat flux density $p(x)$ equals the total power dissipation P_H.

$$A(x)p(x) \tag{1}$$

Furthermore we shall assume that the shape of the heat flow cross section does not change as the heat propagates (which is not true either); i.e.: in this case it remains a square area independent of the distance x from the chip surface. For the half side length $y(x)$ of this square we obtain:

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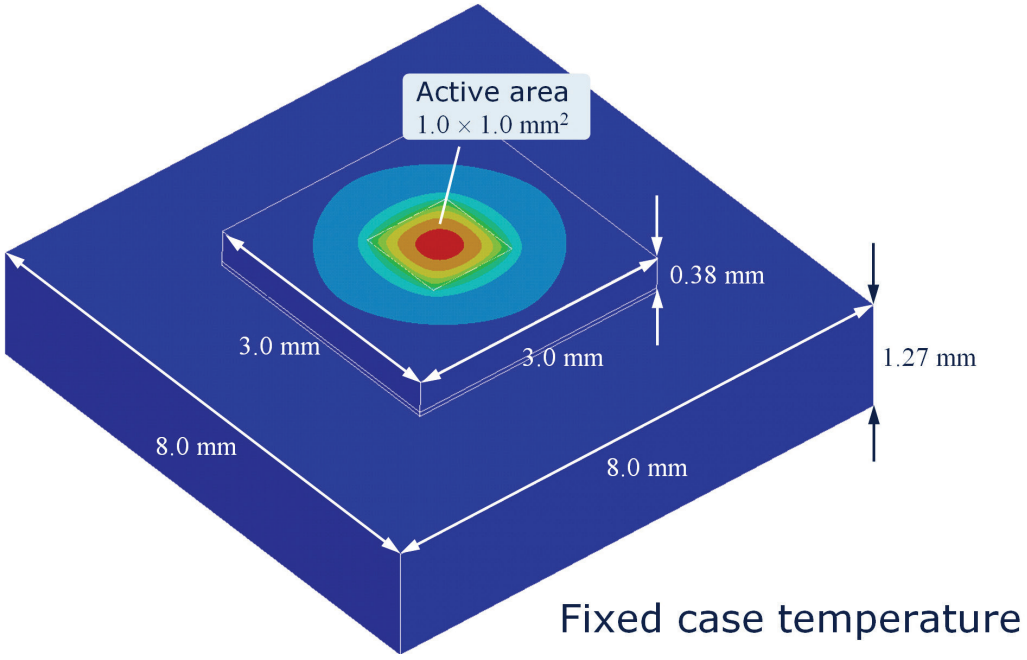

Figure 1: Silicon chip on Cu leadframe (solder die attach).

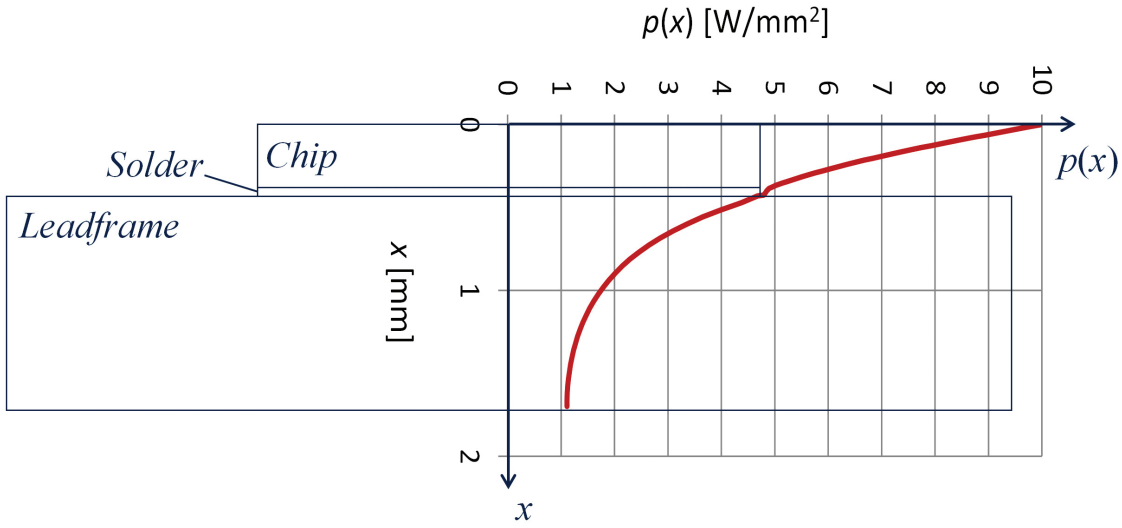

Figure 2: Heat flux density along heat flow path.

$$y(x) = \frac{1}{2}\sqrt{A(x)} = \frac{1}{2}\sqrt{\frac{P_H}{p(x)}} \qquad (2)$$

Plotting *y(x)* vs. distance *x* we obtain the *effective heat spreading profile (figure 3).* We call this the *effective* heat spreading profile as opposed to the real spreading profile because it has been derived for above non-true assumptions. This approach is justified by the fact that we can use the effective heat spreading profile to calculate the spreading resistance within any desired accuracy. *Figure 4* shows a discretization of the effective spreading cone. In this example chip and leadframe are each subdivided into 4 slices and the die attach is represented by one more slice. The temperature drop ΔT_i across each slice can be calculated from the density *pi* of the heat flux passing through it, its thickness d_i, and its thermal conductivity λ_i:

$$\Delta T_i = \frac{p_i}{\lambda_i} d_i \qquad (3)$$

Because the cross sectional area A_i of each slice has been

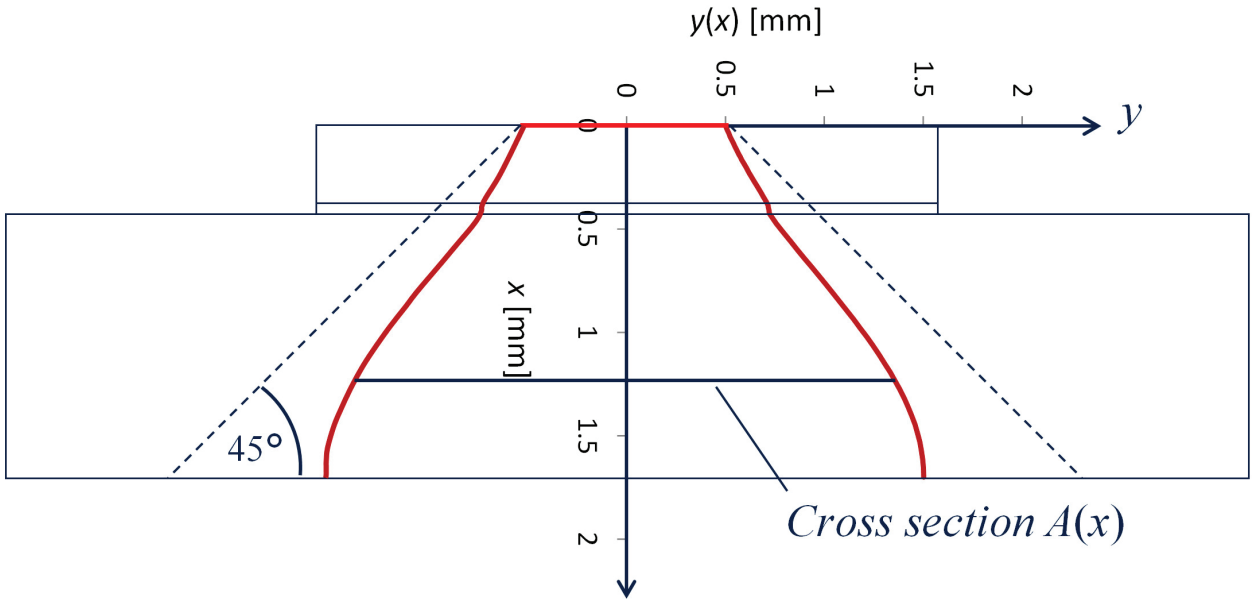

Figure 3: : Effective heat spreading profile.

constructed such that $A_i = P_H/p_i$ we have:

$$\Delta T_i = \frac{P_H}{A_i \lambda_i} d_i = P_H \theta_i \quad \text{with} \quad \theta_i = \frac{d_i}{A_i \lambda_i} \tag{4}$$

where θ_i represents the thermal resistance of the *i-th* slice such that if we multiply it by the total heat flux P_H we obtain the correct temperature difference across that slice. Therefore the sum over all slices:

$$\theta = \sum_{i=1}^{n} \theta_i = \sum_{i=1}^{n} \frac{d_i}{A_i \lambda_i} \tag{5}$$

approximates (and for $n \to \infty$ exactly returns) the thermal resistance of the structure. In practice even a rather coarse discretization of the effective heat spreading profile as in figure 4 results in a quite good approximation of the actual thermal resistance (<1% error in this case). Application of the popular 45° heat spreading assumption on the other hand would overestimate the size of the spreading cone and thus result in a too low value for the thermal resistance *(figure 3)*.

EFFECTIVE HEAT SPREADING ANGLE

Based on the effective heat spreading profile y(x) the corresponding effective spreading angle can be easily computed *(figure 5)*:

$$\tan \phi_{eff} = \frac{dy}{dx} \tag{6}$$

Using Equation (2) we obtain for the heat spreading cone with square cross section:

$$\tan \phi_{eff} = -\frac{1}{4} \sqrt{\frac{P_H}{p(x)}} \frac{1}{p(x)} \frac{dp}{dx} \tag{7}$$

BENEFITS OF THE EFFECTIVE HEAT SPREADING CONCEPT

The attentive reader will now object: That is all well and good but how do I know the heat flux density p(*x*) along the heat flow path which is required to calculate the effective spreading profile? Which is a valid objection since p(*x*) can only be obtained by Finite Element (FE) simulation. There would be little motivation to perform a FE simulation to calculate the heat flux density since we could as well use the FE simulation to directly compute the temperature difference and thermal resistance between junction and case.

In the author's view the effective heat spreading concept serves two purposes. On the one hand it provides a clear definition of heat spreading cone and spreading angle which so far is often based on a somewhat vague idea of how the heat is spread inside a structure. Heat spreading cone and angle can be visualized which helps us to gain insight into spreading mechanism and influencing factors. Looking at figure 3 we see *e.g.* that the popular assumption of a 45° spreading angle is overly optimistic in that case. This is the educational aspect.

On the other hand the effective heat spreading concept also serves a practical purpose. As shown in [5] we can often find generally applicable rules for the effective spreading angle which are valid not only for one particular case/device but provide a

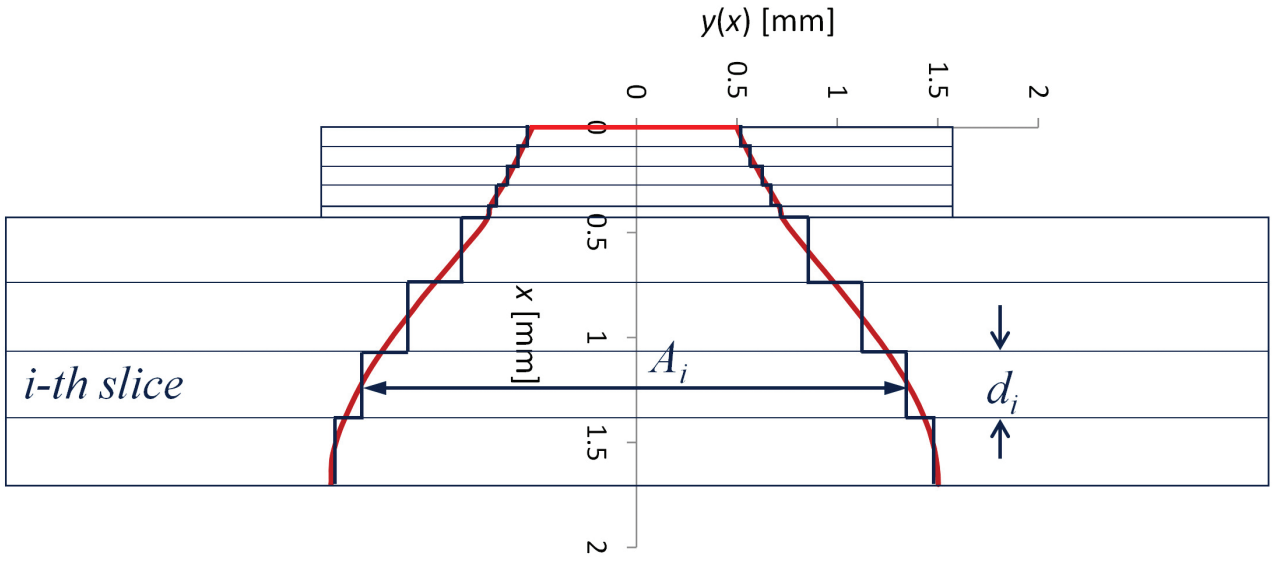

Figure 4: Discretization of the effective heat spreading cone.

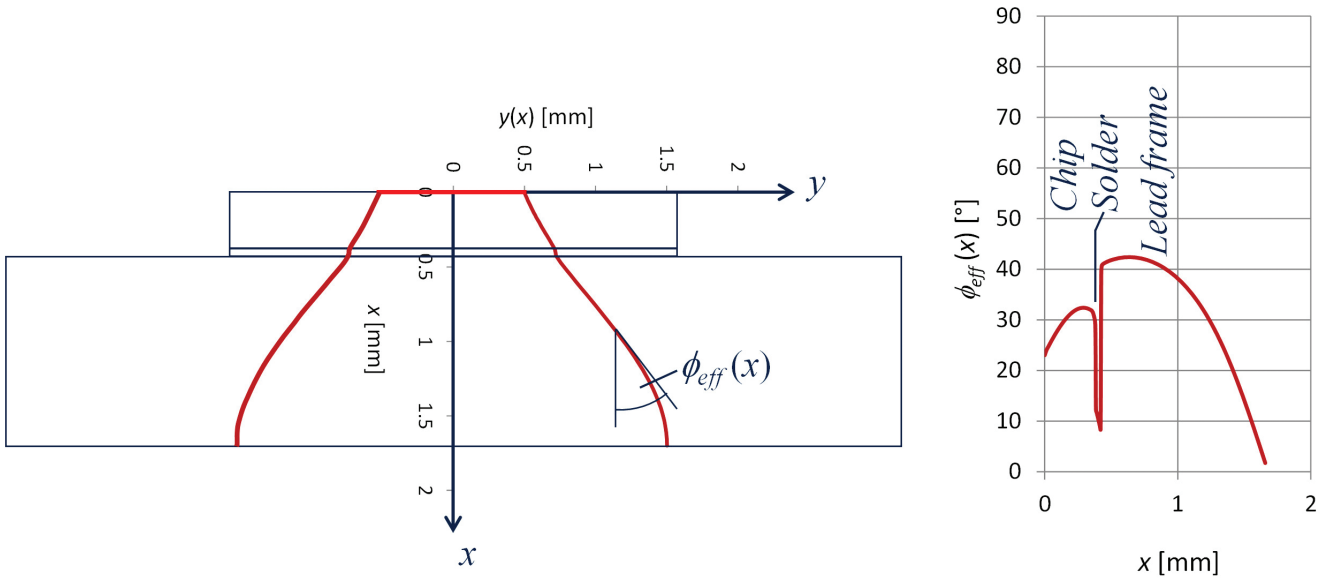

Figure 5: Effective heat spreading angle.

good approximation for a whole sub-class of cases (*e.g.* all power semiconductors with solder die attach). Based on these rules and *Equation (5)* we can implement more accurate spreadsheet calculators for the thermal resistance of this sub-class of devices.

FINAL REMARK

We could also try to define the spreading cone by a surface that intersects all isothermals at 90° angle thus ensuring zero heat flux across that border. But contrary to the approach presented above the resulting heat spreading cone would be useless when it comes to computing the associated thermal resistance since the heat flow density over parallel cross sections of the spreading cone is not constant.

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On-site Cogeneration for Reducing Data Center Primary Energy Use

By Dustin W. Demetriou
IBM

INTRODUCTION

AS MOST READERS ARE AWARE, the data center industry has put an increased focus on energy efficiency and environmental impact. Data centers in the United States are estimated to consume nearly 2% of the total electricity. The *de facto* metric used in the data center industry to evaluate energy efficiency has been the Power Usage Effectiveness (PUE), as defined by The Green Grid [1]. As defined by *Equation (1)*, PUE is the ratio of the total power that enters the data center facility (including cooling, power distribution losses, lights, HVAC, IT Equipment, etc.) to the power provided to the IT equipment.

$$PUE = \frac{Total\ Facility\ Power}{IT\ Equipment\ Power} \quad (1)$$

Recent surveys [2, 3] have shown that the average data center PUE is still greater than 1.7. This means that for every 1.0 watt of IT Equipment power, another 0.7 watts are needed to deliver power and cooling. An example breakdown of the power use in a data center is shown in Figure 1. This example data center has a PUE of 1.71.

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The PUE only accounts for the power distributed throughout the data center. In almost all cases, this electricity is generated and delivered to the data center from a remote power plant. The actual primary energy required (Q_{PE}) to operate the data center is given by:

$$\dot{Q}_{PE} = \frac{P_{IT} \times PUE}{\eta_{th} \times \eta_{dist}} \quad (2)$$

The efficiency in the denominator of *Equation (2)* is the combination of the power plant's thermal efficiency (η_{th}) and the efficiency of transmitting and distributing the power (η_{dist}) from the site of generation to the data center. The US Department of Energy and Energy Information Administration have reported that these distribution losses are typically about 7% [4].

USING ON-SITE POWER GENERATION FOR DATA CENTERS

An on-site power generation system for a data center, as shown in *Figure 2*, provides a number of advantages compared to a grid-powered data center. For example, an on-site power generation system allows the use of the generator's waste energy to provide cooling using a thermally-activated absorption chiller [5], otherwise known as a cogeneration system. Unlike many commercial buildings, a data center can provide a

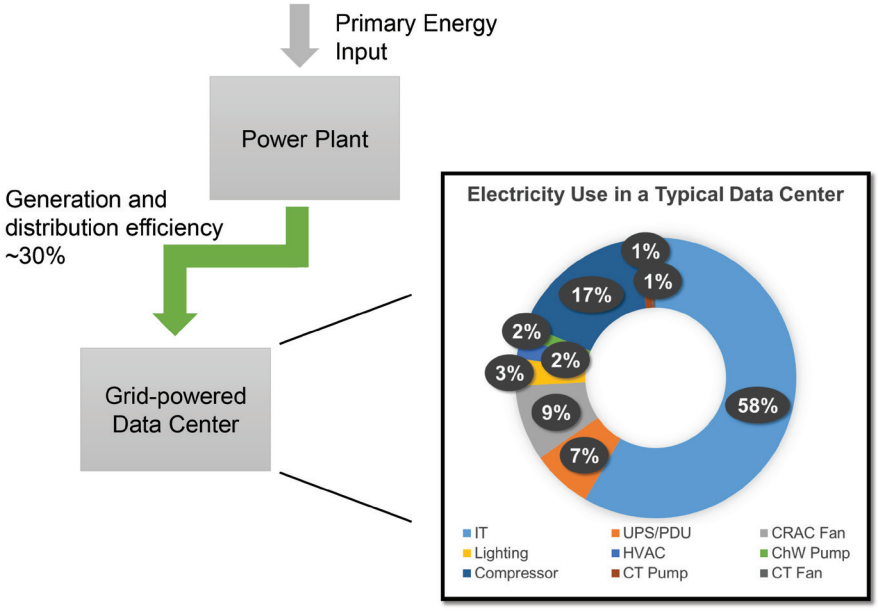

Figure 1: Energy Flow for a Conventional Grid-Powered Data Center.

high utilization of the cogeneration system's thermal output because its electrical and thermal demands are strongly correlated. Every watt of electrical power provided to the data center must be thermally removed. The use of an absorption chiller to provide cooling removes a substantial electricity demand due to the elimination of mechanical cooling.

To determine a PUE for a cogeneration system based data center, we can remove both the HVAC (heating, ventilating, and air conditioning) and compressor loads – as these are provided by the absorption chiller using the data center's waste heat, with substantial reduction in electricity consumption. Additionally, the cooling tower pump and fan power requirements must scale accordingly since the absorption chiller coefficient of performance (COP) is much lower than a conventional vapor compression chiller. The condenser load on the chiller (Q_{CND}) can be computed as:

$$\dot{Q}_{CND} = \dot{Q}_{EVAP}\left(1 + \frac{1}{COP}\right) \quad (3)$$

where, Q_{EVAP} is the evaporator load, which includes the

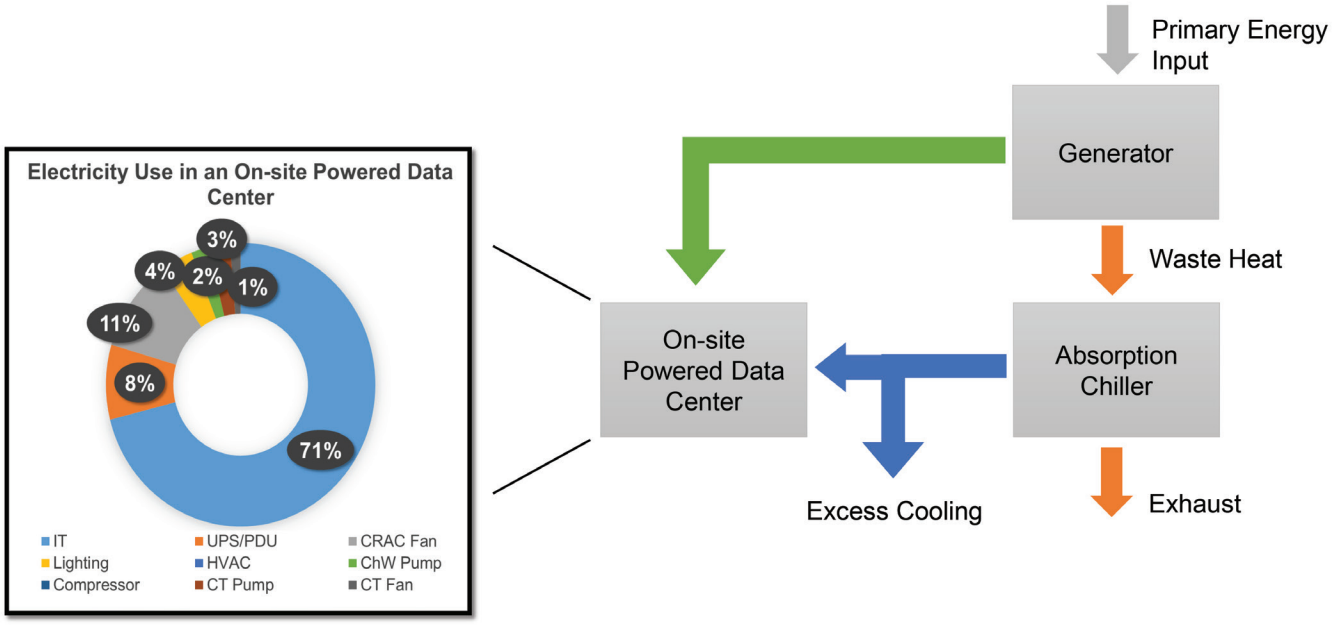

Figure 2: Energy Flow for an On-Site Powered Cogeneration Data Center.

IT power, uninterruptable power supply (UPS) and power distribution unit (PDU) losses, lighting, HVAC and chilled water pumps. The corresponding cooling tower pump power in the cogeneration system can be estimated by scaling the cooling tower pump power in the conventional data center, as observed in *Equation (4)*:

$$P_{CT,pump}^{CG} = P_{CT,pump}\frac{\dot{Q}_{CND}^{CG}}{\dot{Q}_{CND}} \tag{4}$$

Similarly, the cooling tower fan can be scaled based on the condenser load. The corresponding PUE for a cogeneration system based data center, as shown in *Figure 2*, is 1.41. There are many other benefits to generating power on-site that can further reduce the PUE, including water cooling and DC power distribution. These are discussed in more detail in [6].

PRIMARY ENERGY REQUIREMENT OF A COGENERATION SYSTEM DATA CENTER

While PUE can be computed for a cogeneration system based data center, it does not highlight the complete picture when the generator waste heat is used to provide cooling for the data center. Instead, we will focus on the primary energy required for a data center that utilizes a cogeneration system, as described in [6], compared to a traditional grid-powered data center. Referring to *Figure 2*, the generator, which could be a turbine, gas generator, or fuel cell, has a thermal efficiency (η_{th}^{GEN}) defined as:

$$\eta_{th}^{GEN} = \frac{P_{IT}\times PUE^{CG}}{\dot{Q}_{PE}^{CG}} \tag{5}$$

where the product of the IT power and the PUE is the work output of the generator.

The absorption chiller has a thermal coefficient of performance (COP_{th}) defined as,

$$COP_{th} = \frac{\dot{Q}_c}{\varphi \dot{Q}_{ex}} \tag{6}$$

where Q_c is the cooling load, Q_{ex} is the exhaust energy from the generator, and ϕ is a waste heat recovery factor. The recovery factor is a function of the effectiveness and dew point temperature limits of the absorption chiller and describes the fraction of useable waste heat.

The first law of thermodynamics applied to the generator states that:

$$\dot{Q}_{ex} = \dot{Q}_{PE}^{CG} - P_{IT}\times PUE^{CG} \tag{7}$$

By combining *Equations (5), (6) and (7)*, the cooling output of the absorption chiller can be computed as:

$$\dot{Q}_c^{CG} = \varphi COP_{th}\frac{P_{IT}\times PUE^{CG}}{\eta_{th}^{GEN}}\left(1-\eta_{th}^{GEN}\right) \tag{8}$$

As shown in *Figure 2*, part of this cooling is used to cool the data center. However, depending on the generator thermal efficiency, excess cooling ($Q_{c,excess}^{CG}$) may be available to use for other cooling loads, such as a nearby campus building. The amount of excess cooling available is:

$$\dot{Q}_{c,excess}^{CG} = \dot{Q}_c^{CG} - \dot{Q}_{EVAP}^{CG} \tag{9}$$

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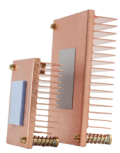

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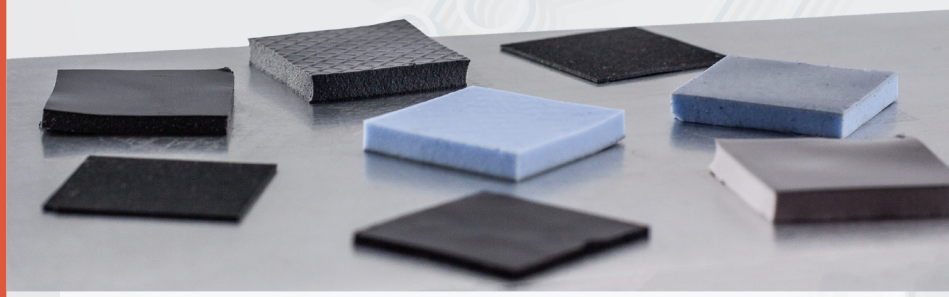

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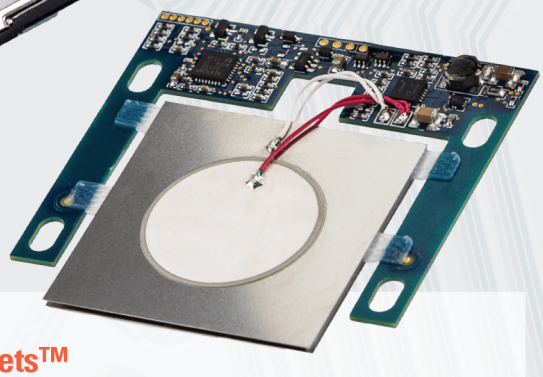

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In a conventional data center, this excess cooling would need to be provided by an electric vapor compression chiller. The primary energy that would be required to generate this excess cooling in a grid-power arrangement is given by:

$$\dot{Q}_{c,offset} = \frac{\dot{Q}^{CG}_{c,excess}}{COP_e \times \eta_{th} \times \eta_{dist}} \quad (10)$$

where COP_e is the coefficient of performance of the electric vapor compression chiller.

Therefore, the net primary energy for the cogeneration system data center is given by subtracting the offset, *Equation (10)*, from the primary energy required by the cogeneration system, *Equation (5)*.

EXAMPLE OF AN ON-SITE POWERED DATA CENTER COMPARED TO A CONVENTIONAL GRID POWERED DATA CENTER

To highlight the energy savings of an on-site power generation system, we can use *Equations (5)* through *(10)* and the data center PUE as shown in *Figures 1* and *2* for the conventional and cogeneration data center, respectively, to compare the primary energy required. We can show this as a percentage savings of the cogeneration system. *Table 1* gives the parameters used in the analysis.

Thermal efficiency, η_{th}	33%
Distribution efficiency, η_{dist}	93%
Electric Coefficient of Performance, COP_e	4.88
Thermal Coefficient of Performance, COP_{th}	1.20
Waste heat reuse factor, φ	58%

Table 1: Parameters used in example analysis of an on-site power data center. Values represent typical values for commercially available equipment.

Figure 3 plots the primary energy savings of the cogeneration system data center versus the generator thermal efficiency. The solid line shows the savings when the cogeneration system's excess cooling can be fully utilized, both to cool the data center and an additional cooling load. The dashed line shows the case where the absorption chiller cooling can only be used to cool the data center. This would be the case if the data center was isolated. It can be seen that compared to a grid-powered data center, with an overall 30% efficiency (generation + distribution), without being able to use the excess cooling, the on-site power system offers little to no advantage until the generator efficiency reaches greater than 25%. Many

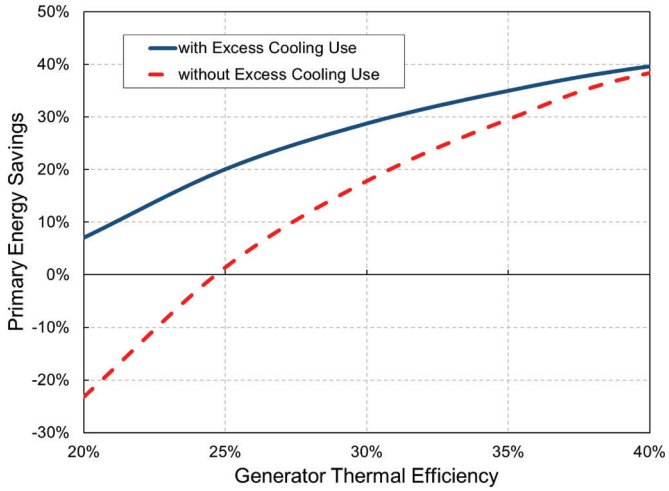

Figure 3: Primary Energy Savings for the Example Cogeneration-based Data Center.

commercial microturbines can now offer thermal efficiencies nearing 28% [7]. When the excess cooling can be used, these systems can provide substantial primary energy savings, in excess of 20%.

As the generator thermal efficiency increases, the amount of primary energy necessary to provide the required data center power decreases, as shown by *Equation (5)*. By the first law of thermodynamics, this also means that less exhaust energy will be available to generate cooling in the absorption chiller. Figure 4 plots the excess cooling, which has been normalized by the data center power, versus the generator thermal efficiency. As the generator efficiency reaches 40%, which may be representative of a large gas generator or a stationary fuel cell, the excess cooling approaches zero. This means that the waste heat from the generator can be used to provide just enough cooling for the data center. Referring back to *Figure 4*, the higher the generator thermal efficiency, the more primary energy savings of an on-site power generation system. Additionally, when the generator efficiency nears 40%, the data center needs to rely less on having an additional nearby source to utilize the excess cooling, as seen by the solid and dashed lines converging.

CONCLUSIONS

This article showed how a simple thermodynamic analysis can be effectively utilized to analyze alternative power and cooling options for data centers. It highlighted the benefits of on-site cogeneration for data center applications, where the thermal and electric demands are strongly correlated. The article also described a primary energy methodology that shows the benefits of an on-site system compared to a traditional grid-powered data center.

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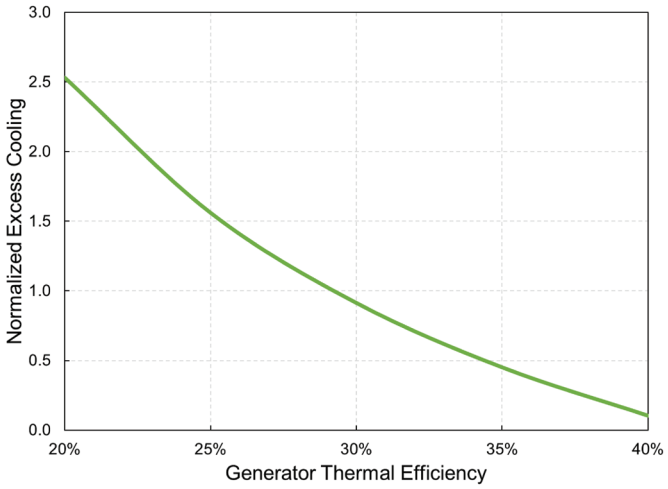

Figure 4: Data Center Excess Cooling Available for the Example Cogeneration System Data Center.

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Greek Symbols		Nomenclature	
η	Efficiency	COP	Coefficient of Performance
φ	Waste heat reuse factor	P	Power, kW
Superscripts		PUE	Power Usage Effectiveness
CG	Cogeneration	$\dot{Q}$	Energy, kW
GEN	Generator		
Subscripts			
c	Cooling		
CND	Condenser		
CT	Cooling tower		
$dist$	Distribution		
e	Electric		
$EVAP$	Evaporator		
ex	Exhaust		
IT	Information technology		
PE	Primary energy		
th	Thermal		

Note: The above are symbols included in this article.

Cooling Matters

News of thermal management technologies

AIR FORCE INQUIRES ABOUT THERMAL MGMT.SOLUTIONS FOR FUTURE AIRCRAFT

8/11/15 - The U.S. Air Force is looking into new thermal management techniques to cool the electronics in future fighter aircraft.

"Officials of the Air Force Research Laboratory at Wright-Patterson Air Force Base, Ohio, issued a broad agency announcement Friday (BAA-AFRL-RQKP-2015-0002) for the Hybrid-Cycle Power and Thermal Management System (PTMS) project," according to Military & Aerospace Electronics.

"The Air Force Research Lab's Power and Control Division, Mechanical & Thermal Systems Branch are asking industry for electronics cooling ways to blend air-cycle cooling, vapor-cycle cooling, chilled fuel, and other thermal energy storage mechanisms to keep electronics cool on future jet fighters," according to researchers.

Source: Military & Aerospace Electronics

3D WHITE GRAPHENE YIELDS FAN-FREE COOLING/THERMAL MANAGEMENT SOLUTIONS

7/20/15 - Researchers from Rice University have discovered that 3D White Graphene could help cool small-scale electronic devices by itself.

When the research group completed simulations of heat flows through 3D white graphene structures, which are made of boron nitride, the normal 2D structure took the form of normal hexagonal structure of graphene. The team then investigated "how its natural heat conduction properties could be exploited in 3D arrangements."

"Simulations show that 3D structures of white graphene-sheets of the 2D stuff held together with boron nitride nanotubes- quickly move heat in all directions. But they also show that by tuning the lengths and densities of the interconnecting tubes, the material can be tuned to channel heat in specific directions- shorter ones slow conduction, while longer ones speed it up," according to Gizmodo.

Even though the team's research is solely based on simulations, they remain positive that this discovery will help introduce new kinds of 3D thermal management systems for small electronic devices in the near future.

Source: Gizmodo

CALIFORNIA ENERGY CODE UPDATED; NEW REGULATIONS FOR COOLING DATA CENTERS

7/28/15 - The California Energy Code, also known Title 24 of the CA Code of Regulations – part 6, has been revised. The new revision implements new regulations for cooling data centers and server rooms in order to improve efficiency, reduce daily operation costs, reduce carbon footprints and simplify cooling models.

The new rules apply to computer rooms, which Title 24 defines as: "A room whose primary function is to house electronic equipment and that has a design equipment power density exceeding 20watts/ft² (215 watts/m²) of conditioned floor space."

The new requirements affect the way data centers are cooled. The new CA Title 24 Code Requirements include: economization, airside economization, waterside economization, reheat prohibited, humidification, fan efficiency, fan control and air containment.

Source: Datacenter Journal

Datebook

SEPTEMBER 15-17	SEPTEMBER 16-19	SEPTEMBER 22-24	SEPTEMBER 22-24
Electric & Hybrid Vehicle Technology Expo NOVI, MICHIGAN, U.S. www.evtechexpo.com	**LED China 2015** SHANGHAI, CHINA www.chinaexhibition.com	**LED Professional Symposium & Exhibition 2015** FESTSPIELHAUS BREGENZ, AUSTRIA www.heatmanagement.com/en/announcements/events	**Advanced Technology Workshop and Tabletop Exhibit on Thermal Management** LOS GATOS, CALIF., U.S. www.imaps.org/thermal

LEDS TO MOVE DATA FASTER IN ELECTRONICS

8/4/15 - University of Virginia engineering researchers have come up with a way for LEDS to move data to wireless devices faster.

This process involves "using light waves from light-emitting diode fixtures to carry signals to wireless devices at 300 megabits per second from each light. It's like having a whole wi-fi system all to yourself; using light waves, there would be more network access points than with radio waves, so less sharing of the wireless network," according to researchers.

"Visible light communications has the potential to significantly increase the speed of Internet connection in multiuser indoor environments due to the broad bandwidth of the visible light. It will offer a huge energy saving for the nation since energy is already used for lighting, and thus does not need to be expended for communications," the team concluded.

Source: Phys.org

NEW MATERIAL DECREASES ENERGY USAGE IN ELECTRONICS

8/4/15 - Researchers have determined that gallium nitride (GaN) could become the next best semiconductor for electronics because it would immensely cut energy usage.

Cambridge Electronics Inc. (CEI) has announced a new line of GaN transistors and power electronic circuits. This line promises to reduce energy usage by 10 to 20 percent in consumer electronics, data centers and electric cars by 2025.

CEI plans to use these transistors to make data centers use less energy, electric cars more powerful and cheaper to build and power adapters one-third of the size, according to Phys.org.

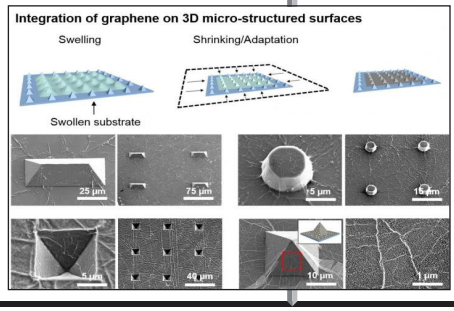
Source: Phys.org

3D SHAPES FORMED FROM FLAT SHEETS OF GRAPHENE

3/9/15 - A team from the University of Illinois at Urbana-Champaign has developed a new method for forming 3D shapes from flat 2D sheets of graphene. This development will pave the way for flexible electronics and integrated systems that are graphene and MEMS hybrid devices.

Integrating 2-D graphene sheets onto 3D structured surfaces allows the graphene to hold its structure; however, the 3D features and dimensions vary from 3.5 to 50 µm.

Source: Science Daily



HPC NETWORKS SUCCESSFUL LIQUID COOLED FOR FIRST TIME

7/20/15 - Icetope, a company that specializes in the liquid cooling of electronics, announced it has successfully liquid cooled HPC networks.

"Liquid cooling systems work by transferring all the heat directly into liquid. The waste heat is then removed in the form of hot water, which is pumped around the cabinet and can be re-purposed for domestic heating," according to Electronics Weekly.

The company developed a "fan-less Mellanox-based InfiniBand and Ethernet network and interconnect switch for supercomputer (HPC) systems."

Source: Electronics Weekly

SEPTEMBER 29-31

SAE 2015 Thermal Management Systems Symposium
TROY, MICH., U.S.
http://saeevents.org

OCTOBER 6-8

THERMAL LIVE 2015
ONLINE
http://thermallive2015.com

THERMAL LIVE 2015

OCTOBER 27-30

Hong Kong International Lighting Fair
HONG KONG, CHINA
www.hktdc.com

DECEMBER 7-10

Gartner Data Center, Infrastructure & Operations Mgmt. Conference
LAS VAGAS, NV, U.S.
www.gartner.com/events

An Additive Design Methodology for Heatsink Geometry Topology Identification

Robin Bornoff and John Parry
Mentor Graphics Corporation

INTRODUCTION

ESTABLISHED HEATSINK manufacturing processes such as extrusion, casting and milling constrain the achievable topology and geometry of the heatsink. The advent of metallic 3D printing (additive manufacture) processes such as selective laser melting (SLM) may remove many of these constraints, forcing the designer to reconsider the approach taken to determine a thermally-efficient heatsink design.

Classic heatsink design involves considering a parametrically specified heatsink topology then optimising those parameters to meet thermal, weight and cost constraints. Those parameters for example might be base thickness, number of fins, fin thickness, fin spacing, and/or fin height. In many ways it is the manufacturing process that dictates those parameters and by how much they can vary. So, how might a heatsink design process be performed if those constraints are no longer imposed?

An additive design methodology has been developed by the Authors that allows a non-parametric topology of the heatsink to be identified as part of an iterative simulation-based process. At its heart, the additive design methodology involves inspection of the performance of an initial design, a determination of where that design should be minimally modified. The modification is then made, and the performance re-evaluated. This process is repeated until a design criterion is met.

This is a subset of a methodology that would entail a minimal improvement made at every possible location, the most advantageous improvement implemented and the process repeated. This in turn is a subset of a methodology that would entail every possible topology being simulated and the best one identified. The present approach aims to be tractable in terms of (simulation) time whilst still having the flexibility to identify an application-specific topology, and is an application of Bejan's Constructal Law [1], which states:

"For a finite-size system to persist in time (to live), it must evolve in such a way that it provides easier access to the imposed currents that flow through it."

Such a law can be said to underpin the formation of many systems both animate and inanimate, including, but not limited to, the branching nature of lightning, rivers, lungs and trees. Various studies based on the Constructal law have focused on "volume to point" (VP) flow systems: thermal conduction of heat [2], liquid flow in a porous media [3] and air flow in lungs [4].

Heatsink behaviour is also a VP problem, though taken as a volume of "cold" used quench a point (rather a small area) heat source. It is not surprising that there are analogies between heatsinks and, say, trees. The heatsink

Robin Bornoff achieved his Mechanical Engineering Degree from Brunel University in 1992. He was awarded a Ph.D. from Brunel University in 1995 for CFD research. He joined Mentor Graphics Corporation, Mechanical Analysis Division (formerly Flomerics Ltd) after his Ph.D. as an application and support engineer, specializing in the application of CFD to electronics cooling and the design of the built environment. Bornoff has served as the Product Manager responsible for the FloTHERM, FloVENT and FloTHERM PCB software. He is currently Market Development Manager.

John Parry, a chemical engineer by training, got involved with CFD more than 30 years ago, joining Flomerics Ltd. when it founded in 1989, coordinating EC-funded and other projects and overseeing the technical integration of MicReD into the company. Now part of Mentor Graphics, John is the Mechanical Analysis Division's Electronics Industry Manager. Parry's technical contributions include developing compact thermal models for fans, heat sinks, chip packages and LEDs, co-inventor of BottleNeck and ShortCut numbers, and applying Design of Computer Experiments and optimization techniques. He serves on the JEDEC JC15 and various conference committees.

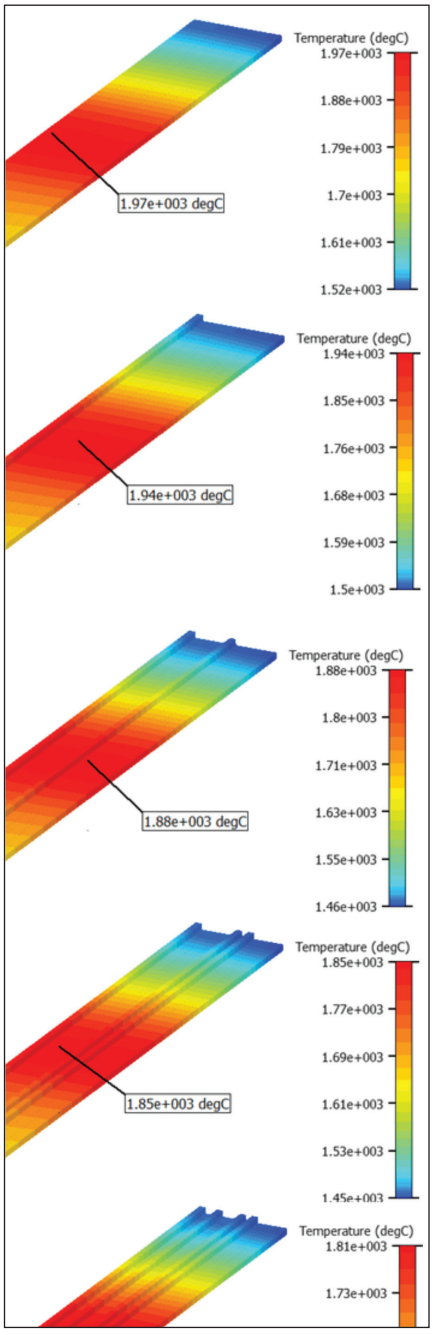


Figure 1: Initial steps of the additive design process.

base, like the tree trunk, enables that which is to flow (heat in a heatsink, liquid in a tree) to pass to the area extending portion of it. The heatsink fins, like branches and leaves of a tree, then transfer what is flowing out to their ambient.

The Constructal law can be seen in action in the organic growth exhibited by the additive design methodology

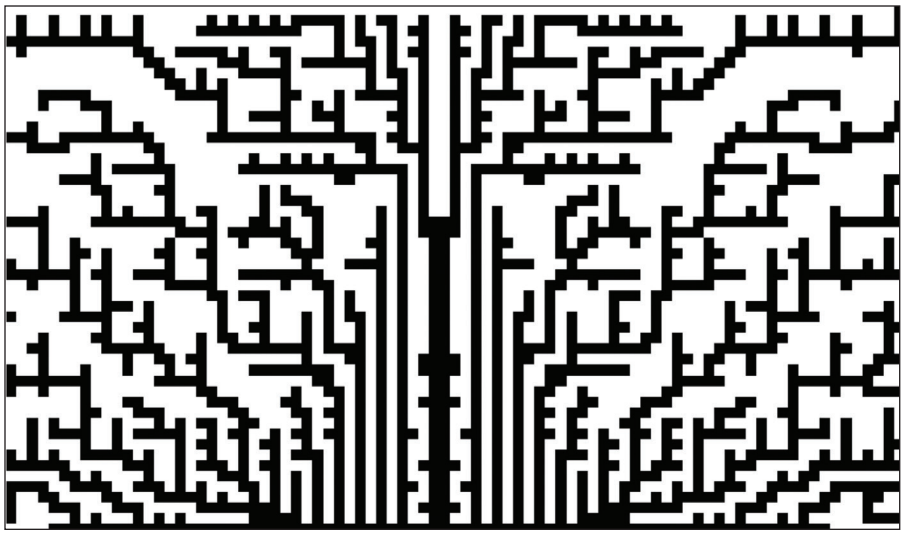


Figure 2: Heatsink profile after one 'year' of growth.

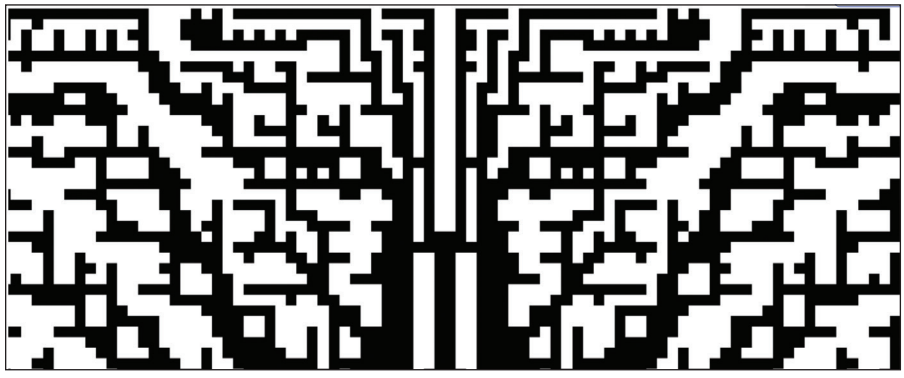


Figure 3: Forced convection heatsink profile after three 'years' of growth.

reported in this article, which is abstracted from Reference [5].

APPLICATION TO A FORCED CONVECTION COOLING ENVIRONMENT

When applied to heatsink design the additive design process starts by considering the thermal performance of a thin section of heatsink base placed on a heat source, a key from which the heatsink geometry may evolve. This initial geometry is simulated in a cooling environment and the maximum surface temperature location identified. It is postulated that an improvement in the thermal performance of the heatsink can be achieved by increasing the surface area at the point of highest temperature. To achieve this, an additional piece of heatsink material geometry is added to the heatsink, on that face, and the modified heatsink geometry re-simulated. For this study a forced convection cooling environment is used and a 1mm x 1mm full length rib is chosen as the additive geometric shape. The first 5 steps in the additive design process are shown in Figure 1. The heatsink design space is 100mm x 100mm x 50mm. There is allowance for 25mm of bypass on the top and the two sides of the heatsink. The initial heatsink base geometry fills the design space in the flow direction, covers the heat 30mm x 30mm heat source in the spanwise direction, is 1mm thick and has a thermal conductivity of 205 W/m-K. The inflow is set to 3m/s with an ambient pressure condition at the outlet.

There is no guarantee that the addition of geometry at the hottest point will always cause a decrease in heatsink thermal resistance. If a geometry ad-

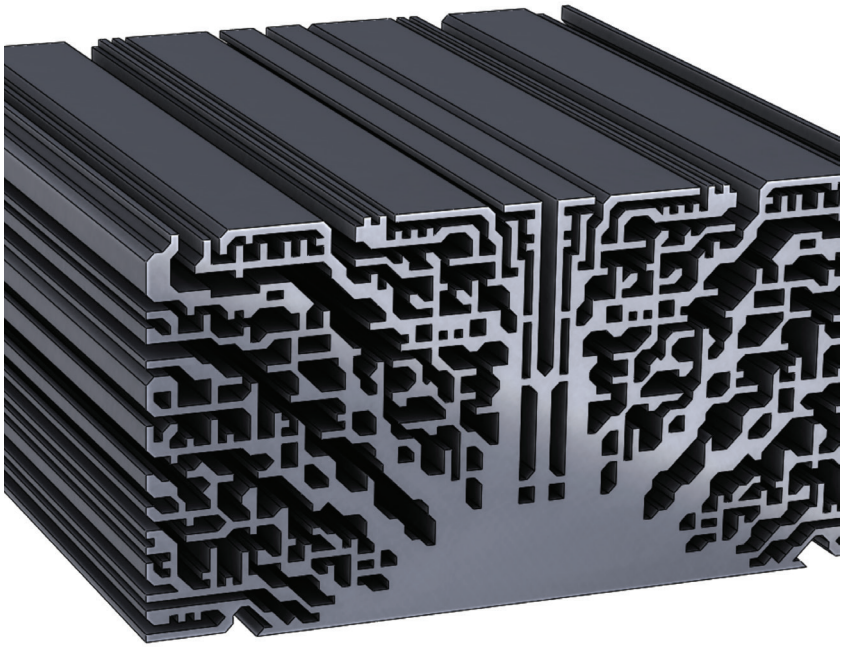


Figure 4: Final chamfered additively designed forced convection heatsink.

dition is made that causes an increase in thermal resistance then that added geometry is removed and the location marked so as not to be considered again during the growth process. The growth process concludes when the heatsink has grown to fill a defined design volume and there are no locations left to extend the geometry so as to improve the thermal performance. We define this as the first "year" of growth. A front view of the geometry after this first year of growth is shown in *Figure 2*. Note that symmetry was assumed for the computational fluid dynamics (CFD) simulations.

A subsequent second year of growth was allowed by resetting all those geometry addition locations that had caused an increase in the thermal resistance of the heatsink during the first year. Some of those locations of area extending that had proved to be detrimental initially, proved to be highly advantageous in this second year of growth. Specifically closer to the heat source where the second year of growth saw a thickening of the base so as to facilitate the flow of heat to the now large surface area (but thin cross section) branched fins.

This resetting and continued growth was repeated for a third "year", after which no subsequent year of growth provided any further improvement in thermal performance and the additive design process was ended. The final heatsink topology is shown in *Figure 3.*

An evident deficiency of the use of a square section rod to grow the geometry is that any angled or curved topological features that manifest will have stair-stepped edges. Although it could be argued this might increase heat transfer, it may be offset by the increase in surface friction. A smoothing stage is therefore conducted where the stepped angled sections are (manually) chamfered (Figure 4). This results in a slight (1.8%) improvement in thermal performance.

COMPARISON TO PARAMETRICALLY DEFINED HEATSINK PROFILES

It was neither the intention nor the outcome of this study to demonstrate a superior thermal performance of an additively designed heatsink compared to more classic heatsink topologies. However, to put the thermal performance of the additively designed heatsink into perspective, it is compared to two other heatsinks with parametrically definable topologies.

A standard extrusion will have manufacturing constraints such as the maximum aspect ratio of each fin (and similarly fin gap) and minimum fin width. A maximum fin aspect ratio of 10:1 and a minimum fin thickness of 1mm were constraints set in an optimization study of a standard extrusion. Base thickness, number of fins, fin thickness and fin height were set as design variants. A design of experiments was used to populate the design space followed by a gradient based sequential optimisation approach to identify a thermal resistance cost function minima [6].

The same optimization approach was adopted for a heatsink profile that did not have the fin aspect ratio constraint imposed. The fin thickness however was set fixed at 1mm to ensure a valid comparison with the 1mm minimum feature size in the additively designed heatsink.

Comparison of the thermal performance of all three heatsinks is shown in *Figure 5*.

The additively designed heatsink "held its own", with a thermal resistance less than 5% greater than a parametrically defined profile whose topology is tailored but bound to such unidirectional forced convection environments. Pressure drops for the standard extrusion, unconstrained profile, and additively designed heatsink are 6.9Pa, 7.2Pa and 8.9Pa, respectively.

Although both the thermal resistance and pressure drop are slightly worse than the classic heatsink with an unconstrained profile, the strength of the additive approach is its adaptability to complex shaped design volumes and to situations where the heat source is non-uniform due to power or layout variations, where taking a parametric approach might over constrain the design.

FUTURE WORK

Instead of using surface temperature as an indicator of where the heatsink would benefit from an area extension, other simulated parameters could be chosen instead. For example the maximum thermal BottleNeck number [7] indicates where there is a lot of heat flow and where the heat is finding it difficult to

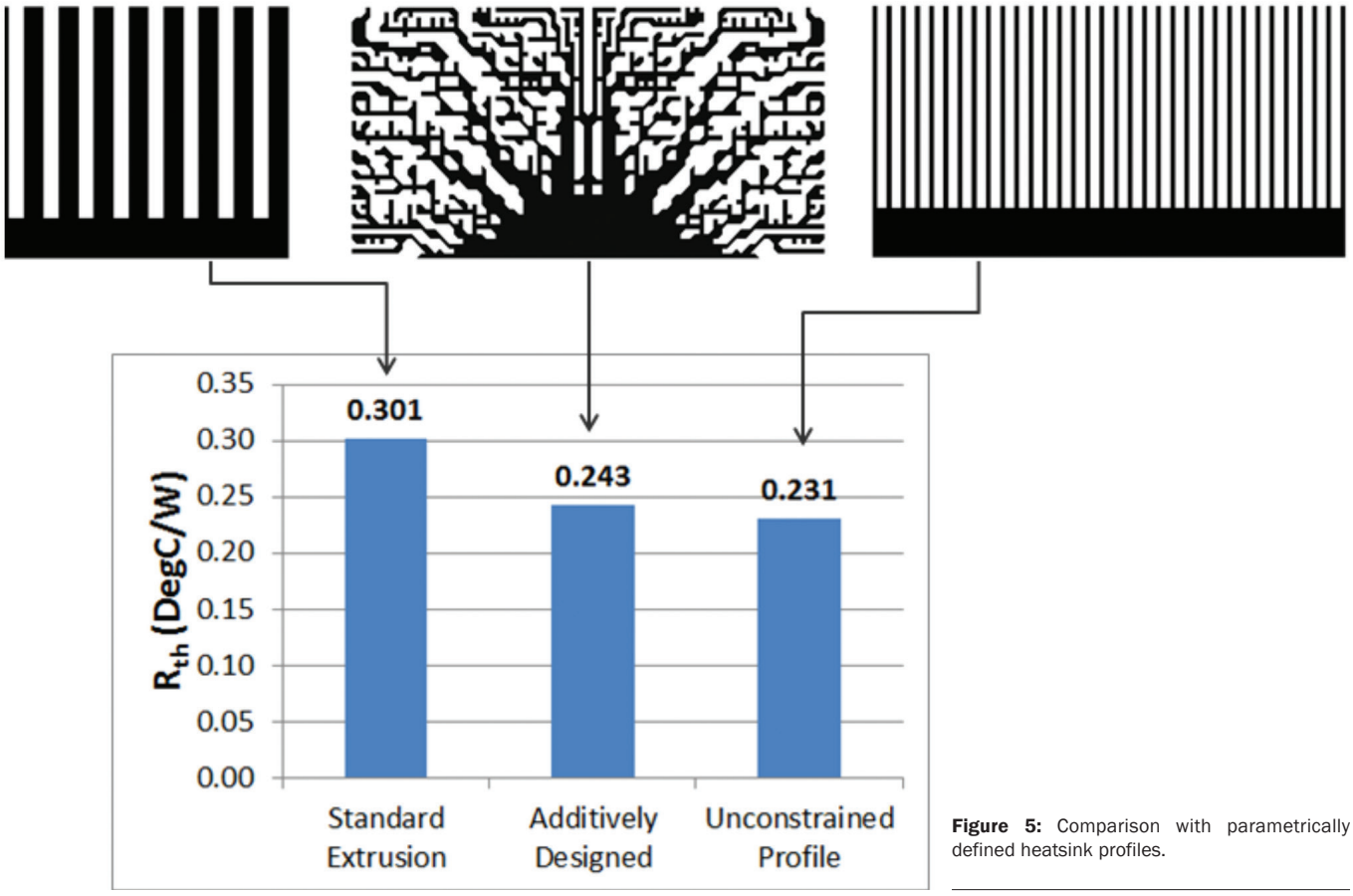


Figure 5: Comparison with parametrically defined heatsink profiles.

flow, i.e. where it is bursting to get out. Use of this parameter to determine where best to incrementally grow the heatsink might result in topologies with better overall thermal performance.
Also, the additive design methodology need not be constrained to 2D profiles. The choice of the additive rib geometry was artificial in that it imposed a 2D extruded type profile. The same "evaluate and add geometry" process could be applied using a cuboidal additive geometry smaller than the design space it is attempting to fill so that it has faces that may be hottest in any one of 5 directions, allowing the heatsink geometry to evolve not just up/down/left/right, but also forwards and backwards. This would allow much more complex geometries and potentially superior thermal performances to be achieved.

CONCLUSIONS

An additive design methodology has been investigated, applied to a forced convection cooled heatsink design. It has been shown that the resulting thermal performance of the additively designed heatsink topology is within 5% of that of a parametrically optimised defined base/fin type.
Generally this methodology could be applied to other design challenges that:
1. Can be quantified in terms of a location that exhibits a behavioural condition indicative of the performance to be optimised.
2. Can be geometrically evolved (grown) using an additive geometry shape that has the intention of improving that performance metric.

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All You Need to Know About Fans

Mike Turner
Sigma Squared Decisions Inc.

Editor's note: The focus of Electronics Cooling is to present articles that are of broad interest to our readership. In celebration of our 20th year, we will be running our most popular articles that are informative and useful to our readers. Based on a review of website traffic from January to July 2015, the following article authored by Mike Turner was deemed one of the most read on the website. It was originally published in Electronics Cooling in 1996 (Vol. 2, No. 2, pp. 10-13) and its selection demonstrates the archival value of Electronics Cooling articles to our readership. Visit www.electronics-cooling.com for more popular articles.

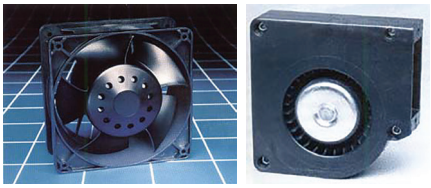
INTRODUCTION

BASIC FAN/BLOWER DESCRIPTION Fans can be thought of as low pressure air pumps that utilize power from a motor to output a volumetric flow of air at a given pressure. A propeller converts torque from the motor to increase static pressure across the fan rotor and to increase the kinetic energy of the air particles. The motors are typically permanent split capacitor alternating current (AC) induction motors or brushless direct current (DC) motors. We shall now look at this system in more detail.

TYPES OF FANS AND BLOWERS

Air moving devices are generally described as being either a type of fan (*Figure 1a*) or a centrifugal blower (*Figure 1b*). The main difference between fans and blowers is in their flow and pressure characteristics. Fans deliver air in an overall direction that is parallel to the fan blade axis and can be designed to deliver a high flow rate, but tend to work against low pressure. Blowers tend to deliver air in a direction that is perpendicular to the blower axis at are relatively low flow rate, but against high pressure.

There are several types of fans, some of the most common being propeller, tube axial and vane axial styles. Propeller fans are the simplest type of fan, consisting of only a motor and propeller. One problem with propeller fans is that tip vortices are produced by the pressure differential across the airfoil section.



(a) Axial fan. (b) Centrifugal blower.

Figure 1: Typical fan and blower designs.

A tube axial fan (the most common type in electronic cooling systems) is similar to a propeller fan, but also has a venturi around the propeller to reduce the vortices. The vane axial fan has vanes that trail behind the propeller in the airflow to straighten the swirling flow created as the air is accelerated.

Centrifugal blowers may have a forward curved wheel, a backward curved wheel, or be of the squirrel cage variety.

BASIC AERODYNAMICS

Fans are of such common use that a basic understanding of the aerodynamics is appropriate. This understanding begins with the recognition that the blades of a fan propeller resemble the wing of an airplane, and as such follow the same aerodynamic laws. For example, a fan blade produces lift when the chord is elevated from the direction of the relative wind as shown in *Figure 2*.

The elevation angle is referred to as the angle of attack (AOA). The greatest airflow delivery from a fan occurs when the AOA is at a minimum, but the pressure differential across the fan is zero. As the AOA is increased, the airflow delivery decreases and the pressure differential increases. The airflow can decrease to nearly zero, but will also deliver the maximum pressure differential in this condition, which is called the shut-off point. When an AOA is reached where the air will no longer flow smoothly and begins to separate from the blades, an "aerodynamic stall" condition exists.

Since a fan is a constant volume machine, it will move the same volumetric flow rate of air irrespective of the air density. However, the mass flow rate does change as the density changes.

This becomes important when equipment is expected to operate at altitudes

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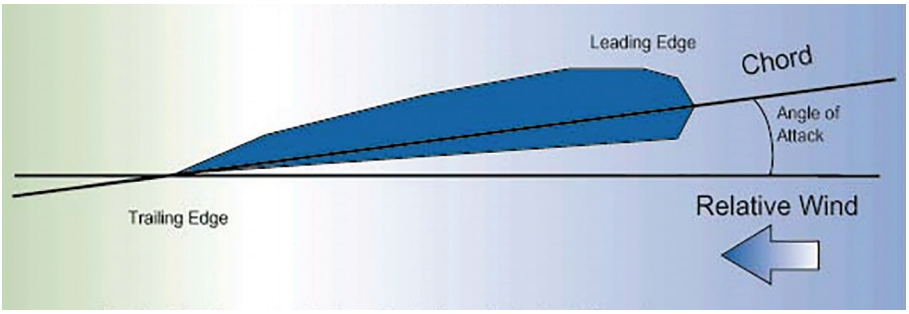

Note: The cord is a line extending from the leading edge to the trailing edge. Angle of attack is the angle formed between the relative wind and chord.

Figure 2: Nomenclature for an airfoil.

significantly greater than sea level. Therefore the volumetric flow rate required at altitude (low density air) will be greater than that required to achieve the same cooling as at sea level.

THE FAN CURVE

All of the aerodynamic aspects of a fan are exhibited in a fan curve such as is shown in *Figure 3*. The fan performance curve is one of the few curves that are read from right to left, because you start with healthy aerodynamic flow and follow it through to aerodynamic stall.

However, in contrast to an airplane wing, there is life after stalling in a fan. A stalled fan continues to deliver air, but at an increased static pressure and a decreased volumetric flow rate, and also at the cost of an increase in noise. If noise is not a consideration, the fan can be utilized in this condition.

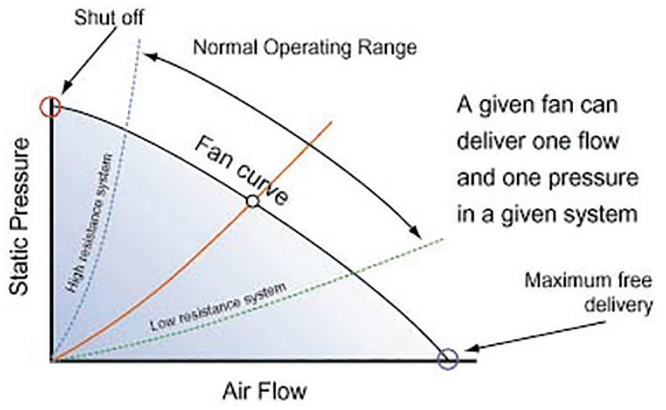

Figure 3: Fan/system interaction.

An energy viewpoint is helpful in understanding the fan performance curve. For example, at the shut-off point, the fan is in the condition of the maximum potential energy. At free delivery, the fan is in the condition of the maximum kinetic energy. Although neither of these extreme conditions are likely to occur in practice, they can be useful parameters in comparing fans.

The governing principle in fan selection is that any given fan can only deliver one flow at one pressure in a particular system.

This "operating point" is determined by the intersection of the fan static pressure curve and the system pressure curve. *Figure 3* illustrates the operating points of both high and low resistance systems. It is best to select a fan that will give an operating point being toward the high flow, low pressure end of the performance curve to maintain propeller efficiency and to avoid propeller stall. Each particular electronic packaging system should be analyzed for possible reduction in the overall resistance to airflow. Other considerations, such as available space and power, noise, reliability, and operating environment should also be brought to bear on fan choice.

STEPS TO FAN SELECTION

ESTIMATE THE REQUIRED AIRFLOW

Before selecting a fan, obtain as accurate an estimate as possible of the heat to be dissipated, because the overall system air temperature differential above the inlet ambient is directly proportional to the heat dissipated. It is then possible to estimate the amount of required cooling air. The basic heat transfer equation is:

$$\dot{Q} = \dot{m} C_p \Delta T \qquad (1)$$

where: Q = amount of heat transferred to system *(Watts)*, (m) = mass flow rate of air *(kg/s)*, C_P= specific heat of air *(J/kg.K)*, ΔT = desired air temperature differential: cabinet to ambient outside air (°C).

The relationship between mass flow rate and volumetric flow rate is:

$$\dot{m} = \rho G \qquad (2)$$

where: ρ = air density, *(kg/m³)*, G = volumetric flow rate *(m³/s)*

The required volumetric flow rate is then calculated from:

$$G = \dot{Q}/(\rho C_p \Delta T) \qquad (3)$$

This yields a rough estimate of the airflow needed to dissipate a given amount of heat at sea level. It should be noted that it is the mass flow rate of air, not its volumetric flow rate, that governs the amount of cooling.

ESTIMATE THE ACTUAL AIRFLOW

The preceding steps indicated the necessary procedure to estimate the required airflow in order to obtain the desired overall air temperature rise ΔT. However, it was also indicated that the actual operating airflow is determined by the intersection of the fan curve and the system resistance curve. There are three options available for estimating this operating point: (i) experimental measurement using a thermal/mechanical mockup of the system, (ii) calculation of the operating point using airflow

network methods [1], or (iii) calculation of the system airflow using computational fluid dynamics (CFD) software (available from commercial software companies).

The experimental procedure can be used to measure the total airflow for specific fans or several pressure-airflow data pairs can be measured to develop a complete system resistance curve. The latter experimental method will then require the Designer to superimpose the selected fan pressure versus airflow curve and system resistance curve to obtain the operating airflow.

The airflow network procedure provides adequate results when the geometry is simple and the flow path within the cabinet is known or a rough estimate can be made. In many practical applications, however, the Designer deals with complex three dimensional flow paths that are not known from the very first instance. In these situations, CFD software can be used. The fan performance curve can be supplied as an input to the CFD software and the software system allowed to determine the operating point and system resistance. CFD works by numerically solving the governing equations of flow and heat transfer in three dimensions and takes into account the effects of turbulence and gravity. CFD can be used to study the performance of fans in series and parallel arrangements as well as optimize the location with respect to other objects inside the cabinet. Both of the computational procedures require a static pressure versus airflow curve for the fan in question.

Irrespective of which method is chosen to estimate the system airflow, all packaging systems are characterized by a system resistance curve of the type shown in *Figure 3*. System resistance curves may usually be expressed as a non-linear expression of pressure versus airflow:

$$\Delta P = K\rho G^n \qquad (4)$$

where: ΔP = system pressure loss, K = a load factor specific to the system, n = a constant which varies between 1 and 2 depending on whether the flow is either completely laminar (n=1) or turbulent (n=2).

If the estimated value of the actual airflow is significantly less than the required value, the packaging system should be examined for regions where the airflow resistance could be reduced. Should it fail to provide an answer a different fan or perhaps even multiple fans should be considered. The search for a different fan is a simple matter of reviewing the catalogs of the various fan vendors. The consideration of multiple fans is a little more complex.

CONSIDER MULTIPLE FANS

Combining fans in series or parallel can sometimes achieve the desired air flow without greatly increasing the system package size or fan diameter. Parallel operation is defined as having two or more fans blowing together side by side. The performance of two fans in parallel will increase the volume flowrate (double at maximum delivery). The best results for parallel fans are achieved in systems with low resistance. A fan curve simulating multiple, identical fans in parallel may be constructed by scaling the fan curve air flow axis data in direct proportion to the number of fans.

In series operation, the fans are stacked one upon the other, resulting in an increase of static pressure (doubling at shut-off, but less elsewhere). The best results for series fans are achieved in systems with high resistance. A fan curve simulating multiple, identical fans in series, may be constructed by scaling the fan curve pressure axis data in direct proportion to the number of fans.

In both series and parallel operation, particularly with multiple fans (5, 6, 7, *etc.*), certain areas of the combined performance curve will be unstable and should be avoided. This instability is unpredictable and is a function of the fan and motor construction and the operating point.

THE FAN LAWS

Sometimes it may be necessary to determine the output of a given fan under other conditions of speed or density, or to convert the known performance of an air mover of one size to that of another geometrically similar unit of a different size. The fan laws permit this.

Geometrically similar fans can be characterized by the following four equations *(next page)*:

Constants	Variable	Fan Laws
Diameter (*D*) Density (ρ)	Speed (*N*)	$G_2 = G_1\left(\frac{N_2}{N_1}\right)$ $P_2 = P_1\left(\frac{N_2}{N_1}\right)^2$ $HP_2 = HP_1\left(\frac{N_2}{N_1}\right)^3$
Speed (*N*) Density (ρ)	Diameter (*D*)	$G_2 = G_1\left(\frac{D_2}{D_1}\right)^3$ $P_2 = P_1\left(\frac{D_2}{D_1}\right)^2$ $HP_2 = HP_1\left(\frac{D_2}{D_1}\right)^5$
Diameter (*D*) Speed (*N*) Volumetric Flow Rate (*G*)	Density (ρ)	$P_2 = P_1\left(\frac{\rho_2}{\rho_1}\right)^2$ $HP_2 = HP_1\left(\frac{\rho_2}{\rho_1}\right)^5$
Diameter (*D*) MassFlow Rate ($\dot{m}$)	Density (ρ)	$G_2 = G_1\left(\frac{\rho_2}{\rho_1}\right)$ $P_2 = P_1\left(\frac{\rho_2}{\rho_1}\right)$ $N_2 = N_1\left(\frac{\rho_2}{\rho_1}\right)$ $HP_2 = HP_1\left(\frac{N_2}{N_1}\right)^2$

Table 1: Summary of fan laws.
Note: Subscripts 1 and 2 refer to two different fan operating conditions.

Volumetric Flow Rate: $G = KND^3$ (5a)
Mass Flow Rate: $m=K\rho ND^3$ (5b)
Pressure: $P=K\rho N^2D^2$ (5c)
Power: $HP=K\rho N^3 D^5$ (5d)
where: N = fan speed in RPM, D = fan diameter.

From these relationships, it is possible to calculate a fan performance at a second condition. *Table 1* is a summary of the fan law equations in a form useful for fan analysis.

CABINET COOLING HINTS

In addition to selecting a fan, there may be some choice in the location of the fan or fans, and in this regard, the illustration in *Figure 4* may prove useful. The following comments should also be kept in mind with regard to fan location:

1. Locate components with highest heat dissipation near the enclosure air exits.
2. Size the enclosure air inlet and exit vents at least as large as the venturi opening of the fan used.
3. Allow enough free area for air to pass with velocity less than 7 m/s.
4. Avoid hot spots by spot cooling with a small fan.
5. Locate components with the most critical temperature sensitivity nearest to inlet air to provide the coolest air flow.
6. Blow air into cabinet to keep dust out, i.e. pressurize the cabinet.
7. Use the largest filter possible, in order to (i) increase dust capacity and (ii) reduce pressure drop.

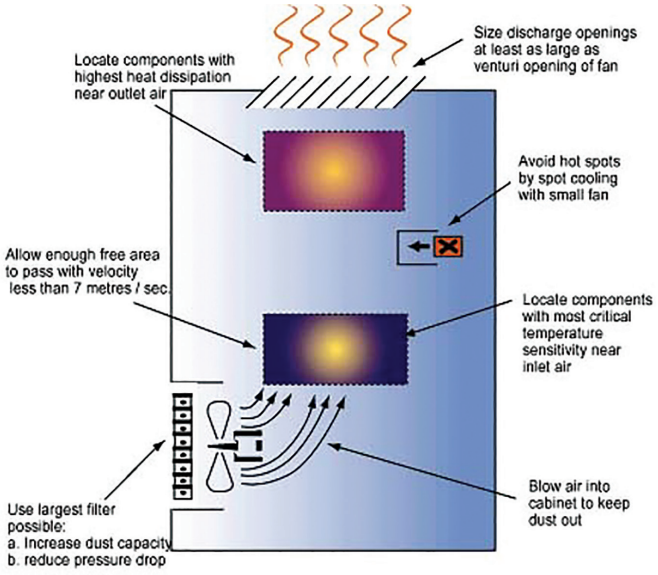

Figure 4: Cabinet cooling hints.

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An Efficient Approach for Multi-Scale Thermal Modeling of Integrated Circuits

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INTRODUCTION

AS THE INTEGRATED CIRCUIT (IC) CHIP AND PACKAGE continue to scale down, the power density and thermal and electrical resistance of these devices continue to increase, resulting in the creation of local hot-spots that are dependent on layout and workload. This can cause major variation in the performance and efficiency of devices. Heat is mainly generated in the transistors which have a characteristic length scale of tens of nm (~10^{-8} m). The generated heat is conducted through the chip and package components such as substrate, mold compound, and heatsink and is ultimately removed from the package via convention. At the package level, the characteristic length scale is on the order of tens of cm (10^{-1} m). Additionally, the transient thermal events in IC devices vary from microsecond (10^{-6} s) at the transistor level to tens of seconds (10^{2} s) at the package level. Therefore, Joule heating in IC devices is a multi-scale problem both in length and time scales.

To model such geometries, traditional full field finite element (FE) and finite difference (FD) methods are computationally inefficient as they require large number of computational nodes or elements. Hence, they are impractical for any parametric study. Several multi-scale modeling methodologies have been developed to determine the thermal profile in IC devices, such as thermal impedance networks [1, 2] and compact models [3]. However, they generally suffer from low accuracy in the presence of complex geometries and boundary conditions, as well as nonlinearity in the heat diffusion equation [4, 5]. Another limitation of such models is the difficulty in handling fluid/solid interactions. In addition, the majority of the previous methods have been focused on steady-state Joule heating in IC devices. In many applications it is necessary to study the effect of transient heat conduction due to the pulsed nature of the electric currents in the transistors and interconnects. Therefore, there is a need for the development of high fidelity transient multi-scale thermal models that overcomes the challenges faced by existing thermal models.

Barabadi *et al.* [6] developed a computationally efficient hybrid multi-scale

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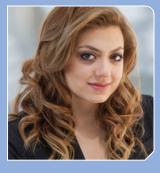

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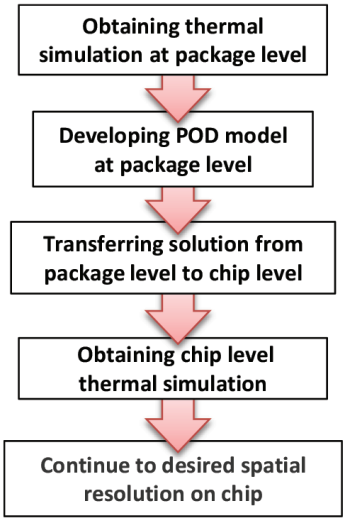

Figure 1: Flowchart of the hybrid scheme used for multi-scale transient thermal modeling.

approach for transient thermal modeling of microelectronics. The model combines two different and well-established multi-scale concepts: "Progressive Zoom-in" (e.g. [7]), and "Proper Orthogonal Decomposition (POD)" ([8]). The method is capable of modeling several decades of length scales, from tens of millimetres at "package" level to tens of micrometres at "chip component" level and to potentially several nanometres at "interconnects" (not included here) level. This characteristic of the proposed model also applies for time scales ranging from tens of seconds to microseconds corresponding to different thermal events. The hybrid scheme can also accurately and rapidly predict the thermal responses of an IC device for different power input profiles based on only a few representative detailed simulation.

It is shown that the proposed model can reduce the computational time by approximately two orders of magnitude at every step of modelling with less than 8% error in simulation[9].

In this article, we briefly describe the hybrid scheme used for transient thermal modelling of a Flip Chip Ball Grid Array (FCBGA) package with an embedded die and its function blocks. To further demonstrate the capability of POD method in predicting different thermal events, randomly generated transient power distributions are assumed for the chip and its individual function blocks. The results are validated against a full-filed FE model developed in a commercially available finite element analysis (FEA) software tool [10]. For more details on this study please refer to recent publications by the authors [11, 12].

METHODOLOGY

The developed hybrid scheme integrates the implementation of POD and progressive zoom-in approach:

POD Method: POD is a robust and computationally efficient method that captures the complexity of a high-dimensional physical system and provides low-dimensional yet accurate description of it by using a reduced number of degrees of freedom [13]. POD technique expands a set of data on empirically determined basis functions, also known as modes, for modal decomposition such that the least square error between the true solution and the truncated representation of the POD model in minimized. This technique numerically predicts the temperature distribution within a system more computationally efficiently than any full-field FE or FV (finite volume) simulations. A comprehensive study on various applications of POD is provided by Holmes *et al.* [14]. In summary, there are four main steps in developing any POD model: The first step is to generate the observation data set which can be obtained either experimentally or numerically (this study). The second step is to calculate the basis functions a.k.a POD modes. Modes are only functions of space. The third step is to calculate the POD coefficients (functions of time). The fourth and final step is to construct the temperature field based on the POD modes and coefficients from the expansion:

$$T(x,y,z,t) = T_0(x,y,z) + \sum_{i=1}^{m} b_i(t)\varphi_i(x,y,z) \quad (1)$$

where T_0 is the time average of temperature (i.e., the mean vector of the observation matrix), $\phi i(x, y, z)$ is the i-th POD mode, and $bi(t)$ is the i-th POD coefficient. Thorough derivation of a 2-D POD based reduced order diffusion model is provided in [9]. The 3-D formulation of POD method for conduction heat transfer is given in [11].

Progressive Zoom-in Approach: Progressive zoom-in is another multi-scale modelling technique that has been previously developed and can be used for transient thermal analysis in IC devices [15, 16]. Following a similar procedure described in [7],various levels of thermal behaviour in a system from package to chip, sub-chip, and ultimately transistor level can be integrated. This is done by passing down the acquired thermal knowledge of the system from each level to the following one through effective boundary conditions. By combining POD with progressive zoom-in approach, the computational efficiency of the hybrid model in covering several orders of magnitude in length and time scale is further improved. The overall hybrid approach for this work is shown in the flowchart of Figure 1 and is outlined below:

First, the entire package including chip, substrate, mold compound, and solder bumps is numerically modelled based on total chip power, boundary conditions, and initial conditions. At this level of simulation, chip is modelled as a solid block with effective material and thermal properties. No knowledge of chip internal features is required at this stage. Once the transient temperature distribution at package level is determined, POD model of the package is developed based on the chip power profile as previously explained. The POD model is able to predict dynamic temperature distribution for different power maps and types of power sources, without developing any further full-field finite element models [9]. This can considerably decrease computational cost and potentially be used to prescribe a criterion for the optimal distribution of the current density in the device. In the next step, a combination of heat flux and temperature on the surrounding walls of chip is extracted and applied in the form of dynamically changing boundary conditions for the chip level simulation. At this level, the chip is no longer treated as a solid block and is divided into subdomains called function blocks. Each block represents a component with unique functionality on the chip and consists of three sub-layers: 1. Silicon layer, 2. Transistor layer, and 3. Interconnect/Dielectric multilayer. The

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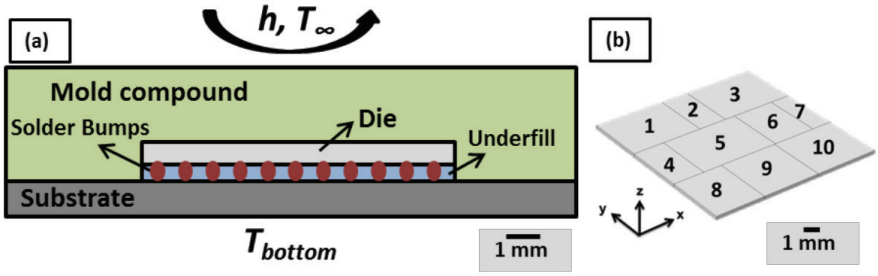

Figure 2: Simplified schematic of (a) FCBGA package used in this study for package level modeling and (b) the enclosed die with function blocks for chip level modeling.

transient thermal solution at the chip level is then determined by assigning the block specific power profiles, thermal and material properties. Based on the desired spatial resolution, this approach can be continued to sub-chip level domains. In this article, the results of two levels (package and chip) is provided.

RESULTS AND DISCUSSION

As described in the Methodology section, the first step is to determine the transient thermal profile for the entire package without chip internal details. A simplified schematic of the FCBGA package used in this work is shown in *Figure 2 (a)*. References [17] and [18] are used as a guideline for dimensions and material selection for the package. The effective material and thermal properties of each component of the package is calculated and in-plane and through-plane thermal conductivity values of the underfill/solder bumps are also determined [11]. This package is used for low power portable systems where compact form factor prohibits the use of heat sinks and forced cooling. Therefore, natural convection boundary condition with a heat transfer coefficient of h = 15 W/m2K (typical range for air [7]) was applied to the top surface and a constant temperature boundary condition is assumed at the bottom surface. Total transient chip power is assumed to have the form Q= 3 sin 2πt + 3 (W) and is applied for 0.5 s which represent a modulating power input to the system. This power profile is chosen only to develop the hybrid scheme. Once the model is complete, temperature distribution corresponding to more realistic power profiles can be determined at a much lower computational cost. A full-field FE model of the package is then developed in consisting of 75,919 elements, of which 343 are for the chip. The convergence of the FE model is verified with respect to the solver type, time step, and time integration method and the proper grid size is determined through mesh independence analysis. The FE temperature profile in the package after 0.5 s is shown in *Figure 3 (a)*. *Figure 3 (b)* demonstrates the 2D spatial distribution of temperature inside the package along the A-A cross section.

Once the transient temperature profile is determined, a POD model is developed at the package level using the procedure described in the previous section. Twenty six observations of the transient thermal solution are taken from the package level FE model. These observations correspond to the temperature solutions obtained at different time instants during the 0.5 s simulation time. As shown by Barabadi et al. [9], for any linear system, POD method can predict transient thermal solution regardless of the temporal or spatial dependence of the applied heat source. This feature can be used to predict temperature distributions for arbitrary heat inputs, by using a smaller sample set of applied heat sources and power maps and will result in significantly lower computational time. To further verify this feature, a POD model is developed based on the original power source (Q= 3 sin 2πt + 3 (W)) for 0.5 s and applied to predict the temperature profile for a randomly varying transient power distribution between 0-18 W for 1 s. The new power profile differs from the previous power input in duration, magnitude, and temporal dependency. POD basis functions (POD modes) are calculated based on the observation data set. To have a fast but reliable reduced order model, only four modes are kept in this study. This is chosen such that the cumulative correlation energy, Em [19] of the system is greater than 99.9%. The corresponding POD coefficients are then calculated as functions of time using the method of Galerkin Projection [9]. Finally, the reduced order transient temperature profile can be determined using Eq. (1).

Figure 4 (a) exhibits the three dimensional temperature profile of the package using the POD model 1 s after the power profile is applied. The domain is sliced in XZ plane along the A-A cross section shown in *Figure 4 (b)*. The right-most slice goes through the center of the chip. To validate the model, a full-field FE model is developed in in the FE software with the same grid size, element, and simulation time step used in POD model (results shown in *Figure 4 (c)*). The POD model closely predicts the transient thermal behavior of the system even for projected time outside of the original time domain when t >0.5 s. The mean absolute error between the POD and FE model is 7.2 % over the entire space and time domain. The computation

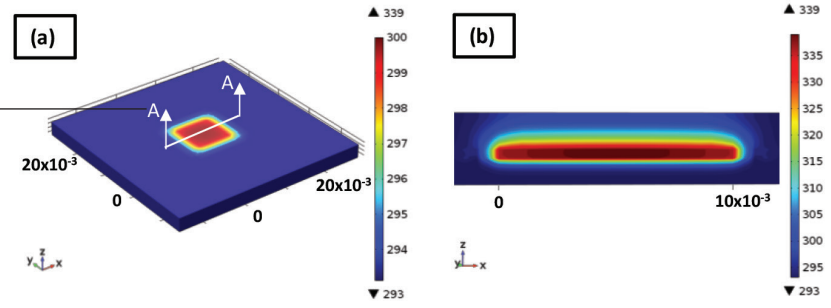

Figure 3: . FE temperature profile after 0.5 s for (a) FCBGA package and (b) the A-A cross section (dimensions in m, temperature in K).

time required for FE simulation is approximately 30 to 100 times higher than that of POD (23.7 min vs. 40 s respectively). The first POD simulation run-time is 40 s. Any additional POD simulations with different power profiles take 15 s each.

Once the transient thermal solution is obtained at the package level for 1 s, the next step in the hybrid scheme is to transfer the solution to the chip with the higher spatial resolution in the form of boundary conditions. A combination of temperature and heat flux is dynamically transferred down every 0.1 s as boundary conditions on top and bottom surfaces of the chip. Due to high aspect ratio of the chip, side walls are assumed to be adiabatic. The thermal solution is then linearly interpolated on each surface of the chip with much higher spatial resolution (268,033 elements in the chip at this level versus 343 elements at the package level).

For chip level modeling, the die is no longer assumed to be a solid block. It is now divided into 10 subdomains called function blocks *(figure 2 (b))*, which represent various components on the chip with different functionalities. Each block consists of three sublayers: top silicon layer (0.249 mm thick), transistor layer (5 μm thick), and the interconnect/dielectric multilayer. The effective properties of the functional blocks are calculated based on a combination of directional volume and surface -averaging methods. The in-plane and through-plane thermal conductivity of each function block is determined by constructing the corresponding equivalent thermal resistance network. At this stage, the spatial resolution of the model is limited to the sublayers of the blocks [11]. A dynamic power grid also needs to be assigned to each individual function block to its transistor sublayer where the majority of the heat is generated. Therefore, ten random transient power profiles are generated separately and assigned to each block such that their sum equals the total chip power used for package level modeling.

Once the power profiles are allocated to each function block, an FE transient thermal model can be developed using the calculated thermal and material properties as the final step of the hybrid approach. The FE model consists of 268,033 elements and the computational time to run the transient simulation for 1 s is approximately 26 min. *Figure 5 (a)* shows 2D contours of temperature profile at various times (0, 0.1, 0.5, and 0.95 s) on top of the transistor layer where maximum temperature occurs. *Figure 5 (b)* displays the temporal distribution of temperature at two different locations on the chip (position shown on the inset plot). In general, the procedure described in this article can be repeatedly applied, until the desired resolution on the chip is achieved.

SUMMARY AND CONCLUSION

An efficient and accurate multi-scale transient thermal model, using a hybrid scheme, was developed with the ability of modeling several decades of length and time scale, at orders of magnitude lower computational cost while maintaining

satisfactory accuracy. Utilizing the proposed model, the computational time is reduced by 30-100 times at every step of zooming into the geometry. The proposed approach is not limited to the package, chip, and function block levels and can be scaled down to "transistor level" while taking advantage of POD method to avoid any further full field simulations. One potential application of this method is during the design stage in IC industry. The multi-scale transient model can be developed for a specific chip structure that uses output signals of temperature sensors embedded on the chip and package as the original observations. This model can be incorporated into a closed loop on-chip control system to predict and potentially avoid the possible locations of hot-spots.

ACKNOWLEDGMENTS

The research is partially funded by Semiconductor Research Corporation (SRC) under Task 1883.001 and Design-to-Silicon division of Mentor Graphics Corporation.

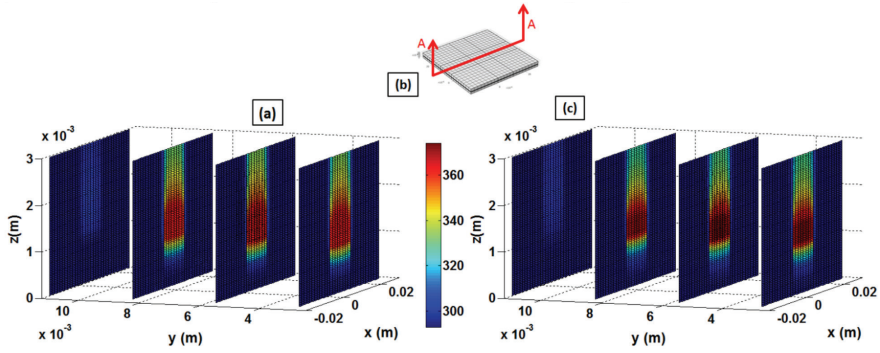

Figure 4: Temperature profile inside the package at 1 s extracted from the POD model (a) and FE simulation (c). The domain is sliced vertically along XZ plane. The right-most slice is the A-A cross section (b) (adapted from [11]).

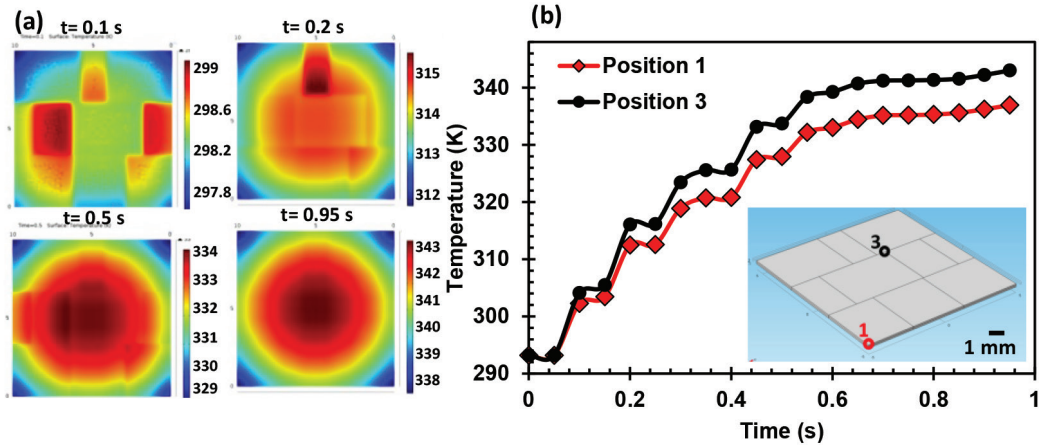

Figure 5: (a) Spatial distribution of temperature profile at chip level on top of the transistor layer after 0, 0.1, 0.5, and 0.95 s, (b) temporal distribution of temperature at two locations on the chip.

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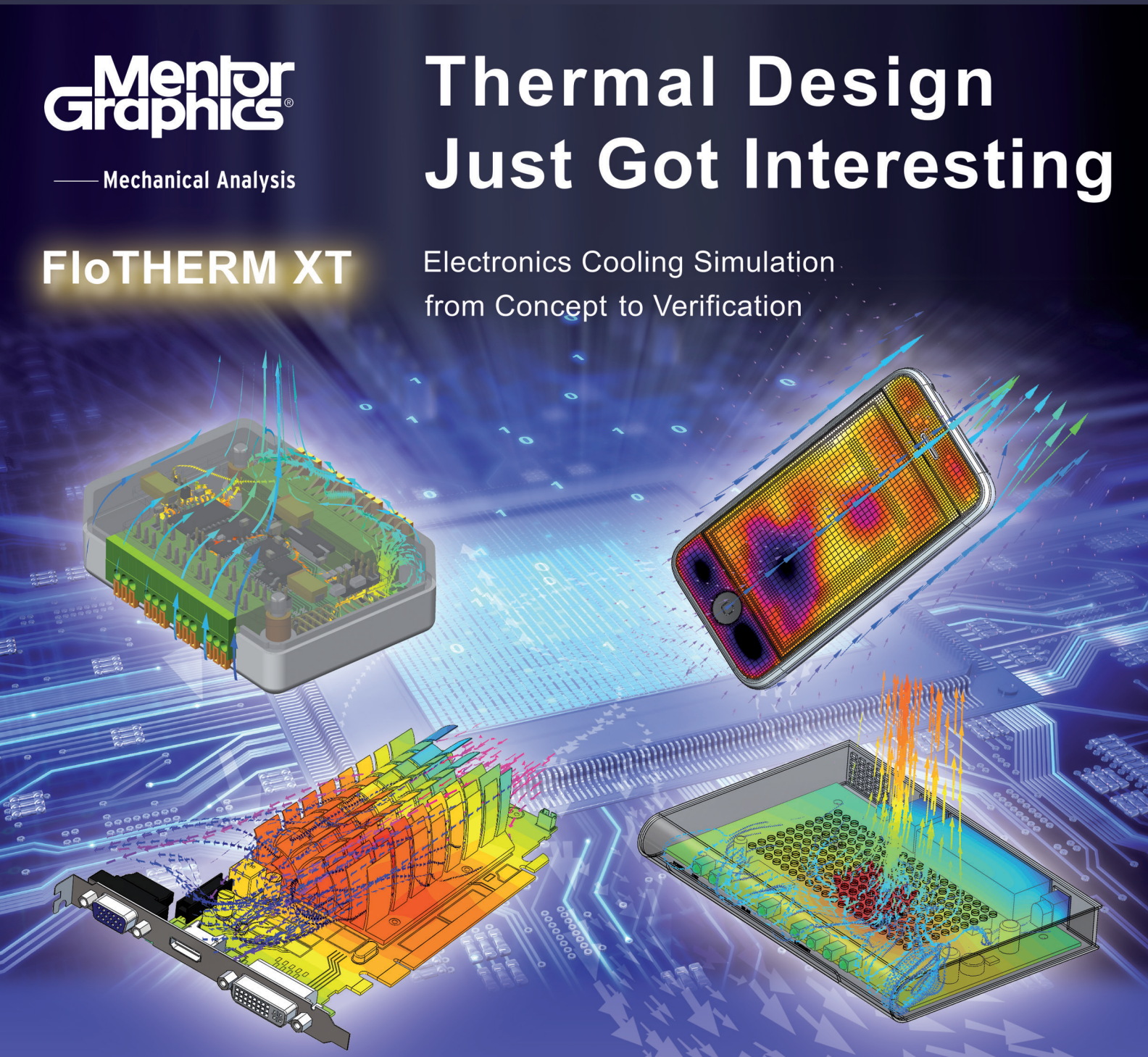
Mechanical Analysis

Thermal Design Just Got Interesting

FloTHERM XT

Electronics Cooling Simulation
from Concept to Verification



FloTHERM XT, the industry's first integrated MCAD – EDA electronics cooling simulation solution, to optimize designs from the early concept stage through to the verification and prototyping stages faster than ever before:

- Electronics cooling simulation solution for **large, complex electronics system design**
- CAD-centric interface and geometry engine as well as direct interfaces to MCAD and EDA software offer **immediate productivity** and short learning curve
- Full geometric and non-geometric SmartParts and Libraries enable **fast/accurate model creation**

Learn how FloTHERM XT can help design better electronics faster – download Step Change in Electronics Thermal Design: Incorporating EDA & MDA Design Flows

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Alpha's Next Generation Heat Sink

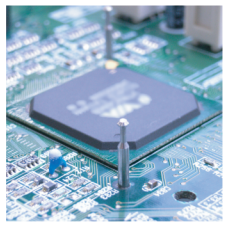
ALPHA

Custom or off-the-shelf.
Simple to complex.
Prototype to mass production.

QSZ Clip

Heat sinks are mounted directly to the PCB, but only take up a minimum of board real estate. Attachment force and shock loads are transmitted to the PCB instead of the chip and solder balls.

Minimum PCB Area



Pins only require 1.8mm diameter holes in the PCB.

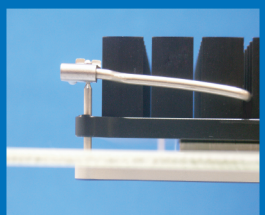
Anchor Pin
Multiple pin lengths are available for thicker/thinner PCBs

Advantages

Flexible Design

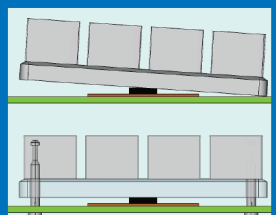
Custom clip/anchor pin spacing is compatible with standard heat sinks.

Mounting Security



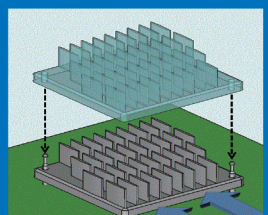
Direct attachment to the PCB is reliable and robust.

Installation-Guide



Internal pins minimize heat sink tilting. Excellent option for bare die packages!

Location-Guide



Inside heat sink footprint, pins set location and orientation.

Easy-Install

Press and hook to install. Easy!

Visit Alpha's WEB SITE !

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Original Cooling Solution
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Reduce size, weight up to 90%!!

Product can meet IP68 & GR487 Rated

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