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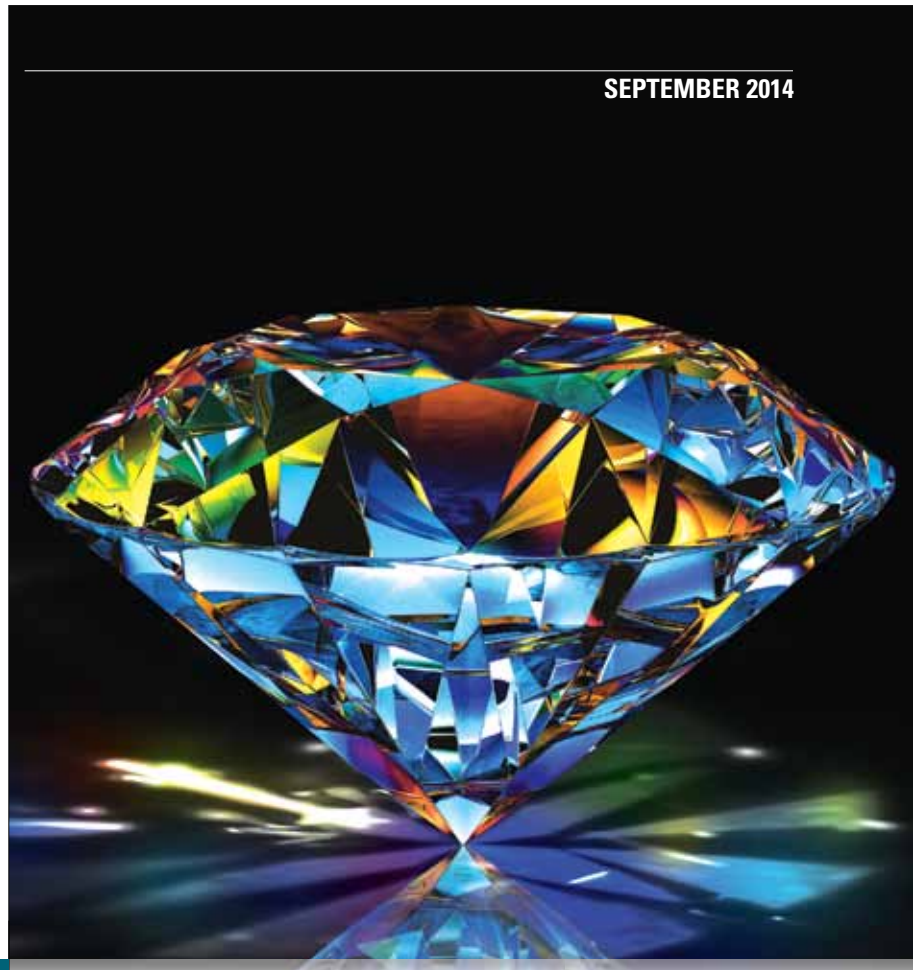

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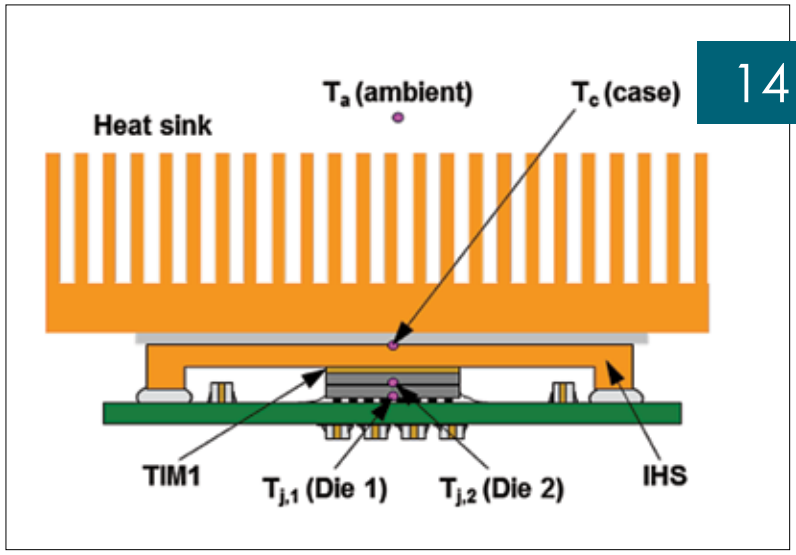

Editorial

The Need for Electronics Thermal Design Practices to Embrace Sustainability

Peter Rodgers, Editor-in-Chief, September 2014

GLOBAL ENERGY DEMAND IS PROJECTED TO INCREASE by 36% from 2010 to 2030, driven by population and economic growth in developing nations. This demand growth, combined with the depletion of fossil energy resources and the consequent escalation in energy prices, as well as environmental and energy security concerns, have motivated increased attention to sustainability. Despite progress in renewable energy conversion, the latest global economic recession has however prompted nations to refocus on conventional energy sources (e.g., fossil), albeit in a more sustainable way than in the past.

In relation to a previous 2008 editorial titled "en Route to a Greener Thermal Technology" [1], the question was posed "What can thermal engineers do to facilitate this change?" Suggestions included (i) adopting a holistic view of energy consumption, so that we all understand the true energy costs associated with performing tasks demanded by modern life, and (ii) contribute to the development of electronics-based technologies that are energy efficient, not only at the device level, but also at the system and societal level. Both points are touched upon in this article, to evaluate current progress in these areas.

Before doing so, let's consider two simple statistics regarding present days' magnitude of electronics energy usage:

- Since 2010, the electricity consumption of the global data center industry has risen from 1.3% to approximately 3% in 2014, with almost half of this power used for cooling the electronics.
- When accounting for wireless connections, data usage and battery charging, an average iPhone consumes 361 kWh each year, which exceeds the power consumption of a medium-sized, energy-efficient refrigerator.

To date, thermal design optimization has rarely been driven by energy outcomes, but rather by tradeoff between product electrical, thermal-hydraulic performance and non-holistic economic figures. This is in spite of well-known energy conservation metrics developed for electronics thermal management over the last two decades. With the objectives to reduce the material and energy consumption rates associated with the cooling of microelectronic equipment, design optimization methodologies focusing on least-energy, entropy generation minimization, and exergy efficiency have long been proposed. Such metrics permit the cost and environmental impact associated with energy consumption to be evaluated, and are widely used in energy-intensive industries (e.g., cement, steel, chemical, petrochemical). In those sectors, these metrics have led to the adoption of waste heat recovery technologies, which have resulted in substantial economic and environmental gains.

Unfortunately, the potential of these design methodologies is hardly exploited in today's electronics thermal design environments, with the recent exception of data centers. The extension of these design strategies to other electronic applications now needs to be considered. Technologies for recovery of low-grade heat are emerging, including:

- Conventional and nanocomposite thermoelectric devices for electrical power generation
- Phase change materials for energy storage
- Chip-level combined heat and power (CHP)
- Semiconducting materials for conversion of heat into electron-spinning energy

Sustainability will play an increasingly important role in the thermal optimization of electronic systems in the future. To accelerate the "en Route to a Greener Thermal Technology," ultimately new regulations will require to be established that will place greater constraints on the consumption of energy by electronic systems.

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Cooling Matters

News in thermal management technologies

CONTROLLING THERMAL CONDUCTIVITY TO IMPROVE ENERGY STORAGE

6/4/2014 - Researchers at the University of Illinois at Urbana-Champaign have experimentally shown for the first time that the thermal conductivity of lithium cobalt oxide (LixCoO2), a material used in the cathodes of lithium-ion batteries, can be reversibly electrochemically modulated over a significant range.

The new research on LixCoO2 represents "the first experimental demonstration of the electrochemical modulation of the thermal conductivity of a material, and, in fact, the only demonstration of large variable and reversible thermal conductivities in any material by any approach, other than very high pressure experiments."

During the experiment, researchers deposited a LixCoO2 film directly on a metal coated electrode, then immersed it in a common electrolyte. Time-domain thermoreflectance (TDTR) was used to measure the thermal conductivity of the lithium cobalt oxide thin film as a function of lithiation.

The study's findings are expected to significantly impact the field of electrochemical energy storage.

Source: University of Illinois

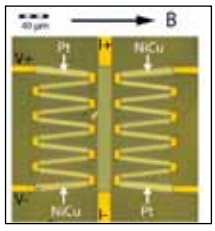
SPIN WAVES TRANSPORT HEAT IN INSULATING MATERIALS

7/8/2014 - An international team of researchers has designed a nanoscale cooling element that utilizes fundamental subatomic properties to transport heat in electrical insulators.

The technology relies on the intrinsic spin of an electron that corresponds with its magnetic movement to move heat away from a component. While physicists have used spin for cooling purposes before, the The study, "Observation of the Spin Peltier Effect for Magnetic Insulators," new research marks the first time researchers have done so in insulating materials.

The latest study builds upon previous research demonstrating that directing an electric current through a magnetic layer causes the spins of the electrons in the current to all point in the same direction parallel to the magnetization.

This spin current can be used to influence the temperature at the boundary between the surfaces of a nonmagnetic metal and a magnetic metal.



Source: Physical Review Letters

SUPERCONDUCTING REFRIGERATOR COOLS VIA TUNNELING CASCADE

6/26/2014 - Researchers from Italy and France have proposed a new design for a superconducting refrigerator that uses a series of steps to more effectively cool objects down to temperatures near absolute zero.

The design for a multistage superconducting refrigerator, or "cascade cooler," from M. Camarasa-Gomez et al. adds an additional tunnel junction on each side (S2IS1INIS1IS2) of the SINIS design. In this case, when a voltage bias is applied to the S2, the hot quasiparticles tunnel from the normal metal to the S1 superconductors and then to the S2 superconductors, removing additional heat compared to the SINIS design. This multistage operation allows the refrigerator to easily cool a normal metal from a bath temperature of 0.5 K to 100 mK.

"[This is] a novel kind of electronic cooler based on hybrid superconducting tunnel junctions. A cascade geometry allows to cool a first superconducting stage, which is used as a local thermal bath in a second stage," they said.

The cascade cooling method could be easily implemented in a practical device, the researchers added, using a set of two additional junctions. The company hopes this cascading magnet technique could replace the traditional compressor and chemical refrigerant used in commercial refrigerators by the end of the decade.

Source: Applied Physics Letters

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- *How do you design protection from HEMP and IEMI to keep data centers safe?*
- *What is the role of existing lightning protection for protection from HEMP and IEMI?*
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Virtual Prototyping

Peter Rodgers
The Petroleum Institute

THE FOCUS of this article is on the use of computational fluid dynamics (CFD) as a virtual prototyping tool for electronics thermal design. However, first of all, given that this is my first thermal facts & fairy tales article, I decided to adopt the following quote as point of reference:

"In a utilitarian age, of all other times, it is a matter of grave importance that fairy tales should be respected." Charles Dickens (Frauds on the Fairies, 1853)

BACKGROUND

Since the 1990s, CFD has been widely adopted in the electronics industry for the thermal design of electronic products and is progressively marching on to be considered by some to be a *de facto* virtual prototyping tool. Its advantages in terms of product improvements and enhanced productivity of design analysis are undisputed [1,2]. However, although not unsurprisingly reported, the industry has also found that incorrect product design decisions can be made as a result of inaccurate CFD predictions. The potential pitfalls of CFD analysis for electronics thermal design, in absence of supporting experimental characterization, are well documented [3,4]. To broaden the horizon of discussion on the capability of CFD analysis outside the field of electronics cooling, this article discusses the world of Formula One (F1) motorsport and NASA.

FORMULA ONE AERODYNAMICS

Race pole position in F1 is often determined by hundredths of a second in qualifying. Consequently, car aerodynamics have become key to success, with budgets of tens of millions of dollars allocated for research and development each year [5]. To achieve optimum performance, the aerodynamic designer has two primary concerns: (i) the creation of downforce to promote car tire adhesion onto the track and improve cornering forces, and (ii) the reduction of drag generated by car body-induced turbulence.

To maximize aerodynamic performance, CFD is applied in parallel with wind tunnel characterization of scaled mock-up prototypes in wind tunnel environments to both develop and validate the design. However, an interesting departure to this strategy was adopted by one team for the 2010 and 2011 FIA F1 World Championships. Their car's aerodynamics design was undertaken primarily by simulation (i.e. CFD), bypassing experimentation on scaled prototypes. This CFD-only design approach has found previous success in American sports car racing, but at this point was unproven in F1, where aerodynamics are more complex. During the car's presentation at the start of the 2010 season [6], the team acknowledged that *"there is scepticism about our approach," and said in relation to CFD, "We fully expect to encounter issues along the way. CFD (computational fluid dynamics) is an approximation, as is scale-model (wind-tunnel) testing. It is only when you hit the track that you can really appreciate the effect of factors that are tricky to model with any technology."*

Although the car was found to lack aerodynamic performance throughout the 2010 season, with engine and driver factored for, the subsequent model that competed at the start of the 2011 F1 World Championship was again designed primarily by simulation [7], with some wind tunnel testing in late 2010 to try to resolve problems with the earlier design [8]. At the 2011 car's launch, the continued use of CFD as the primary design strategy was defended: *"..those who don't believe in (the system) are members of the flat-earth society. It is the future of motor racing."* [7]. However the car again faced performance difficulties, and by mid-season the team acknowledged, *"What has been disappointing has been our pace. It's aero efficiency. We're nowhere with it."* [8]. It was then also announced that the team would consider, budget permitting, a future wind tunnel testing programme. For the 2012 F1 World Championship, the car aerodynamics were actually developed through a combination of CFD and wind tunnel testing [9].

The CFD-driven design strategy, which was ultimately unsuccessful, had been motivated by the escalating, unsustainable costs of aerodynamics design in full-scale wind tunnels and on-track testing. This was recognized by the F1 team organization (FOTA) in 2009, with the introduction of a subsequent resource restriction agreement (RRA) to help constrain overall team expenditures. For example, in terms of aerodynamics, limitations were introduced on wind tunnel testing (in terms of wind-on time), as well as CFD processing (measured in

teraflops) due to the cost of high performance computing clusters, but with limited success [10]. Considerably greater restrictions were imposed in the 2014 FIA sporting regulations than in the previous RRA by the sport's governing body (FIA), with aerodynamic testing effectively reduced to nearly one-third of that allowed under the previous RRA [11]. Under the new FIA 2014 regulations, wind tunnel testing and CFD analysis are capped by a formula of 30 units (a unit being an hour per week of wind-on time, or a teraflop of compute capacity used for the solving of CFD cases) based on an eight-week aerodynamic testing period. For example, a team can use up to 30 hours per week of wind-on time, with no CFD processing, or 30 teraflop of CFD and no wind tunnel, or a combination of both. In addition, other restrictions were adopted on the number of wind tunnel runs (80) and operating time (60 hours) per week [11].

To help illustrate the implementation of the new regulations in the F1 aerodynamic design process, the following analogies were given by Sauber F1 team [12], between wind tunnel and hairdryer usage, and between CFD processing and computer usage: *"You may be in the bathroom for 60 hours per week, but you may only switch on the hairdryer 80 times and not for longer than 30 hours in total. If your hairdryer runs 30 hours, you are not allowed to use your computer at all; less running time of your hairdryer will allow you to use your computer, but in any case you can't spend more time than 30 hours per week in total with your hairdryer and computer combined."*

The introduction of the these restrictions is now leading to a greater emphasis on the use of CFD in F1 car aerodynamic development process, coupled with more efficient use of wind tunnel testing. However, not all F1 commentators agree that this is the best practice, given that the sport has often served as an innovator to the automotive industry. For example, concerns have arisen [13] that F1 may not be able to contribute to the rest of the CFD world in developing transient simulations, as future analysis maybe constrained to outdated teraflop-friendly steady-state science. Time will tell, but this story highlights the need for both optimization and effective use of CFD, combined with effective experimental characterizations. This strategy could be better implemented as part of an electronics cooling thermal design process.

NASA CFD VISION FOR 2030

It might be tempting to believe that NASA's goals for CFD analysis do not apply to electronics cooling, however a recent report [14] commissioned by NASA presents altogether a series of seven findings, a vision for CFD capabili-

ties required by 2030, and a set of six recommendations for achieving these capabilities. All findings are equally applicable to electronics cooling, particularly Findings 3 and 4:

- Finding 3: The use of CFD in the aerospace design process is severely limited by the inability to accurately and reliably predict turbulent flows with significant regions of separation. Advances in Reynolds-averaged Navier-Stokes (RANS) modeling alone are unlikely to overcome this deficiency, while the use of Large-eddy simulation (LES) methods will remain impractical for various important applications for the foreseeable future, barring any radical advances in algorithmic technology.
- Finding 4: Mesh generation and adaptivity continue to be significant bottlenecks in the CFD workflow, and very little government investment has been targeted in these areas.

Among the six recommendations given to achieve the NASA 2030 vision of CFD capabilities, of particular interest to electronics cooling is the following:

- Recommendation 4: NASA should lead efforts to develop and execute integrated experimental testing and computational validation campaigns.

SUMMARY

Considering the experiences documented in other industries, such as the above, hopefully the fairy tale that the thermal design of electronics can somehow be achieved through virtual prototyping alone can be laid to rest for the foreseeable future.

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An Inexpensive Multi-channel AC Heater Control System

Lucien François Dorthe and Paul Kolodner
Bell Laboratories, Alcatel-Lucent, Inc.

INTRODUCTION

A COMMONLY-encountered problem in the experimental modeling of thermal-management solutions is the need to independently power many sources of heat. A typical telecomm circuit pack, for example, may contain a dozen or more integrated circuits (ICs) or optical components, and it is often desired to test cooling solutions by replacing each IC with an independently-computer-controlled resistive heater. This could be accomplished using multiple DC power supplies, but this approach is overly precise, bulky, and, worst of all, expensive—at least several hundred dollars per channel. This technical brief describes a much more economical system, using triac-based AC lamp dimmer modules originally intended for hobby or household use. Controlled by an inexpensive processor board, this approach costs less than $100 per channel.

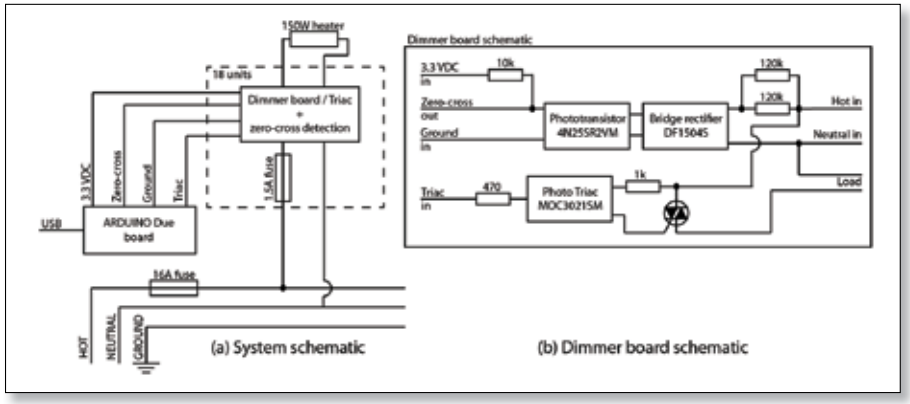

FIGURE 1: Multi-channel AC heater control system.

CIRCUIT DIAGRAM

The standard circuit used for dimming AC lighting systems uses a triac to control the connection of the load to the AC power source. The triac turns off the drive current after an adjustable time delay with respect to each zero-crossing of the AC waveform, and the user increases or decreases this delay to increase or reduce the time-averaged power. A small-format, single-channel dimmer module that performs this function is available for $40 from a hobbyist website [1]. These circuits can switch 10 A, or 1.2 kW per channel at 120 Vac, and they can be modified for operation at higher currents. The system described herein uses 18 of these circuits, controlled by an Arduino Due processor module [2]. Arduino is an inexpensive, open-source electronics platform targeted towards hobbyists and educators (see [3] for complete information). Arduino processor modules contain a small microprocessor, programmable input/output pins, and USB ports, and they run code written in a simple, C-like language. The Arduino

Lucien Dorthe obtained his master's degree in mechanical engineering at the Swiss Federal Institute of Technology of Lausanne in March 2014. His main fields of study are thermodynamics, energetics and heat transfer. He worked on several projects (modeling, simulation and experimental testing) to develop new methods like pump cycles or thermosyphons to cool electronic components using two-phase fluids.

Paul Kolodner recently retired from Bell Laboratories after a 34-year career. He was most recently a Distinguished Member of Technical Staff in the Thermal Management Group in the IP Routing Laboratory. He has performed experimental research on a variety of problems, including the use of rare-earth-chelate films for high-resolution fluorescent thermal imaging, convective pattern formation, protein photobiology, precision microlens array characterization, applications of superhydrophobic surfaces, and thermal management of electronics. He has written or co-authored approximately 130 published papers and 40 issued or pending patents.

Due module, which costs about $50, is based on a 32-bit microcontroller running at a clock speed of 84 MHz. The module has 54 digital I/O pins, which would allow for control of up to 53 heater channels. The processor has 512 kB of flash memory for control code and is programmed by a computer running LabVIEW [4], via serial communication over the USB port.

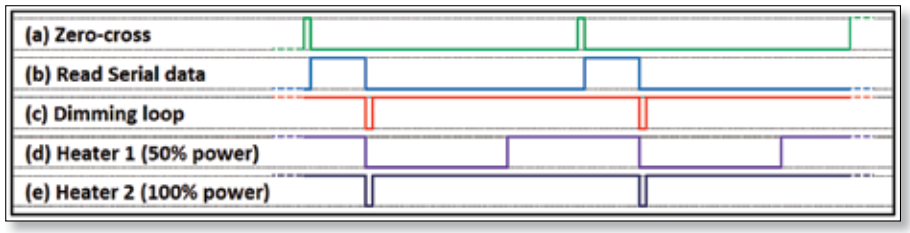

FIGURE 2: Timing diagram.

As shown in Figure 1(a), the Arduino Due processor accepts a "zero-cross" input logic signal from one of the 18 dimmer modules (shown in Figure 1(b)); this signal consists of a train of short positive pulses that are synchronous with the sign changes of the AC waveform. Each of the 18 modules is assigned a separate "Triac" output pin on the Arduino board, and the program brings this signal high to connect that heater for the selected fraction of the AC waveform. The whole system is powered through the USB port.

The components are mounted inside a grounded aluminum electronics enclosure, which is mounted adjacent to the test fixture into which the 18 heaters have been clamped. This proximity allows the heater cables to be short and neat, reducing the risk of accidental disconnection. The heater cables are plugged into the control-circuit box using individual high-current, male electrical connectors to eliminate any shock hazard.

CODE AND TIMING ISSUES

The control program is transferred to the Arduino board over the USB port. This program is included as an Appendix in the online version of this article and can also be requested by email from either of the authors. The code defines the input and output pins on the processor board and then runs several loops continuously, each of which is triggered once per half-cycle by the "zero-cross" signal. The "read loop" reads a string containing the 18 control parameters from the USB port. The "dimming loop" checks the on/off state of the 18 triacs and alters each at the time corresponding to the input parameter for that channel. A "delay loop" corrects the timing synchronization and allows the input string to be read, as detailed below.

Several timing and resolution issues affect the details of the code:

1. The zero-cross signal pulses precede the zero crossings by about 2.3 msec. Thus, the "delay loop" postpones the start of the "dimming loop" by this amount, relative to the zero-crossing pulses.
2. The serial input buffer of the Arduino processor is limited to 64 bytes. Therefore, the 18 power levels are encoded by a 56-byte string of 2-digit integers between 0 (full on) and 64 (full off), separated by commas and preceded by a start character ("s"). The time resolution step is 1/64th of a half-cycle, or 130 μsec, and the integers in the string represent the number of time steps in the "dimming loop" that elapse before each heater is turned on. At the fastest baud rate (112500 bit/sec), this string takes a bit less than 2.3 msec to read. This input is transferred once per half-cycle by the "read loop." The transfer takes place during the "delay loop."
3. The "dimming loop" checks the on/off state of each of the 18 triacs once every 130 μsec and alters each according to the input string for that channel. Due to the limited speed of the Arduino Due processor, it was not possible to increase the timing resolution to 1/128th of a half-cycle in this implementation.

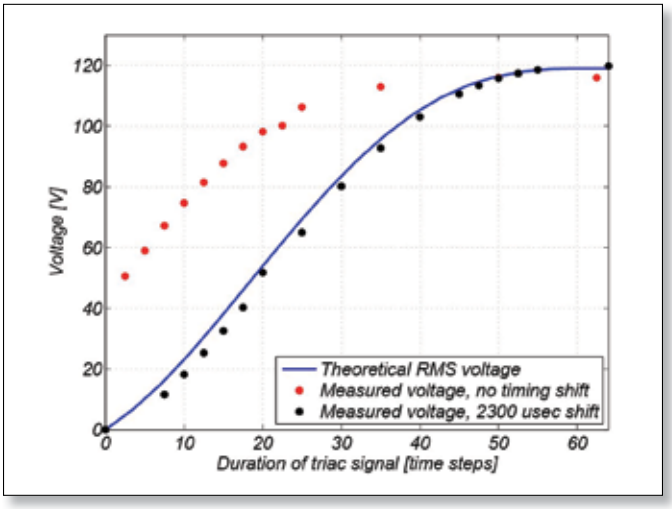

FIGURE 3: Measured and theoretical RMS output voltages as a function of the duration of the triac signal, for one heater channel.

Figure 2 shows a diagram of the signal timing. The zero-cross signal (trace (a)) triggers the "read loop" (trace (b)), which allows 2.3 msec for reading the serial data and synchronizes the start of the "dimming loop" with the actual zero-crossing of the AC waveform. Trace (c) shows the period available for the individual heaters to be turned on and off. Traces (d) and (e) show two representative triac signals.

CONTROL CHARACTERISTICS

The control system was evaluated by measuring the AC output voltage of one channel with a true-RMS meter as the time delay was varied. A comparison between the measured

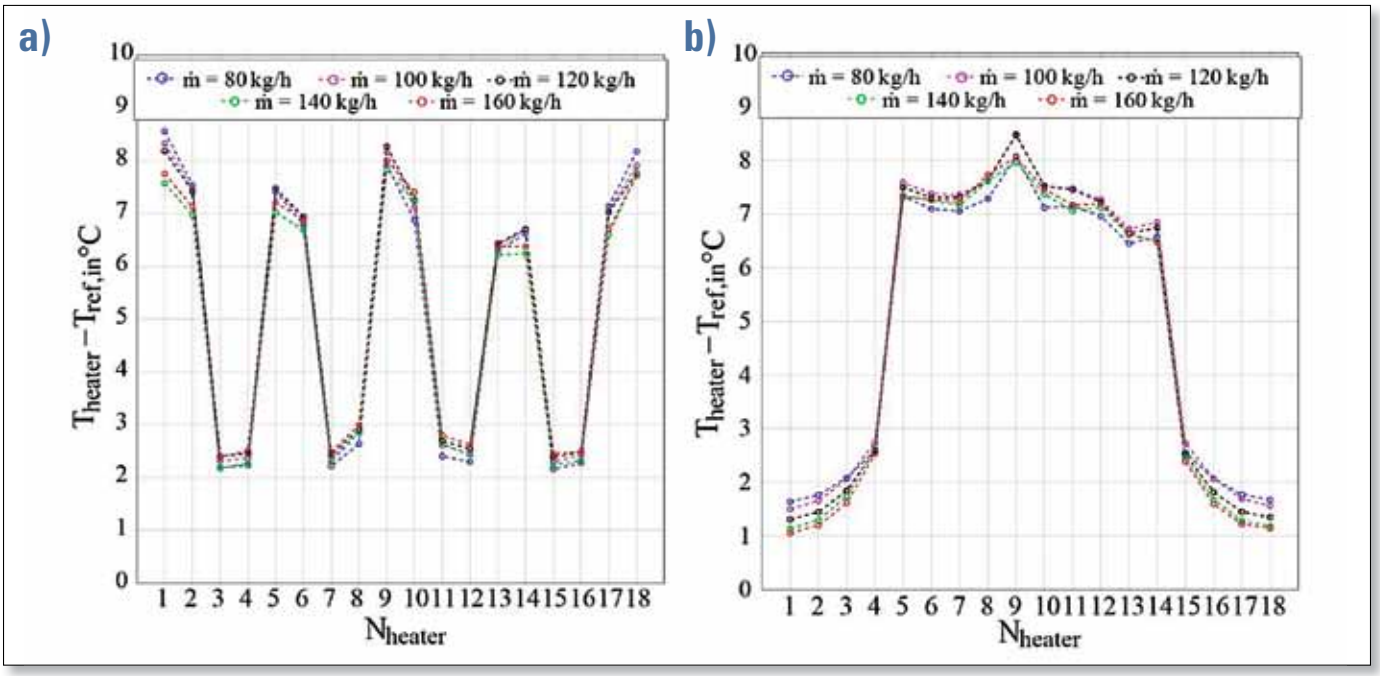

FIGURE 4: Measured spatial temperature profiles obtained with non-uniform heating using pumped refrigerant at different flow rates, ṁ.
a) Square-wave profile **b)** Rectangular profile

and theoretical RMS output voltages is presented in Figure 3. The blue curve shows the theoretical voltage, which is just the square root of the integral of a squared sine function. The red data points show the measured values with the length of the "delay loop" set to zero. The length of this delay was adjusted empirically to 2.3 msec in order to get the measured data points in black to overlap with the theoretical curve. The slight offset with respect to the theoretical curve indicates that this delay was set approximately 2 time steps too long.

THERMAL PERFORMANCE

The heater control system was used to test a segmented aluminum cold plate cooled by pumped R134A refrigerant. The vertically-oriented cold surface has dimensions 417.5 mm wide x 80.0 mm high. Its interior consists of 18 vertical channels of height 53 mm, arrayed horizontally and connected in parallel to upper and lower manifolds, so that refrigerant flows upward through the channels. The test heaters each consist of a square copper bar of height 50 mm and width/depth 20 mm, with a vertical axial hole of diameter 6.35 mm holding a 140-Ω cartridge heater. Each bar also has an embedded thermocouple. The heaters were clamped against the cold surface, and the entire system is heavily insulated.

Figure 4 shows the thermal response of the system to non-uniform heating at five different refrigerant flow rates (ṁ) for two different spatial heating profiles. The plotted quantity is the heater temperature (T_{heater}) relative to the input refrigerant temperature ($T_{ref,in}$). All data used sub-cooling $\Delta T_{sub} = 2$ °C and total heating power 1,000 W. Figure 4(a) shows the result for a square-wave heating profile with period 4; low-power heaters are off. In Figure 4(b), a rectangular profile was applied, with the center 10 heaters on and outer heaters off. The variations between the different curves suggest that (a) the power resolution in each channel is a few Watts, and (b) heater number 9 is running slightly hot, possibly because of a defect in its thermal interface. This performance has been more than adequate to allow the detailed characterization of this cold plate when operated as a gravity-driven thermosyphon.

CONCLUSIONS

The control system described in this paper represents a new and useful compromise between cost, precision and flexibility. It is hard to imagine a cheaper way to control many heaters. The resolution and precision of this system is a few percent and could be improved if required. And, as to flexibility, the present implementation could be expanded to a channel count of 53 before a new architecture would be required. Because of the 64-bit word length of the Arduino Due module, a more complicated read protocol would be needed to increase resolution and/or channel count. Operating at higher powers could be enabled by replacing the triacs on the dimmer control modules.

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Estimating the Thermal Interaction between Vertically Stacked Chips in a Multi-Chip Package

Je-Young Chang, Ashish Gupta
Intel Corporation

INTRODUCTION

3D INTEGRATION is considered a promising packaging technology option to increase transistor density by vertically integrating two or more dice with a dense high-speed interface with shorter interconnect length, enabling a smaller package form factor across a variety of market segments [1-2]. However, despite its promising electrical benefits, effective cooling of 3D stacked die packages remains a challenge [3-5], which could impact the long-term reliability of active devices in the package. In order to better understand and quantify the thermal response of 3D stacked die packages, accurate characterization of thermal behavior and establishment of appropriate thermal design rules for the feasibility of various integration options are essential.

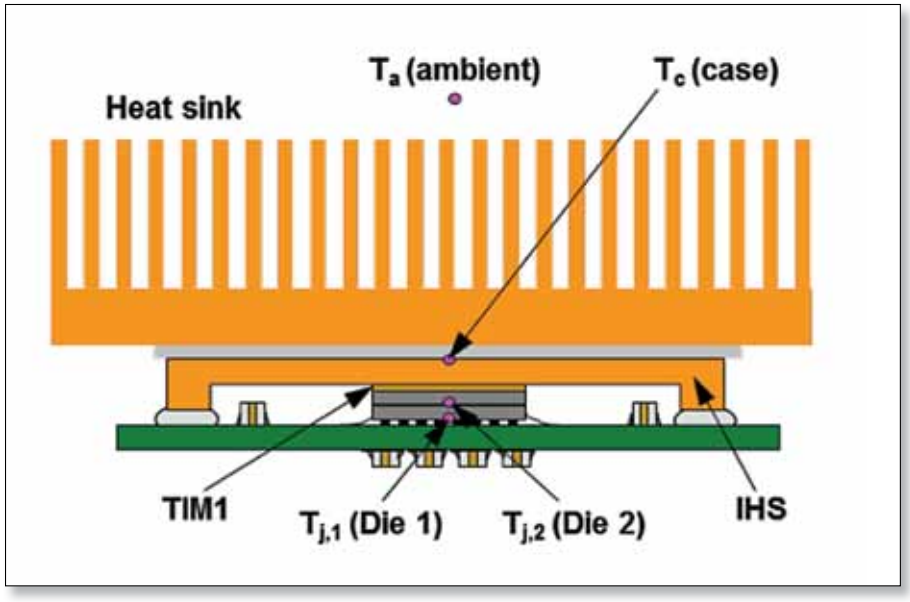

FIGURE 1: Schematic of speculative MCP with 3D die stack (Not drawn to scale).

In the previous article by the current authors [6], a thermal analysis methodology was presented for predicting cooling capabilities of Multi-Chip Package (MCP) architectures with multiple side-by-side dice. The thermal analysis methodology is based on the principle of linear superposition in conduction heat transfer to calculate the die junction temperatures at an arbitrary combination of powers applied to the dice under steady-state conditions [7-8]. In this article, the thermal analysis methodology is extended to predicting cooling capabilities of MCP architectures with 3D stacked dice.

Je-Young Chang received his B.S. and M.S. degrees from the Seoul National University in South Korea and his Ph.D. degree from University of Texas at Arlington, all in mechanical engineering. He worked at Penn State University for three years as a research associate before joining Intel in 2000. He has worked on many aspects of advanced cooling technologies, including two-phase immersion cooling, single/two-phase microchannel cooling, corrosion reliability of liquid cooling systems, heat pipes, TIMs, heat exchangers, etc. He has 19 issued/pending US patents, and more than 60 articles in archival journals, conference proceedings and Intel internal publications.

Ashish Gupta manages the Thermals/Fluids Core Competency Team in Intel's Assembly and Test Technology Development Group in Arizona. He holds a Ph.D. degree in Mechanical Engineering from Purdue University. His group is responsible for the R&D of advanced package thermal and cooling technologies, modeling methodologies and metrologies for Intel's current and future generations of processors for product segments during the discovery, definition, development and certification stages of technology maturity. The team's scope covers the entire gambit of Intel product segments across all market segments ranging from handheld devices and small form factor packages to higher power server products.

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ESTIMATION OF COOLING ENVELOPE OF MC WITH 3D DIE STACK

In Figure 1, a typical 3D package architecture is illustrated with the locations of temperature measurements. As shown in the figure, the package has two dice stacked under an integrated heat spreader (IHS), which is cooled by a heat sink.

For the above 3D MCP in Figure 1, the same equation in the previous article [6] can be used to express the junction temperature of any of the dice as a function of the power(s) applied to all of the dice:

$$\begin{bmatrix} T_{j,1} \\ T_{j,2} \end{bmatrix} = \begin{bmatrix} \Psi_{11} & \Psi_{12} \\ \Psi_{21} & \Psi_{21} \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \end{bmatrix} = \Psi_{ca} \cdot (P_1 + P_2) + T_a \quad \textbf{(1)}$$

where $T_{j,i}$ is the junction temperature of Die "i"; P_i is the power dissipation of Die "i"; Ψ matrix, also called the "influence" coefficient matrix, is the thermal resistance from the junction to the case; Ψ_{ca} (°C/W) is case-to-ambient thermal resistance; and T_a is the ambient temperature.

For the 3D MCP in Figure 1, the cooling envelope can be estimated using the same analysis methodology in the previous article [6]. For comparison purposes, a 2D planar MCP is also analyzed using the same power-maps and heat sink conditions. In 3D MCP, there is only one TIM1 interface (i.e., thermal interface material (TIM) between the die and IHS), over the die stack; however, additional thermal resistance at the die-to-die interface causes significant impact on the package cooling capability [3-5]. In the current analysis, considering the objective of this article, a thermally favorable die-to-die interface (i.e., a fully-populated thermal bump array at the die-to-die interface) is assumed for 3D MCP. Table 1 shows representative results from thermal simulations for two different cases of die power scenarios for each of the 3D and 2D MCPs.

For the above data of 3D MCP model, junction temperature differences from the reference point (e.g., $\Delta T_{j,i} = T_{j,i} - T_c$) are considered in actual calculations, while the downstream variables (i.e., Ψ_{ca} and T_a) are assumed constant. In this case, all the calculation results (i.e., $\Delta T_{j,i}$ and P_i values) can be summarized as:

$$\begin{bmatrix} 11.78 \\ 6.52 \end{bmatrix} = \begin{bmatrix} \Psi_{11} & \Psi_{12} \\ \Psi_{21} & \Psi_{22} \end{bmatrix} \cdot \begin{bmatrix} 60 \\ 20 \end{bmatrix} \text{ and } \begin{bmatrix} 17.67 \\ 9.34 \end{bmatrix} = \begin{bmatrix} \Psi_{11} & \Psi_{12} \\ \Psi_{21} & \Psi_{22} \end{bmatrix} \cdot \begin{bmatrix} 95 \\ 10 \end{bmatrix} \quad \textbf{(2)}$$

Equation (2) can be rearranged for each of $\Delta T_{j,1}$ and $\Delta T_{j,2}$ values, and "power input" matrix can be expressed as:

$$\begin{bmatrix} 11.78 \\ 17.67 \end{bmatrix} = \begin{bmatrix} 60 & 20 \\ 95 & 10 \end{bmatrix} \cdot \begin{bmatrix} \Psi_{11} \\ \Psi_{12} \end{bmatrix} \text{ and } \begin{bmatrix} 6.52 \\ 9.34 \end{bmatrix} = \begin{bmatrix} 60 & 20 \\ 95 & 10 \end{bmatrix} \cdot \begin{bmatrix} \Psi_{21} \\ \Psi_{22} \end{bmatrix} \quad \textbf{(3)}$$

For Equations (1) to (3), the values of Ψ matrix elements can be calculated from an inverse matrix solver, and the complete form of Equation (1) for the 3D MCP in Table 1 can be written as:

$$\begin{bmatrix} T_{j,1} \\ T_{j,2} \end{bmatrix} = \begin{bmatrix} 0.181 & -0.045 \\ -0.094 & 0.045 \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \end{bmatrix} + \Psi_{ca} (P_1 + P_2) + T_a \quad \textbf{(4)}$$

Using the same procedure, the complete form of Equation (1) for the 2D MCP in Table 1 can be derived as:

$$\begin{bmatrix} T_{j,1} \\ T_{j,2} \end{bmatrix} = \begin{bmatrix} 0.116 & -0.083 \\ -0.060 & 0.213 \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \end{bmatrix} + \Psi_{ca} (P_1 + P_2) + T_a \quad \textbf{(5)}$$

GRAPHICAL REPRESENTATION OF MCP COOLING ENVELOPES

For both Equations (4) and (5), there are two linear equations expressed in terms of P_1 and P_2, which represent cooling capabilities of Die 1 and Die 2 as defined by junction temperature limits and ambient temperature condition [6]. In Figures 2(a) and 2(b), cooling capabilities of 3D and 2D MCPs, respectively, in Table 1 are illustrated. In each figure, the solid lines represent the cooling capabilities of Die 1 and Die 2 with respect to junction temperature limits and ambient temperature condition, and the overlapped region (highlighted with gray color) represents thermal operation space of the MCP.

As shown in Figure 2(a), 3D MCP shows a strong thermal coupling between two dice due to close proximity in 3D stacked configuration, as indicated by the similarity in the slopes of the two junction temperature limiter lines. This can be clearly compared with the analysis results of 2D MCP in Figure 2(b), where the junction temperature limiter lines have very dissimilar slopes. In the extreme case, if there is no thermal cross talk between two dice, the junction temperature limiter lines should be perpendicular each other.

TABLE 1: EXAMPLE TEMPERATURE DATA FOR MCP ANALYSES (Ψ_{CA} = 0.24 °C/W IS ASSUMED)

	3D MCP Model		2D MCP Model	
	Case 1	Case 2	Case 3	Case 4
Die-1 power [W]	60	95	60	95
Die-2 power [W]	20	10	20	10
$\Delta T_{j,1} = T_{j,1} - T_c$ [°C]	11.78	17.67	5.29	10.17
$\Delta T_{j,1} = T_{j,2} - T_c$ [°C]	6.52	9.34	0.67	-3.55

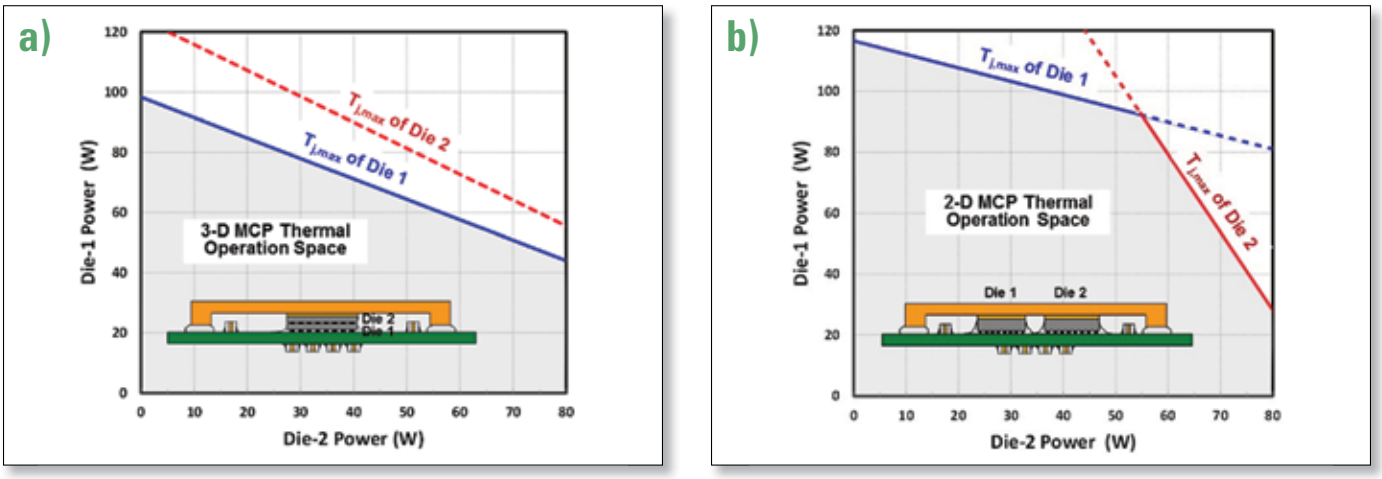

FIGURE 2: Cooling envelopes of speculative MCPs at steady-state conditions ($T_{j,max}$ = 95 °C for both dice, T_a = 54 °C, and Ψ_{ca} = 0.24 °C/W are assumed). **a)** 3D MCP, **b)** 2D planar MCP.

As shown in Figure 2(a), for a 3D MCP, junction temperature limiter of either die can determine the whole thermal operation space, thus if it is set at too low a value (e.g., 80 °C for memory die), the package cooling capability can be significantly impacted. In the current analyses, both dice are assumed to have the same junction temperature limit (95 °C). For a speculative 3D MCP in Figure 1, the bottom and top dice could be logic and memory chips, respectively. In this case, it is imperative that $T_{j,max}$ of memory die should be kept as close possible to $T_{j,max}$ of logic die to ensure thermal management of 3D package under control, as long as memory performance (e.g., memory refresh rate, leakage) and reliability requirements can be met.

The above graphical representations of the cooling envelopes of both 2D and 3D MCPs are useful to estimate thermal operation spaces for different design conditions, such as different junction temperature limits, ambient temperatures and heat sink designs. It should be noted that, for accurate estimation of thermal operation space, the Ψ matrix should be re-calculated, if there is any significant change in:

a. Design conditions, such as die dimensions, die locations, die-to-die spacing, die-to-die interface in 3D die stack, IHS dimensions, *etc.*
b. Material conductivities, such as thermal interface conductivity.
c. Die non-uniform heating power-maps.

Finally, as more and more dice are integrated into 3D packages, there will be more frequent examples of a combination of "side-by-side" and "vertically stacked" dices. Both analysis results of the previous [6] and current articles have demonstrated that the principle of linear superposition is applicable to any configuration of multiple dice in an MCP with conduction being the dominant heat transfer mechanism, and provide the first order approximation of the system.

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High Heat Flux, Single-Phase Microchannel and Minichannel Cooling with Water and Liquid Metal

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Rui Zhang received her B.S. from Shandong University in China in 2009, where she majored in energy and power engineering with an emphasis on the design and operation of heat exchangers and boilers in power plants. In 2011, she received her M.S. in mechanical engineering from Tufts University, Medford, Mass., where her research focused on optimization of thermoelectric module-heat sink assemblies for minimal power consumption for precision temperature control of photonic components. She recently completed her Ph.D. degree in the mechanical engineering department at Tufts University on water-based microchannel and Galinstan-based minichannel cooling beyond 1 kW/cm^2 heat fluxes.

Marc Hodes received his MS in mechanical engineering from the University of Minnesota, where he researched microelectronics dielectric liquid cooling, and a Ph.D. in mechanical engineering from the Massachusetts Institute of Technology, where he researched salt deposition (fouling) in supercritical water oxidation reactors. After more than 10 years at Bell Labs, he joined the Tufts University Mechanical Engineering Department in 2008 as an associate professor. His research areas include aerogel thermal insulators; heat transfer in microchannels containing superhydrophobic nanostructured surfaces; increasing the conversion efficiency of thermoelectric modules for precision temperature control and power generation; and liquid metal heat sink optimization.

Nathan Lower received his B.A. in mathematics, physics, and computer science from Coe College in 2001. After completing his Ph.D. in Ceramic Engineering at the University of Missouri-Rolla in 2004, he joined the Rockwell Collins Advanced Technology Center and is currently a principal mechanical engineer. He specialized in microelectronic system development, miniaturization, material development, thermal management, 3D MEMS fabrication and processing, and electroplating and PCB fabrication. During this time, he has developed a number of novel packaging and thermal management technologies, including Z-Fab (3D microfabrication process), electroformed die attach, inorganic thermal and protective composite materials and liquid metal cooling techniques.

Ross Wilcoxon received B.S. and M.S. degrees in mechanical engineering from South Dakota State University and a Ph.D. in mechanical engineering from the University of Minnesota. Prior to joining Rockwell Collins in 1998, he was an assistant professor at South Dakota State University. He is a principal mechanical engineer in the Rockwell Collins Advanced Technology Center where he conducts research and supports product development related to component reliability, electronics packaging and thermal management. He currently holds 23 U.S. patents.

INTRODUCTION

MICROCHANNEL HEAT sinks provide significant opportunities for enhanced thermal management technology through a combination of increased surface area and small length scales that lead to very low thermal resistance. In addition to providing surface area enhancement, microchannel cooling exploits the fact that the convective heat transfer coefficient in fully-developed laminar flow is inversely proportional to the hydraulic diameter. Therefore, although the caloric resistance of microchannels, $1/(\dot{m}c_p)$—where $\dot{m}$ is mass flow rate and c_p is specific heat—is high, extreme heat fluxes may be accommodated.

Tuckerman and Pease [1] introduced the thermal community to the opportunities afforded by microchannel cooling in 1981. They achieved a thermal resistance of 0.09 °C/W when a heat flux of 790 W/cm^2 was imposed on a 1 cm × 1 cm footprint portion of a 400 μm-thick silicon substrate utilizing single-phase water as the coolant. Their result remains the benchmark today.

In this study, the cooling potential of alternate fin configurations in microchannel heat sinks with both water and liquid metal as the coolant is investigated, based on the same physical constraints (1 cm × 1 cm × 400 μm heat sink volume, and total pressure drop of 214 kPa) as reported in Tuckerman and Pease [1]. Testing showed that under these constraints an optimized water-cooled microchannel test section

achieved a heat flux of 1002 W/cm^2 with thermal resistance of 0.071°C/W. For a liquid metal-cooled heat sink with larger minichannels, testing was constrained by high pressure drops in the test section that that limited the coolant flow rate. However, this configuration did demonstrate a minimum thermal resistance of 0.077°C/W under similar temperature and pressure drop constraints as used in [1] and, with a higher temperature limit, achieved a maximum heat flux of 1.5 kW/cm^2.

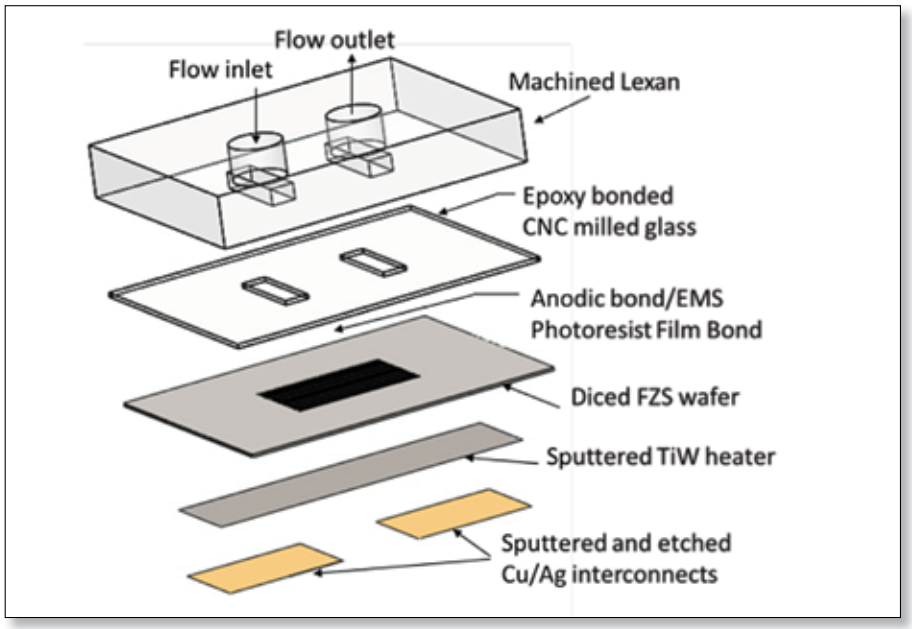

FIGURE 1: Exploded view of microchannel test section.

TABLE 1: MICROCHANNEL TEST SECTION GEOMETRIES

Configuration	Coolant	Channel Width [μm]	Wall Thickness [μm]	Number of Channels	Heater Size [mm^2]
1	Water	50	50	100	98
2	Water	44	20	160	90
3	Galinstan	334	26	28	92

BACKGROUND

Hodes *et al.* [2] reviewed the literature on subsequent investigations and developed a first-order model that predicted that thermal resistance can be reduced by 23% and 40% using optimal water-based microchannel and Galinstan -based minichannel heat sinks, respectively, under the constraints imposed by Tuckerman and Pease [1].

Galinstan[2] is a liquid at room temperature and its thermal conductivity of 16.5 W/m.K (i.e. 28 times that of water) results in high convection heat transfer coefficients. Wilcoxon *et al.* [3] demonstrated its use as a coolant in a three-layer FR-4 prototype that included an integrated magnetohydrodynamic pump and achieved an effective thermal conductivity of 6,000 W/m.K. Due to the density and viscosity of Galinstan being ~6 and ~2.4 times that of water [3], respectively, it exhibits a relatively high flow resistance. In addition, Galinstan has a volumetric heat capacity (ρc_p) that is approximately one-half that of water [4], which further increases the caloric thermal resistance. Therefore, the flow resistance must be reduced when the coolant is changed from water to Galinstan and optimal channel spacing will vary significantly depending on the coolant [2]. For the geometry constraints of this study, the majority of the total thermal resistance for water is due to the convective thermal resistance ($1/(hA)$); however, with Galinstan the caloric thermal resistance ($1/(\dot{m}c_p)$) is much more significant. Therefore, for a prescribed pressure drop, Galinstan requires larger flow channels (i.e., minichannels) that enable sufficiently high flow rates to minimize caloric thermal resistance.

TEST SECTION AND EXPERIMENTAL APPROACH

Three different heat sink geometries, specified in Table 1, were tested in this study. The heat sinks consisted of a 400 μm-thick float-zone silicon substrate into which 302 μm-tall channels were cut to a controlled depth using a Disco (Model DAD321) dicing saw. A titanium-tungsten (TiW) heating element, slightly less than 1 cm^2 in size to account for any misalignment with the fins, was sputtered onto the other side of the substrate. Configuration 1 was similar to that utilized by Tuckerman and Pease [1], Configuration 2 was optimized using the methodology of [2] and Configuration 3 had a minichannel geometry optimized for use with Galinstan. Figure 1 shows an exploded view of the test section. Details on the test section fabrication and assembly processes are described in [4].

TEST SETUP

Coolant was pumped through the test sections with a magnetically driven gear pump. Liquid passed through a heat exchanger that was cooled with an external liquid chiller to maintain a test section inlet temperature of 20°C. Temperatures were monitored using Type-T thermocouples at the test section inlet and outlet and the pressure difference across the test section was measured using an Omega® PX409 differen-

[1] The thermal resistance is defined as $R = (T_{max} - T_{in})/q$, where q is the heat dissipation, T_{max} is the highest measured temperature on the heating element and T_{in} is the inlet temperature of the liquid.

[2] Galinstan is the trade name of a eutectic alloy of gallium, indium and tin developed by Geratherm Medical AG (Geschwenda, Germany) and is used as a non-toxic replacement for mercury in oral thermometry.

tial pressure transducer. An infrared (IR) camera was used to measure the temperatures of the heater, which had been painted.

Water testing used an open loop in which a steady flow of deionized (DI) water was supplied to an open beaker from which the pump drew out a controlled rate. The water was then pumped through a 5 µm filter. Galinstan testing was conducted with a closed loop that recirculated the liquid metal and included a custom stainless steel filter designed to remove any oxidized particles of the Galinstan that could block test section channels. The filter included a mesh screen and also was oriented with the exit below the entrance so that lower density particles would separate from the flow.

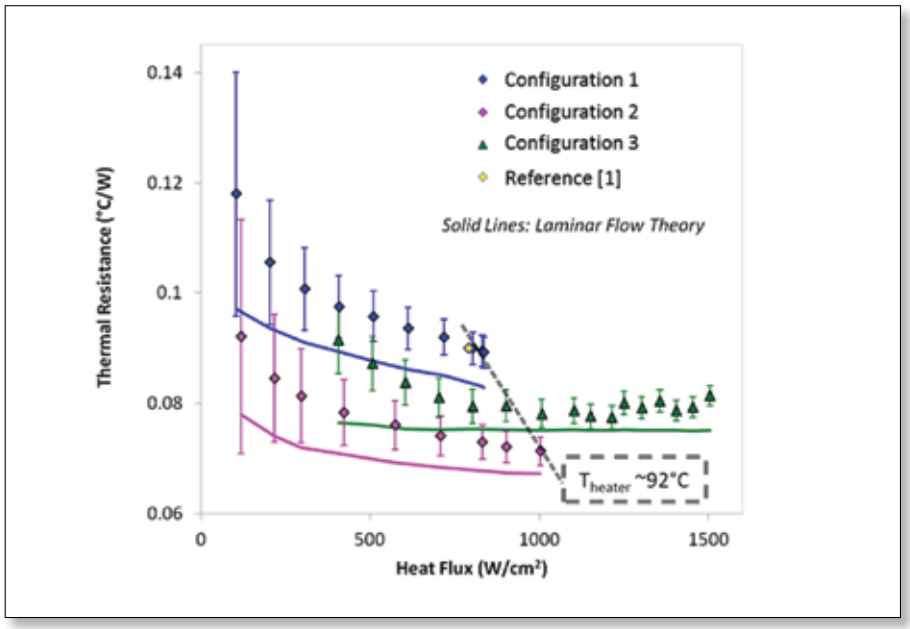

FIGURE 2: Measured versus predicted thermal resistances for the three microchannel test section configurations defined in Table 1.

EXPERIMENTAL TEST RESULTS

Figure 2 shows the measured thermal resistance as a function of heat flux for the three configurations. In each test, the total system pressure drop was held constant at 212 ± 2 kPa. Testing with water was limited to the maximum average heater temperature of ~92 °C indicated in the figure. The thermal resistance values shown in this figure are based on the average temperature of the trailing edge of the heater and are normalized to a heater area of 1 cm². Configuration 1 testing reproduced the thermal resistance, and exceeded the maximum heat flux, reported in [1] while the results for Configuration 2 demonstrated that the optimized microchannel geometry achieved a minimum thermal resistance of 0.071°C/W, which is ~21% lower than reported in [1] with a maximum heat flux of over 1kW/cm². The thermal resistance of the Galinstan minichannels (Configuration 3) fell between those of the other two configurations. Because Galinstan has a boiling point >1,300 °C, Configuration 3 could operate at higher heat fluxes to a maximum value of more than 1.5 kW/cm². At this heat flux, the average heater temperature was 157 °C with a peak hot spot temperature of 174 °C. Error bars in the plot indicate the measurement uncertainty as calculated using the method presented by Kline and McClintock [5]. Solid lines in the plot indicate the thermal resistance values predicted for laminar flow through the heat sinks.

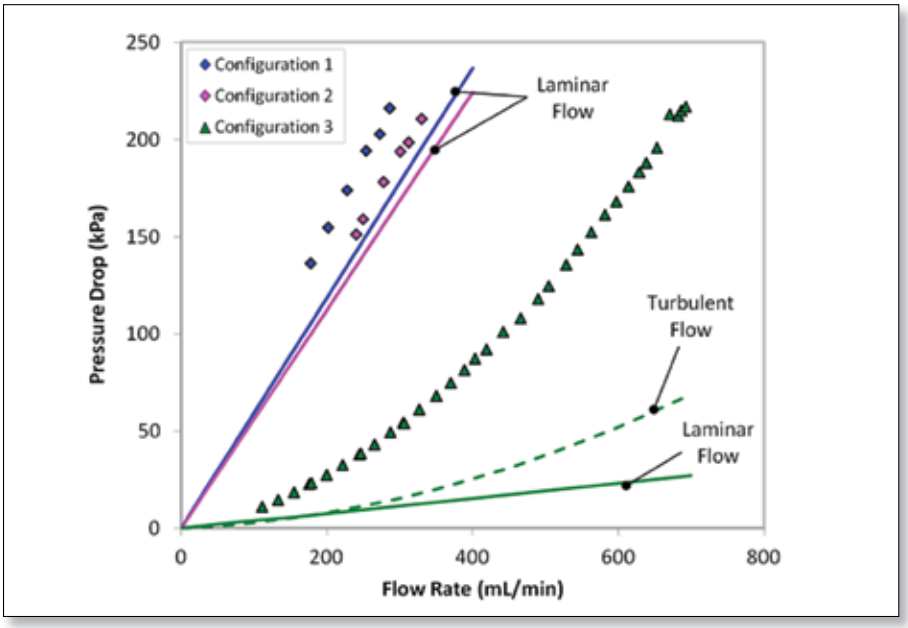

FIGURE 3: Measured versus predicted pressure drops for the three microchannel test section configurations defined in Table 1.

Symbols in Figure 3 show the experimentally measured overall pressure drop in the test section as a function of coolant flow rate. The lines indicate the predicted pressure drop associated with flow through the channels (flow through the channels as well as channel entrance/exit effects) for each configuration; both laminar and turbulent predictions are shown for the configuration for liquid metal cooling.

DISCUSSION

Thermal resistance results for the water-cooled microchannel heat sinks re-

produced thermal resistance reported by Tuckerman and Pease [1] and demonstrated the efficacy of the more comprehensive optimization method proposed by Hodes et al. [2] that reduced the thermal resistance by 21%. Measured thermal resistances were generally ~10% higher than laminar flow theory predictions. This relatively small offset is likely due to a combination of non-uniformities in the flow distribution, imperfections in the fin geometry and some contribution of conduction through the silicon substrate between the heater and the fins. The liquid metal minichannel heat sink did demonstrate a low thermal resistance of 0.077°C/W and the ability to cool heat fluxes up to 1.5 kW/cm^2. However, it did not achieve the extremely low thermal resistance performance predicted by Hodes *et al.* [2], primarily due to the fact that flow rate was limited to less than 700 mL/min. This limitation can be best understood by comparing the measured system pressure drop and predicted channel drops of the three configurations, shown in Figure 3.

Due to the extremely small hydraulic diameter of the microchannels, the system pressure drops in Configurations 1 and 2 are dominated by the channel pressure drop. In contrast, the minichannels in Configuration 3 have a much smaller contribution to the overall pressure drop, even if the flow is turbulent. In the liquid metal heat sink, the 'minor' losses associated with the complex three-dimensional flows entering and leaving the test section actually led to the majority of the overall pressure drop. Improved design of the flow in the test section would greatly reduce these pressure drops and allow the flow rate to increase. The optimized geometry of Configuration 3 was based on predictions with a flow rate of ~1,300 mL/min rather than the ~700 mL/min that was achieved with the current test setup.

CONCLUSIONS

Microchannel heat sinks that utilize single-phase water as the coolant at high heat fluxes were tested and experimental data, which agreed well with theoretical predictions, for the flow and thermal resistance were provided for two different configurations. The authors validated the results reported by Tuckerman and Pease [1] for a thermal resistance of 0.09°C/W and demonstrated an optimized geometry based that cooled a heat flux of 1002 W/cm^2, with a lowest reported thermal resistance of 0.071°C/W. Galinstan-based heat sinks demonstrated a thermal resistance as low as 0.077°C/W, which could be further reduced with an increased flow rate. Configuration 3 (with liquid metal) had higher than expected inlet/outlet pressure drops that prevented operating the liquid metal cooled minichannel heat sinks at their full potential. Testing with liquid metal did demonstrate an exceptionally high heat flux capacity of more than 1.5 kW from an area of ~1cm^2.

ACKNOWLEDGMENTS

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CVD Diamond – Integrating a Superior Thermal Material

Thomas Obeloer, Bruce Bolliger
Element Six

INTRODUCTION:

AS SEMICONDUCTOR devices continue to increase in power density, heat fluxes are becoming extremely high (several tens of kW/cm^2), and can represent, for example in GaN RF devices, five times that of the sun's surface. This trend is increasing thermal management challenges for these electronic devices. It has been as stated by various sources [1] that heat related issues are a common cause of failures in high-end electronic systems. This can be for both a catastrophic failure due to devices exceeding allowable operating temperatures as well as failure to achieve required system lifetime due to exposure to elevated thermal loads and possibly leading to failures in interfaces, connections or the device itself.

This article covers several important issues that advanced thermal solutions, particularly for RF power amplifiers, must address. Here, we are concentrating on new materials, such as CVD (chemical vapour deposition) diamond as a heat spreader to reduce overall package thermal resistance compared to today's more commonly used materials for thermal management. A practical application example of an RF device mounted on a CVD diamond heat spreader is modeled and analyzed for its impact on the overall package thermal resistance.

CVD DIAMOND

Diamond possesses a remarkable set of properties including the highest known thermal conductivity, stiffness and hardness, combined with high optical transmission across a wide wavelength range, low expansion coefficient and low density. These characteristics can make diamond a material of choice for thermal management to significantly reduce thermal resistance. To synthesize the diamond for this purpose, the first step is choosing the most suitable deposition technology. Microwave-assisted CVD enables the best control of grain size and grain interfaces to generate high-quality, high repeatability, polycrystalline diamond at the thermal conductivity level needed for particular applications. CVD diamond is now readily commercially available in different grades with 1,000-2,000 W/m-K thermal conductivities. Also very important is the fact that CVD diamond has fully isotropic characteristics, enabling enhanced heat spreading in all directions. Figure 1 shows a comparison of the thermal conductivity of CVD diamond with other materials traditionally used for heat spreading purposes.

With recent technology advances, CVD diamond has become readily available in volume and costs have declined rapidly. Unmetallized CVD diamond heat spreaders are available today at a typical volume cost of \$1/mm^3. Prices vary dependant on the thermal-conductivity grade used. With a typical thickness between 0.25 - 0.40 mm and lateral dimensions equal to the die size, a diamond heat spreader for RF devices will often be less than 5 mm^3 in size. Thus, for an incremental cost of a few dollars at the chip level, system costs can be substantially reduced. For instance, enabling system operation at an elevated temperature can reduce both the initial cost of the cooling sub-system and the on-going operating cost as well. And using an appropriate die-attach method, diamond heat spreaders provide reliable thermal management solutions for semiconductor packages [2].

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Bruce Bolliger is the head of semiconductor business at Element Six, where he leads worldwide semiconductor industry business development for synthetic diamond applications. He brings more than 20 years of experience in manufacturing, business development and marketing to his current role, as well as seven years of operations management experience in Asia. Prior to joining Element Six, Bolliger served as head of service solutions organization for test and measurement device manufacturer, Tektronix, in Singapore. In this role, he was responsible for after-sales support of product lines across the Asian market, and is credited with started new calibration service business in China, India and Japan.

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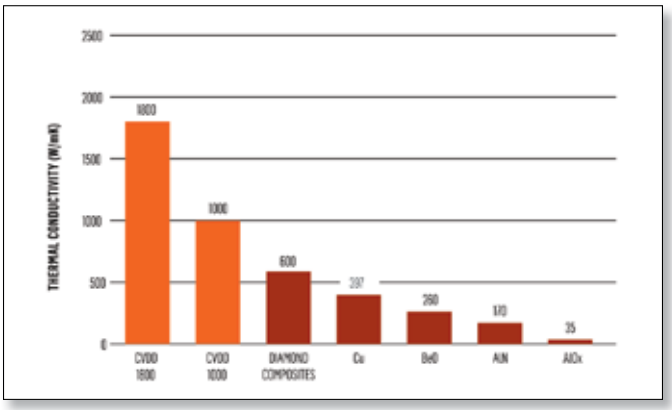

FIGURE 1: Comparison of thermal conductivity of CVD diamond and other, 'traditional' heat spreading materials [2, 3]

FIGURE 2: Advanced CVD diamond heat spreader design exhibiting a patterned metallization for a high-power laser-diode application

SOLUTIONS TO THERMAL ISSUES IN DEVICE PACKAGES FOR HIGH-END APPLICATIONS

To harvest the maximum heat-spreading effectiveness of diamond in the overall system design, package integration issues need to be carefully considered. Failure to address any one of these issues will result in a sub-optimal thermal solution. Here are the most important ones to be considered:

- Surface preparation
- Metallizations
- Mounting techniques
- Diamond thickness
- Functional considerations.

- Surface preparation: The surfaces of die level devices have to be machined in a suitable fashion to allow good heat transfer. Both the macro scale shape issues, typically described by the surface flatness and the surface roughness itself, which is stated in Ra, an arithmetic value of filtered roughness profile from deviations about the center line, are to be considered. Surface flatness for heat spreaders should typically be less than 1 micron/mm and the roughness better than Ra < 50 nm, which can be achieved by polishing techniques. Any surface protrusions can inhibit heat transport and are not allowable. Any deficiency in flatness must be compensated for by the mounting techniques and will cause higher thermal resistance. In general, flatness is less important to smaller devices such as laser diodes or RF transistors having edge lengths up to 1.5 mm. However, for larger devices, such as laser diode arrays, RF MMICs or power transistors having dimensions of ~3 - 5 mm, a flatness of less than 1 micron / mm is required.
- Metallizations: High-quality, sputter-deposited, thin-film metallizations are strongly recommended for advanced thermal solutions. As thermal contact resistance between the device and the heat spreader must be minimized, any additional metal interface being added to the system must be avoided. Sputtered layers, especially of titanium, can form a very effective chemical bond with CVD diamond to ensure long-term stability even at elevated temperatures. To separate the required gold attach layer from the titanium adhesion layer, a platinum or titanium / tungsten (TiW) barrier layer is recommended. Adhesion and barrier layer thicknesses should be in the range of 80 – 200 nm. The thickness of gold attach layer is usually 500 – 1,000 nm for soldering purposes, and in some rare instances is as thick as 2,000 – 3,000 nm when high electrical current (several tens of Ampere) is required. Diamond's inherent insulating property, combined with patterned metallizations, enables the heat spreader to also act as a submount for additional device mounting and/or wire bonding termination pads. Figure 2 shows a sample CVD heat spreader with a patterned metallization for a high-power laser-diode application. The part shown here has overall dimensions of 3.00 x 3.00 mm and contains connected and isolated gold areas for die mounting and wire bonding as well as a central pre-deposited AuSn (gold/tin) solder pad (0.4 mm wide central shaded strip).
- Mounting techniques: Whereas in some advanced device applications, such as high-power laser diodes, atomic-force bonding techniques are being considered, most applications currently employ soldering techniques for die attachment to the heat spreader. Again, solder layers should be kept to minimum thickness, particularly for the primary TIM1 (thermal interface material (TIM) between die and heat spreader), to minimize thermal resistance. Pre-deposited solder materials, such as eutectic AuSn (gold/tin at T_m=278 °C) or AuGe (gold/germanium at T_m=361 °C), with sputter-deposited or evaporated thicknesses of 2-4 microns, are recommended. A suitably designed die-attach process will result in near void-free solder layers only a few microns in thickness. Lastly, with diamond's thermal conductivity so high, even the secondary TIM2 thermal interface between the heat spreader and submount or package is important. The use of thermal pads or epoxy-type bonding, at thermal conductivities of about 0.8-4 W/m.K, prevents an optimal thermal design, so low melting solder materials such as pure In (indium) or InSn (indium/tin) materials are instead recommended. The attachment sequence usually creates the most critical TIM1 interface first and then solders the chip-on-heat-spreader into the package in a second step at a lower temperature. An attachment variation is using the same solder

TABLE 1: SOLDERING MATERIAL OVERVIEW [2]

Solder Material	Composition (wt%)	Soft / Hard	Liquidus Temp. (°C)	Solidus Temp. (°C)
InSn	52/ 48	Soft	118	eutectic
InSn	50 / 50	Soft	125	118
InAg	97 / 3	Soft	143	eutectic
In	Pure	Soft	156.6	156.6
InPb	70 / 30	Soft	171	162
SnPbAg	62 / 36 / 2	Soft	179	eutectic
SnPb	63 / 37	Soft	183	eutectic
SnPb	60 / 40	Soft	191	183
AgSn	3.5 / 96.5	Soft	221	eutectic
AuSn	80 / 20	Hard	278	eutectic
AuSn	75 / 25	Hard	356	278
AuGe	88 / 12	Hard	361	eutectic
AuSi	82 / 18	Hard	363	eutectic
AuSn	73 / 27	Hard	370	278
AuSn	70 / 30	Hard	390	278
InCuSil	5 / 27 / 68	Hard	760	743
InCuSil	28 / 72	Hard	780	eutectic

Note: Soft versus hard solder relates to the behaviour of the material; a soft solder is a ductile material whereas a hard solder is brittle.

material on both sides of the heat spreader and attaching the complete device/heat spreader/package stack in one step. In any instance of soldering, the expansion mismatch between the CVD diamond and the semiconductor material can influence performance and lifetime. However, even GaAs (Gallium Arsenide) devices up to an edge length of 2.5 mm can be hard soldered to CVD diamond without CTE-mismatch problems (note, the CTE for CVD diamond is 1.0 ppm/K at 300K). For edge lengths greater than 2.5 mm, using a soft solder can avoid excessive stresses in the device. Table 1 shows a wide range of solder materials commercially available to address various needs for soldering processes.

- Diamond thickness: The thickness of the CVD diamond is important. For devices with small hot spots and power densities greater than 0.5kW/cm^2, a thickness of 250 to 400 microns is sufficient. Diamond's isotropic characteristics effectively spread the heat to reduce maximum operation temperature at constant power output. However, applications with larger heat spots on the order of 1 – 10 mm in diameter require thicker diamond for better results. An example is disk lasers that can have an optical output power of several kW and a power density of about 2kW/cm^2; a diamond thickness of several mm has proven to be beneficial to its operation [4].
- Functional considerations: There are also functional requirements that may be important. One is the electrical conductivity of the heat spreader. For devices such as laser diodes, it is easiest to run the drive current through the device and the heat spreader for ground contact. For other devices, the heat spreader is required to be insulating. As CVD diamond is an intrinsic insulator, this insulation can be maintained by keeping the side faces free of metallization. This may be required for RF amplifiers and transistors, especially at higher frequencies (f > 2 GHz).

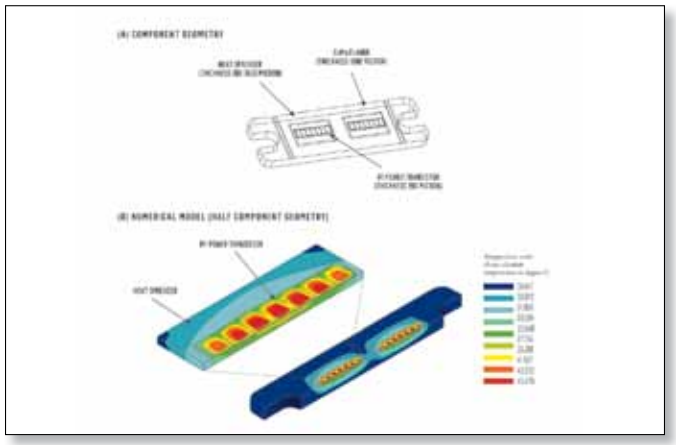

FIGURE 3: Thermal analysis of a RF VDMOS power amplifier package [4].

Thermal simulation helps optimize the heat spreader configuration to find the best solution based on power output needs, material thickness, metallization scheme, heat source geometry and package configuration. For design optimization, it is important that the thermal simulation model the complete junction-to-case system, including the device details, all interfaces, materials and the subsequent heat sinking solution.

APPLICATION EXAMPLE

To demonstrate the impact of a diamond heat spreader in a practical example, an RF- amplifier design was analyzed. In this example, a VDMOS power amplifier package was initially made with a BeO (berillium oxide, dimension 7.50 x 3.00 x 1.00 mm) heat spreader on a CuMo (copper/molybdenum) flange (dimensions 34 x 10 x 1.60 mm). Details of the components used in this simulation are shown in Figure 3. The end user was interested in lowering the overall thermal resistance of the system design as well as avoiding the use of BeO due to its toxicity. Thermal modeling of the design was performed with parameters for heat-spreader thermal conductivity and thickness using an In/Sn-based solder solution.

The key findings are shown in Figure 4. It demonstrates the temperature profile junction-to-case for one of the optimal designs (out of a total of 12 models run with BeO and 2 diamond grades, 2 different thicknesses, and 2 heat spreader sizes). Note, that the distance from bottom given in the horizontal axis corresponds to the actual thickness used in this simulation case. Here, the heat spreader solution using CVD diamond with a thermal conductivity of 1,000 W/m.K and thickness of 0.30 mm was found to have 30% lower thermal resistance. (The original solution used a 1.00 mm thick BeO heat spreader and has been taken as the base case, see Figure 5.) Note the almost horizontal, constant temperatures within the CVD diamond, which indicates that the heat spreader is not even used to its full capability. But even so, the improved

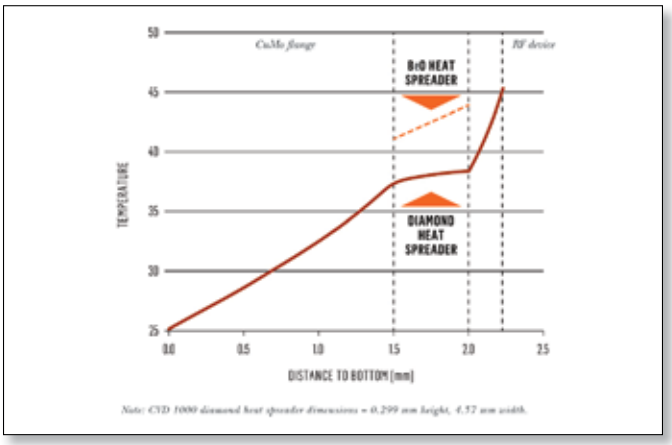

FIGURE 4: Predicted temperature profile as a function of height for an RF VDMOS power amplifier package having either a BeO or CVD 1000 heat spreader [4].

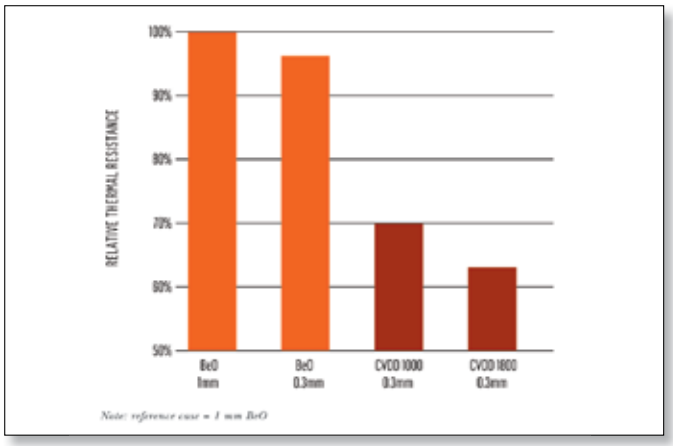

FIGURE 5: Predicted junction-to-case thermal resistance of an RF VDMOS power amplifier package as a function of heat spreader [4].

thermal resistance of the diamond heat spreader has led to this device functioning with better linearity in its RF performance and with improved reliability due to its reduced junction temperature. The results of these simulations were validated at the end user site by means of infrared (IR) thermography. Measured temperatures were within 5 °C of the simulation results.

OUTLOOK, FUTURE DEVELOPMENTS

One important finding from the above example is the need to modify device architecture for improved thermal management. The main temperature rise is within the device itself. Here, a thinning of the substrate, to bring it closer to the diamond heat spreader, would further enhance the thermal design. Also, mounting such devices with the active layers facing the diamond would provide even further benefit. An example would be the mounting laser diodes p-face down with the quantum well structures soldered directly against the heat spreader. Another way to bring the device gate junction closer to the diamond is the use of a different substrate altogether. This has been demonstrated by using GaN (gallium nitride) on diamond wafers, which remove both the Si substrate and transition layers, replacing them instead with CVD diamond [5]. The result brings the diamond material within 1 micron of the heat generating gate junctions. Initial users of GaN-on-diamond wafers for RF HEMT devices have demonstrated as much as three times the power density when compared to equivalent GaN/SiC (silicon carbide) devices, which is today's leading technology for advanced power devices [6].

Another improvement in the design of diamond heat spreader components embeds CVD diamond in CuW (copper/tungsten), CuMo (copper/molybdenum) or other packaging materials. This package-design improvement cost effectively decreases thermal resistance of the path between gate junction and package case.

SUMMARY

As can be seen, significant thermal-management improvements to electronic systems can be realized by using advanced materials such as CVD diamond. The integration can be relatively straightforward as the diamond heat spreader can be a direct replacement to AlN (aluminium nitride), BeO (berillium oxide) or other advanced ceramics. Attention to detail at the interfaces is important to keep overall thermal resistance low and thereby optimize the effectiveness of the diamond. For example, once the thermal resistance of the TIM1 (primary thermal interface material) is minimized, attention must be turned to the secondary interface (TIM2) as this now would become the limitation to the overall system performance.

As CVD diamond becomes more attractive as a heat spreader through improved synthesis technology, advanced processing and on-going cost reduction efforts, its use in high power density applications has increased. It is expected that this trend will continue in the years to come, in line with the ever increasing need for smaller and more powerful electronic devices and systems.

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Jet Impingement on Micro Pin Fins

Sidy Ndao
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INTRODUCTION

RECENT YEARS HAVE witnessed a surge in sophisticated personal portable electronic devices (e.g., smart phones, tablet PCs and wearable electronics) and emerging technologies requiring extensive computing (e.g., artificial intelligence, signal processing and data mining), garnering much interest for research and development of miniaturized CMOS technology (e.g., 14 nm generation) and three-dimensional integrated circuits (3D IC) architectures. This miniaturization of the electronic semiconductors along with their increasing operating frequencies has led to an exponentially spiraling increase of the devices' heat flux. Unless cooled properly below their typical maximum operation temperature, resulting high surface temperatures will lead to the degradation in performance and failure of the electronic chips. With air-cooled cooling technologies clearly not able to accommodate the increasing power density of electronic and photonic devices, advanced cooling technologies need to be explored.

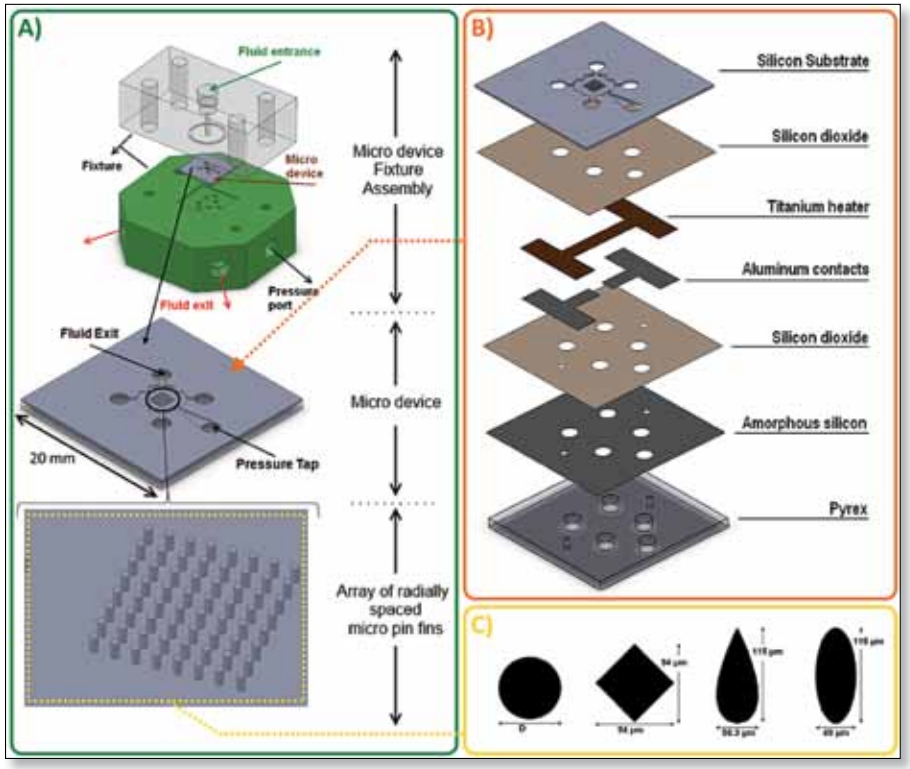

FIGURE 1: a) CAD illustration of micro device (micro-cooler); **b)** Exploded CAD view of micro device; **c)** Micro pin fin geometries with dimensions, D = 50 – 125 μm.

Jet impingement heat transfer has long been identified as a promising cooling solution due to its high heat transfer coefficients, especially at the stagnation zone. Further improvements can be attained by introducing enhanced microstructures on the impinging surface, hence jet impingement on micro pin fins. This article presents recent experimental work carried out on the single-phase and flow boiling heat

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transfer of jet impingement on micro pin fins for the thermal management of high heat flux microelectronics.

MICRODEVICE DESIGN AND FABRICATION

The micro device (i.e., micro-cooler) used in this study consists of an array of radially spaced micro pin fins of various geometries and diameters ranging from 50 μm to 125 μm, with a height of 230 μm, pitch of 250 μm, and a base area of 2 × 2 mm^2. The design and configuration of the micro pin fins arrays are guided by an earlier study on the multi-objective thermal design optimization and comparative analysis of electronics cooling technologies [1]. Figure 1(a) shows a CAD representation of the micro device. As can be seen on the drawing, the micro device consists of an array of micro pin fins (64 micro pin fins) extruded from a silicon base of thickness 20 μm. Four fluid exit holes are symmetrically located around the pin fin array with a pressure transducer port extending from one of the sides. Underneath the silicon base is a 2 × 2 mm^2 titanium heater with a thickness of 100 nm. Power to the heater is achieved via two 1-μm thick aluminum pads extending from the two opposite sides of the heater.

For structural integrity of the micro device, a 1-mm predrilled Pyrex wafer was bonded to the bottom of the silicon substrate. Figure 1(b) shows an exploded view of the micro device assembly. As can be seen on the figure, the micro device is made up of several layers. The top foremost layer consists of the silicon substrate on which the micro pin fin structures are etched. Underneath the silicon substrate is a thin film oxide layer (880 nm) used as an electrical insulator. The heater is deposited underneath the oxide film and consists of a thin layer (100 nm) of titanium and a 1-μm thick layer of aluminum. The titanium layer acts as the actual heater while the aluminum layer is used for electrical contacts and vias. Because aluminum is very prone to electromigration failure as observed during the heat transfer experiments, the use of Al-Cu alloy is suggested instead.

The electrical resistance of the titanium film is much larger than that of the aluminum, such that all resistive heating occurs in the 2 × 2 mm^2 region of the exposed titanium. To protect the heater, a relatively thick layer of silicon dioxide (2.0 μm) is deposited on the heater. The last two layers shown on the figure consist of a 300 nm amorphous silicon and a 1-mm Pyrex wafer. The amorphous silicon is used to facilitate bonding between the Pyrex and the rest of the micro device by providing a conductive path for ions during anodic bonding. Electrical contacts to the heater are achieved through two small holes drilled through the Pyrex wafer then etched through the amorphous silicon and bottom silicon dioxide layer.

The micro pin fin geometries (Figure 1(c)) investigated were circular, elliptical, hydrofoil and square. The micro devices were fabricated using MEMS microfabrication techniques, consisting of steps of thin film deposition, photolithography, etching, Chemical Mechanical Polishing (CMP), bonding and dicing. Scanning Electron Microscopy (SEM) images of the micro pin fins are shown in Figure 2.

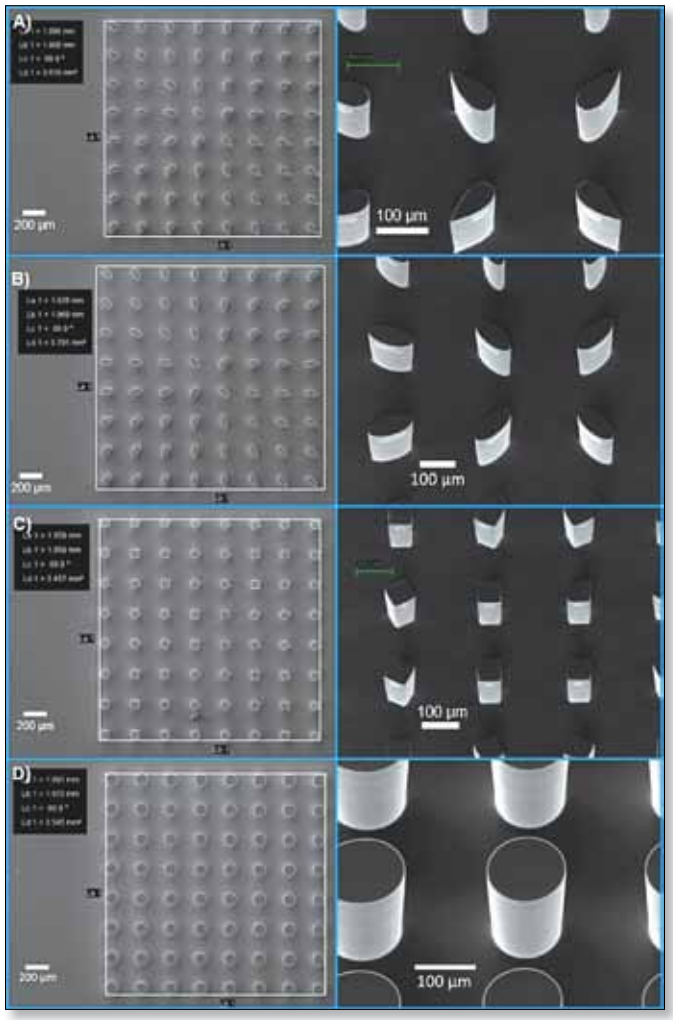

FIGURE 2: SEM images of **a)** hydrofoil pin fins, **b)** elliptical pin fins, **c)** square pin fins and **d)** circular pin fins.

HEAT TRANSFER EXPERIMENTS AND RESULTS

Heat transfer experiments were carried out to investigate the single-phase and flow boiling heat transfer enhancement of jet impingement on micro pin fins using refrigerant R134a as working fluid. The experiments were conducted for a single jet (jet diameter of 2 mm, stand-off ratio of 0.865) impinging on a 2 x 2 mm^2 base micro pin fins array over a wide range of jet velocities. The effects of heat flux, jet velocities, pin fin geometry and pin fin array configuration on the single-phase and flow boiling heat transfer characteristics are investigated.

Single-Phase Heat Transfer Enhancement

Figure 3(a) shows a comparison of the heat transfer coefficients based on the projected area (heater area) between jet impingement on a smooth surface and on 125 μm diameter micro pin fins. As can be observed from the figure, there is a significant enhancement of the heat transfer coefficients, reaching enhancement factors as high as 3.03 or about 200%

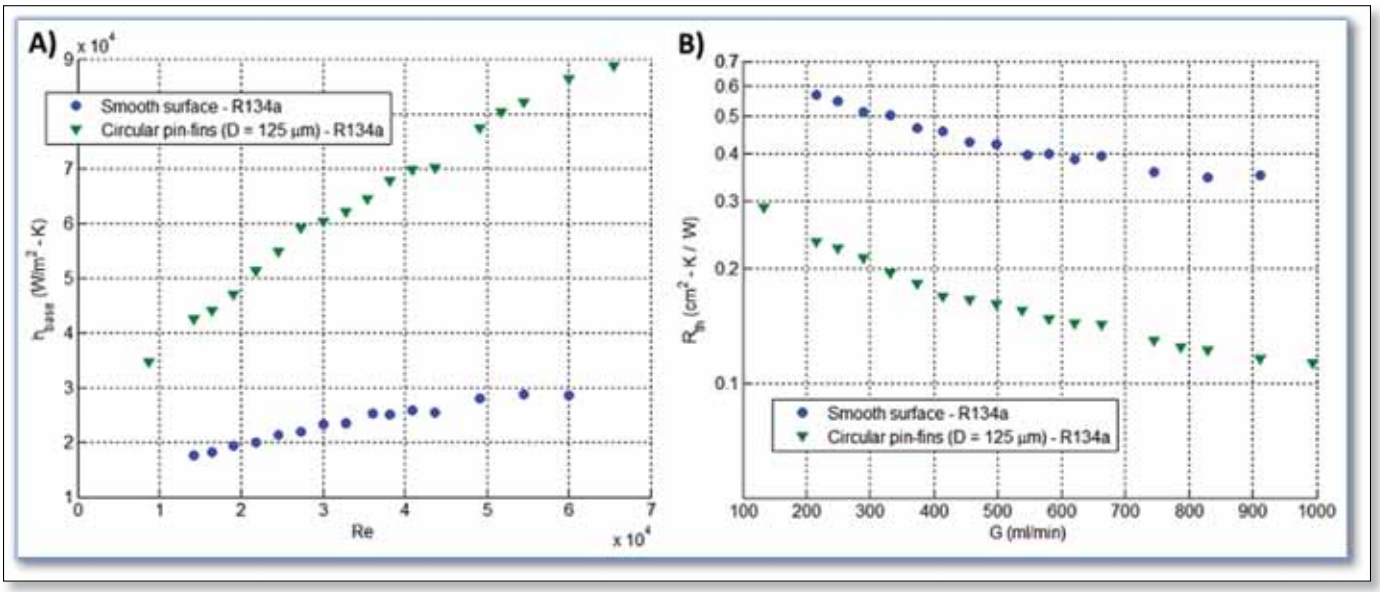

FIGURE 3: a) Heat transfer coefficients based on projected area as a function of Re (Re is based on jet diameter), smooth versus enhanced surface; **b)** Variation of the thermal resistances as a function of flow rate (flow rate is related to Reynolds number, e.g., 215 ml/min is Re = 14,176), smooth versus enhanced surface. [2]

increase in the heat transfer coefficients. This results in thermal resistances as low as 0.11 cm^2-K/W, Figure 3(b). With such thermal resistance values, heat fluxes as high as 450 W/cm^2 could be achieved with wall to inlet fluid temperature difference of only 50 °C. It is also interesting to note that the total heat transfer rate enhancement, 3.03, is larger than the area enhancement, 2.44. This suggests that there is enhancement of the heat transfer coefficients besides area enhancement as a result of the presence of the micro pin fins. This hypothesis is further supported by the strong Reynolds number (Re) dependency on the enhancement factor.

Flow Boiling Heat Transfer Enhancement

Flow boiling experiments with R134a are carried out at a saturation pressure of 820 kPa, corresponding to a saturation temperature of approximately 31 °C. Three Reynolds numbers, Re = 13,600, 28,300, and 50,100 (G = 207, 430, 762 ml/min), corresponding to jet velocities ranging from 1.1 - 4.0 m/s are investigated.

Figure 4 shows a side-by-side comparison of flow boiling jet impingement on a smooth surface, Figure 4(a), and square micro pin fins at three different velocities, Figure 4(b). There are two important observations worthy of mentioning in this comparison. First and foremost is the overall enhancement of the onset of nucleate boiling (ONB) from the smooth surface to the micro pin fins. For a given jet velocity, temperatures at which ONB occurs are consistently smaller for the micro pin fins in comparison to the smooth surface, with differences as high as 12 °C at a jet velocity of 4.0 m/s. For both surfaces, the ONB decreases with increasing jet velocity. Also related to the ONB is the absence or reduction of temperature overshoot (or temperature hysteresis) in the case of the micro pin fins.

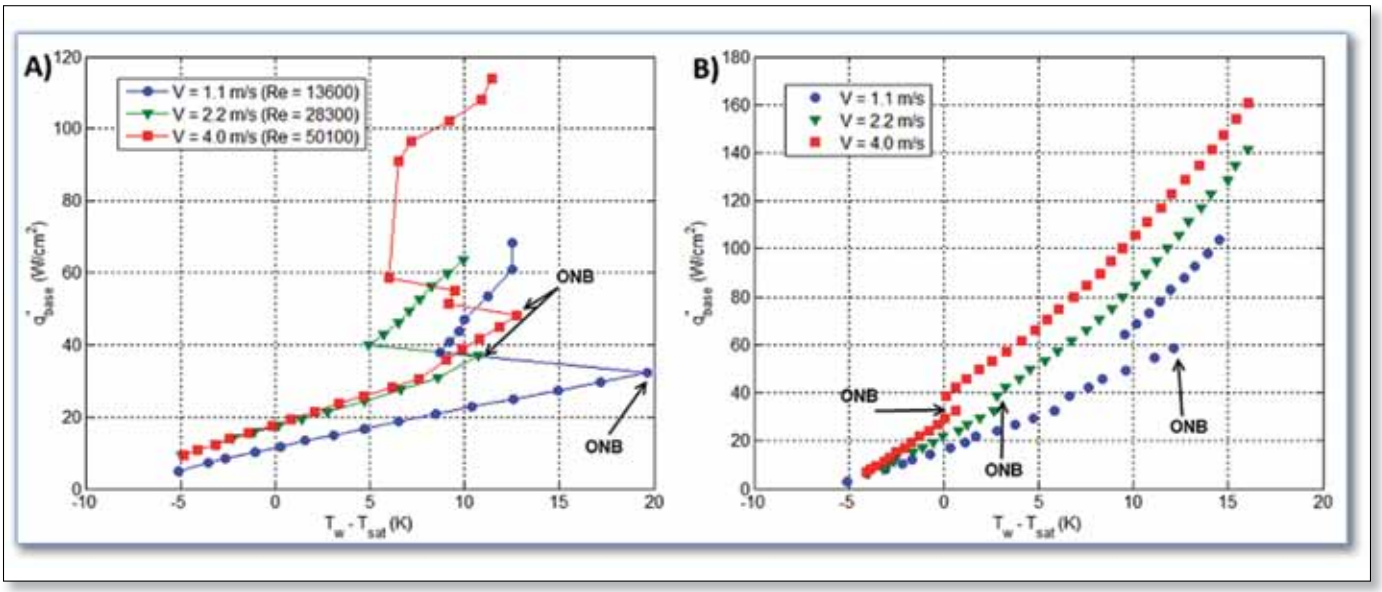

FIGURE 4: a) Boiling curve for jet impingement on a smooth surface, T_{in} = 26 °C, T_{sat} = 31 °C; **b)** Boiling curve for jet impingement on square micro pin fins, T_{in} = 26 °C, T_{sat} = 31 °C. [3]

Transition from single-phase to two phase regime occurs relatively very smoothly in comparison to the smooth surface. This characteristic of flow boiling jet impingement on micro pin fins, which is very beneficial to electronics cooling as it reduces thermal stresses, can be attributed to the increase in possible nucleation sites as a result of surface augmentation. The added surface increases the probability for a wider range of cavity sizes, thus increasing the probability for nucleation. Another source of increased nucleation sites is the Deep Reactive Ion Etch (DRIE) microfabrication process used to fabricate the micro pin fins. DRIE produces deep vertical sidewalls on the silicon wafer with characteristic peak-to-peak roughness in the micrometer and nanometer scales, forming cavities which could act as nucleation sites.

The second distinction between the boiling curves of the micro pin fins and the smooth surface is their difference in thermal performance. Boiling jet impingement on micro pin fins accommodates higher heat fluxes for a given wall superheat. Unlike single-phase heat transfer results, heat transfer enhancements are slightly smaller than area enhancements. This is possibly because nucleate boiling is more important than convective boiling in the boiling regime; hence, most of the enhancement occurs in areas of high active nucleation site density. With both cases however, the heat transfer coefficients increase with increasing jet velocities.

COMPARING MICRO PIN FINS GEOMETRIES

Figure 5(a) shows the effects of micro pin fin geometry on the single-phase heat transfer coefficients. The circular pin fins along with the square pin fins display the highest heat transfer coefficients for a given Reynolds number. The circular pin fins are shown to slightly outperform the square pin fins. The elliptical and hydrofoil pin fins displayed similar trends and magnitudes of their heat transfer coefficients. Their heat transfer coefficients values were, however, relatively lower compared to the circular and square pin fins, especially at higher Reynolds numbers. A more detailed comparison of the single-phase results can be found in [4].

Very high heat transfer coefficients are achieved with flow boiling jet impingement on micro pin fins (Figure 5(b)). Heat transfer coefficients exceeding 150,000 W/m^2.K are observed at a relatively low velocity of 2.2 m/s with the large (D = 125 μm) circular micro pin fins. Heat fluxes above 200 W/cm2 for wall superheat less than 15 °C and inlet subcooling as little as 5 °C have been demonstrated. Higher heat fluxes could have been achieved; however, to avoid device burnout, the experiments were carried out at heat fluxes much below expected CHF condition. One set of experiments where CHF was believed to have occurred is shown in Figure 5(b) with the hydrofoil pin fins; for an inlet subcooling of about 10 °C, CHF is reached at a heat flux of 275 W/cm^2.

With high single-phase and two-phase transfer coefficients along with being compatible with CMOS nano/microfabrication technologies, liquid-cooled jet impingement on micro pin fins positions itself as a promising cooling technology for the thermal management of high heat flux microelectronics. The use of multiple jets instead of one single jet can possibly further enhance the heat transfer coefficients.

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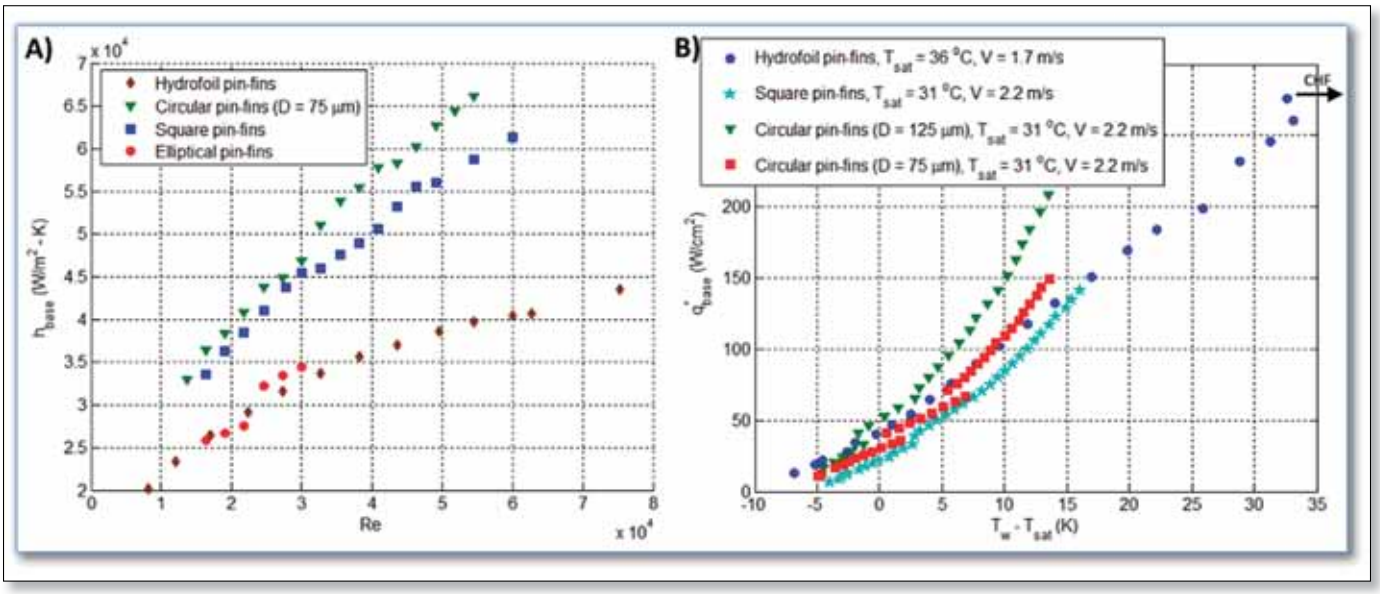

FIGURE 5: a) Effects of pin fin cross sectional shape on the single-phase heat transfer coefficients [4];
b) Boiling curve based on base area – effects of pin fins geometry [3].

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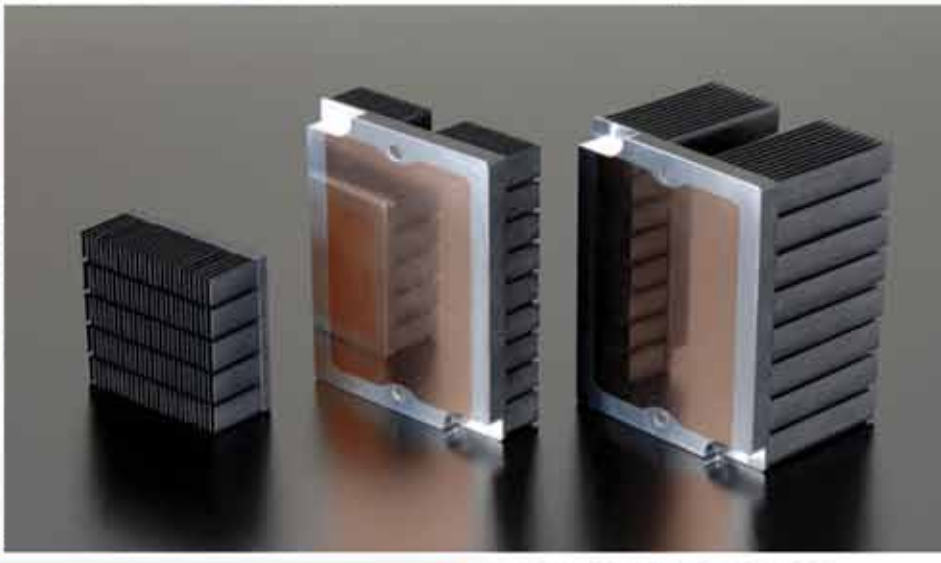

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