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MARCH 2015
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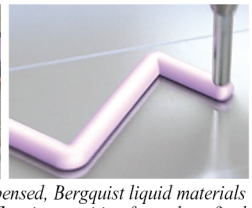

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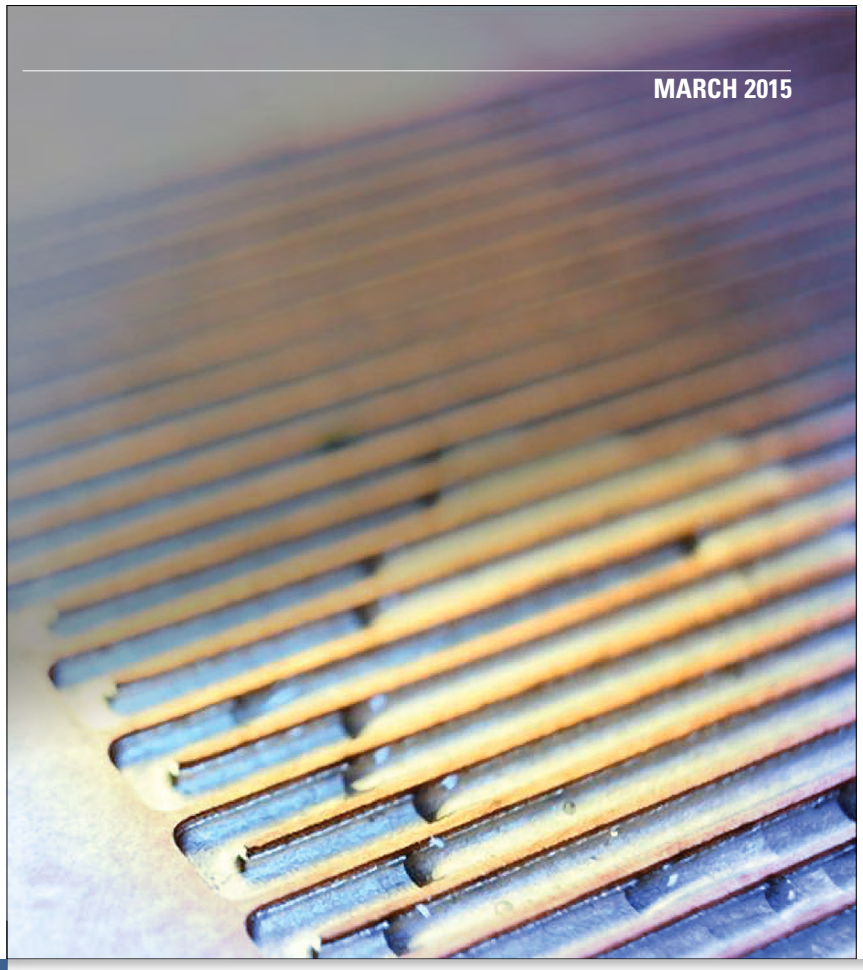

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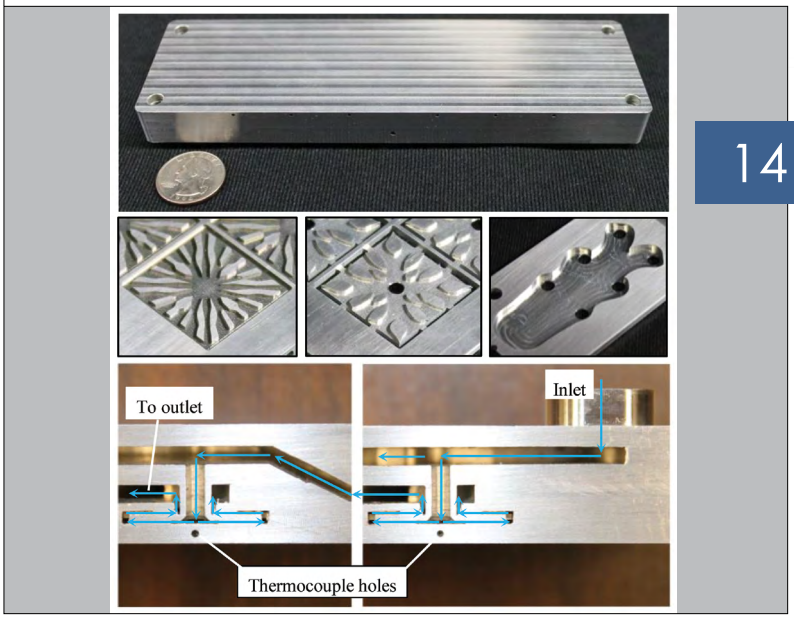

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Editorial

Encouraging and Investing

Jim Wilson, Editor-in-Chief, March 2015

Welcome to our first edition of ElectronicsCooling in 2015. Most of us start a new year with reflection on the topics of goals and accomplishments. Even with our busy schedules and work demands, forcing ourselves to pause and consider career progress and aspirations is beneficial. A common method of reviewing your progress is to start with your accomplishments for the prior year. Listing some short and longer term goals helps focus your desires and align them with the needs of your employer. Another important part of this assessment process is to identify training that would help you be a better and more productive employee. Following through with this training requires investment of time, effort, and money, usually from both the employee and employer. Investments like training usually have some expectation of a tangible return. For example, learning a new software program might make you more efficient or enable you to expand your design and analysis capability. Learning advanced testing techniques might prevent repeated errors in making measurements. For this editorial, I would like to encourage our readers to make some investments that have great return but are harder to quantify from a business perspective.

In the past few months I have been asked to write several letters of recommendation for friends and coworkers. Some of these were for technical awards and some for job promotions, and as of writing this editorial, a number of them have been awarded. While the recommendation letters are required as part of the nomination process, these individuals earned success with their accomplishments and hard work. Writing the letters was a nice diversion from my usually technical job and it has been rewarding seeing them receive their awards and promotions. Related, I have also increased my appreciation for those that encouraged and help me in the past.

As thermal engineers, much of our mental effort goes into managing complicated heat transfer processes and we can overlook opportunities to encourage others. Other barriers can come from the side effects of competition and confidence. An overly competitive environment can inhibit investing in others from a fear of making someone else even more competitive. Friendly competition is healthy and fosters even better ideas but should not prevent you from acknowledging others good work and input. Similarly, confidence in our work is required but overconfidence can hinder encouraging your teammates. I have come to truly appreciate coworkers that ensure everyone's contribution is acknowledged. They have learned to invest in relationships. Even if their relationship investments are not intended to have a response, I personally want to work harder for them. The environment set by an encouraging coworker also helps mitigate some of the stress that comes with working on challenging problems as a team.

Investing in coworker relationships extends beyond your immediate work environment. Technical conferences and meetings can be a good venue to collaborate and look for occasions to acknowledge the work of others. My personal opinion is that the some of the most valuable time spent at conferences is the interaction with colleagues during breaks discussing technical issues and fostering relationships.

A final challenge to you is to encourage your coworkers and invest in your professional relationships. It will be rewarding.

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Cooling Matters

News of thermal management technologies

THERMALLY UNSUITABLE PRODUCT DROPPED FROM SAMSUNG PRODUCT LINE

1/ 26/15 - Samsung reportedly dropped Qualcomm's Snapdragon 810 from its upcoming line of Galaxy S6 devices because Qualcomm's 20nm processors aren't running cool enough.

Samsung's reason for dropping the Snapdragon from its product line is extremely vague since it is well known that Qualcomms have been produced and sold in 20nm modems for more than a year.

It is unclear at this time how the drop will affect Samsung.

Source: Extreme Tech

LIQUID COOLING DECREASES ENERGY CONSUMPTION AND REDUCES FOOTPRINTS

2/2/15 - Icetope, a UK firm, partnered with Intel and the University of Leeds last year and launched a line of servers, which uses liquid cooling to cool electronics. The system, known as the PetaGen system, uses a combination of liquid coolants to cool electronics. Every motherboard is completely immersed in coolant inside a sealed container.

"The coolant is an exotic fluid called Novec developed by 3M, which is not electrically conductive and disperses heat from the components by convection. The blades fit into a rack-mount enclosure, with a separate cooling system in the rack that circulates water to remove heat from the blades. This arrangement enables a fully populated rack to mount up to 72 blade servers, each blade being a twin socket system based on the latest Intel Xeon E5-2600 v3 processors," according to V3.

The liquid cooling reduces the need for air condition in server rooms, which lowers energy consumption. Energy consumption is a common concern in data centers since the use of mobile devices is constantly growing and more data traffic comes online.

Source: V3

HIGH TEMPERATURE BRINGS DOWN DATA CENTER IN AUSTRALIA

1/19/15 - A heatwave that rose outside temperatures to 112 degrees Fahrenheit, brought iiNet's data center down in Western Australia.

The data center went offline due to equipment failures. Because servers can give off tremendous amounts of heat, the lack of sufficient cooling can lead to such cooling failures.

The record breaking temperature was the hottest day recorded in January since 1991. The high temperatures lead to an air conditioner failure, thus knocking the data center offline for more than six hours.

Heat bringing down data centers is very common; however, power infrastructure problems or cooling problems usually cause this occurrence, not outside weather.

"We have had multiple air conditioners fail on site causing temperatures to rise rapidly. We have additional cooling in now. We will begin powering services back up once the room has cooled adequately. If we are premature the room won't recover and risk the A/C failing again," Christopher Taylor, company representative, said.

Source: Data Center Knowledge

Datebook

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THERMAL SIMULATION TO IMPROVE LED CAR HEADLIGHT DESIGN

1/13/15 - Structural changes to LED headlights have generally been adding to the complexity of its production, according to researchers. Currently, the only constant in LED headlights is its thermal management.

CFD (computational fluid dynamics) simulation software is typically used to efficiently create prototypes of changes to LED headlights.

"The CFD analyst has to assign grids to the solids and flow spaces, creating an optimised computing mesh. This mesh aids the engineer in setting boundary conditions and influences the solution convergence as well as accuracy of the result," according to researchers.

Mesh generation for new lighting systems is very time consuming and details in the structures of headlights add to the complexity of this process. Researchers have discovered a solution – they believe LED car headlight designs can greatly benefit from thermal simulation.

Source: Electronics Weekly

NEED FOR HEAT SPREADERS YIELDS COOLING TECHNOLOGY

1/6/15 - The Air Force Research Laboratory and a small business partner have announced they are developing technologies that will help electronics stay cool. With funding from the Air Force Small Business Innovation Research program, the AFRL expects to produce a technology that "will enable successful use of high-power processors that operate on satellites."

One of the technologies currently being tested is an OHP (oscillating heat pipe)-embedded micro-chip carrier that reduces the temperature of satellite components to manageable thermal levels. This is an advantage because it improves reliability and allows opportunity to increase on-board processing. This technology is currently being developed by ThermAvant Technologies, LLC in Missouri.

Source: AFRL

RESEARCH GROUP AT U-MICHIGAN DEVELOPS HEAT-CONDUCTING PLASTIC

12/16/14 - A research team from the University of Michigan has developed a heat-conducting plastic that bends 10 times better than previous materials.

Plastic is a favorable material for electronic devices because it is lightweight, flexible and inexpensive. However, a known issue with plastic is its limited availability to dissipate heat. "The new U-M work could lead to light, versatile, metal-replacement materials that make possible more powerful electronics or more efficient vehicles, among other applications," according to researchers.

Source: University of Michigan

UNIVERSITY OF MICHIGAN

AIR FORCE FUNDS THERMAL MANAGEMENT PROJECT

12/16/14 - The Air Force has provided over $1.5 million dollars in funding to the Air Force Research Lab for an effort to improve methods of managing heat of electronics on fighter aircraft.

The goal of the project is to "enhance the technology and manufacturing readiness for nano-enhanced thermal interface material grease and to integrate it with power system modules that are currently used on advanced fighter aircraft."

"With further testing, the thermal interface material grease is expected to provide a 10 degrees Celsius or better reduction in junction temperatures. This reduction is expected to provide a direct increase in fuel cooling loop temperatures, improved end-of-mission thermal capability during ground idling, and improved reliability and cost savings," researchers said.

Source: Greene County News

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Strategies for the Thermal Modeling of Metal Traces on Printed Circuit Boards

Bruce Guenin
Assoc. Technical Editor

INTRODUCTION

AS INTEGRATED CIRCUIT (IC) devices get more complex, the interconnections between them provided by printed circuit boards (PCBs) get more complicated as well. Thermal simulation software tools are getting more capable of importing PCB layouts and automating the process of creating a model of the PCB whose local thermal conductivity is representative of the underlying layout. However, in many cases it is necessary to perform a thermal model of a package on a PCB without creating a highly detailed model of a PCB. This article is the first of a series of columns that will explore the effectiveness of different strategies for accurately accounting for heat transfer into a PCB, while using a simplified solid model of the PCB.

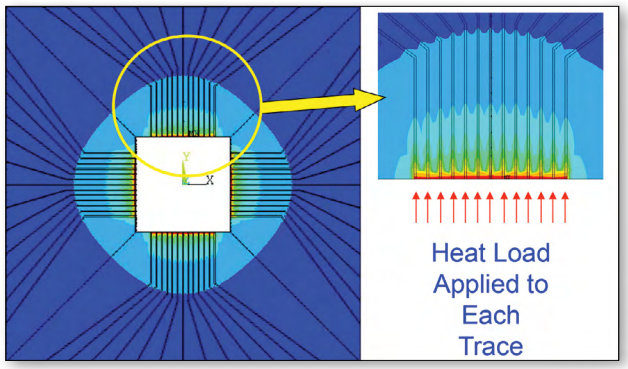

FIGURE 1a - Temperature contour map, top surface of board.

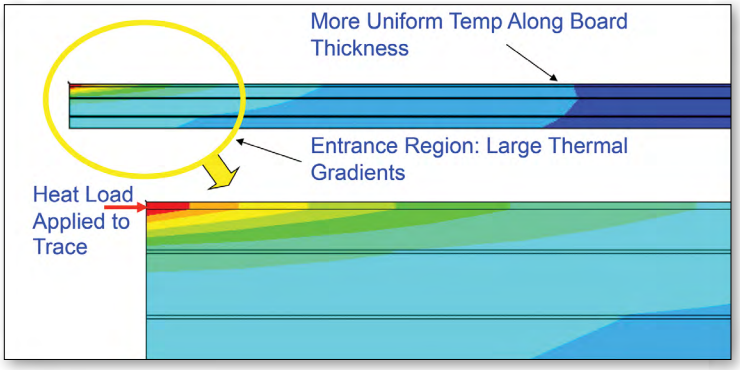

FIGURE 1b - Temperature contour map along cut through centerline. Both figures illustrate the method used of applying a heat load directly to the exposed cross-sections of the traces at the periphery of the cutout [Ref 2].

THERMAL MODEL

The heat generated by an IC often has several flow paths into the PCB it is mounted to. Quite often in ball grid array (BGA) packages the central balls connect to vias in the PCB that route the heat directly into the power and ground planes in the PCB. In contrast, the peripheral balls tend to be connected to surface traces on the PCB. Some of the heat conducted by the traces flows directly into the ambient air. However most of it will flow to the interior of the PCB and enter the power and ground planes. These planes are typically effective in spreading the heat from a given package over a large area in the PCB, whence it can flow more efficiently into the ambient air.

This analysis is devoted to exploring the heat transfer from the traces to the inner planes of the PCB. Any other heat flow path into the PCB is neglected in the model. The construction of the model is illustrated in Figure 1. The portion of the PCB where a package would normally be mounted has been removed. This exposes the cross-section of each of the traces at the periphery of the cutout. A heat flux is applied to the exposed surface of each trace. The magnitude of the heat flux to chosen so that a total of 1 W of heat is injected collectively into all of the trace cross-sections. There are adiabatic boundary conditions at the exposed cross-section for each trace so that all the applied heat flows from that surface into the trace.

For convenience, the PCB geometry corresponds to that of a JEDEC-standard PCB, that would be used in the thermal testing of BGA packages [1]. The board consists of six layers: the top metal traces, two interior planes, and three

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dielectric layers. The board is 101 mm sq. and is 1.54 mm thick. The interior planes are 35 µm thick. For reasons of test reproducibility, the traces on a JEDEC-standard PCB are 70 µm. However, in PCBs used in products, a 35 µm thickness is more common. Traces of both of these thickness values are analyzed in the model. The cutout in the PCB is 27 mm sq. Further details regarding the PCB construction may be found in a previous column [2].

A commercial finite element analysis (FEA) software tool was used to generate solid models of the multilayer board with a number of different trace configurations [3]. In all cases, the thermal solution was obtained assuming an ambient temperature of 0 ˚C (so that the reported temperatures represent $T - T_{Ambient}$) and a heat transfer coefficient of 10W/m^{2}K (typical of natural convection cooling) was applied to the top and bottom surfaces of the PCB.

The trace geometries are represented accurately in the model. Since the model was generated with an appropriately refined FEA mesh, the model results are assumed be "exact" when compared with the results of the models having simplified geometries.

Table 1 presents the various parameters characterizing the trace geometries for the three configurations studied. Each configuration has an "a" version and a "b" version. In all of the "a" versions, the trace thickness is 35 µm. In all of the "b" versions, it is 70 µm.

The images in Figure 3 illustrate the trace pattern of each configuration. [Note that a discussion of the thermal contours in this figure follows later in this article.]

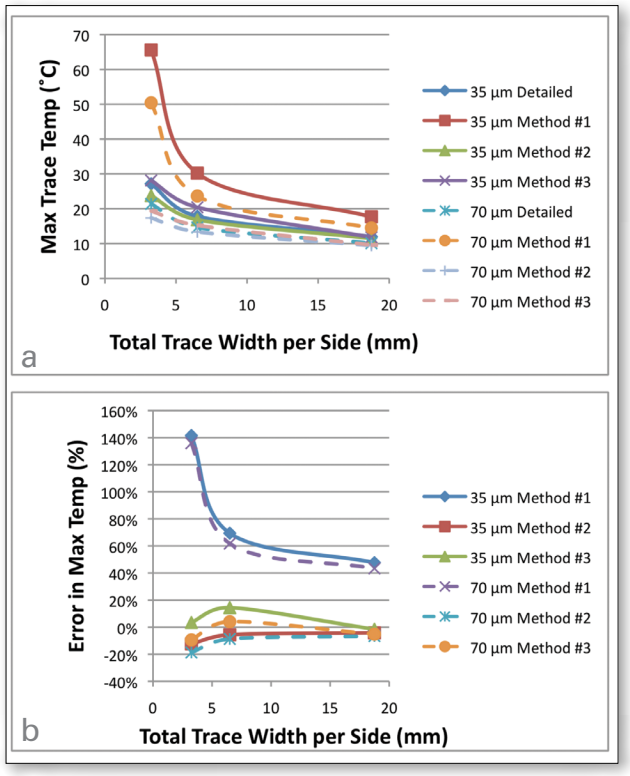

FIGURE 2 - Graphs depicting simulation results from Table 2 versus total trace width per side of the cutout in the parallel region of the traces: a) maximum trace temperature and b) error in maximum trace temperature.

SIMPLIFYING ASSUMPTIONS

It is common practice to represent the trace layer of a PCB as a continuous plane whose thickness equals that of the traces and whose thermal conductivity equals the copper coverage of the traces multiplied times the thermal conductivity of copper. This is commonly referred to as "smearing" the trace layer. This procedure is defined herein to be Method #1 and is specified as:

- Simplification Method #1: represent trace layers by a plane. Plane thickness = trace thickness. Plane effective thermal conductivity = Factor x thermal conductivity of copper. Factor = % of PCB surface occupied by the traces.

All of the simplified models discussed here represent the trace geometry by a plane. However, they differ by the

Table 1: Thermal conductivity of TPP laminate. The core laminate with annular vias from [12] is listed as benchmark case.

Table 1 - PCB Parameters							
Configuration Number	Trace Thickness	Number Traces/side	Trace Pitch	Trace Width	Sum of Trace Widths/side	%Cu in Parallel Trace Area	%Cu in Entire PCB Area
	(mm)		(mm)	(mm)	(mm)		
1a	0.035	13	0.65	0.25	3.25	38.5%	3.2%
2a	0.035	13	1.5	0.5	6.5	33.3%	6.1%
3a	0.035	25	1	0.75	18.75	75.0%	16.7%
1b	0.070	13	0.65	0.25	3.25	38.5%	3.2%
2b	0.070	13	1.5	0.5	6.5	33.3%	6.1%
3b	0.070	25	1	0.75	18.75	75.0%	16.7%

method used to calculate an effective thermal conductivity of the plane.

The thermal contour maps in Figure 1 indicate a significant thermal gradient in the traces as heat flows through them on their journey into the internal planes in the board. The side view also illustrates that the heat flows from the traces to the top plane of the PCB in a gradual way, due to the relatively low thermal conductivity of the board FR-4 dielectric (0.25 W/mK). The flow of heat from the traces to the plane is affected by the fact that the traces do not represent a continuous plane. Hence the heat flows, not uniformly over the full area of the dielectric, but is concentrated in local regions, directly under each trace.

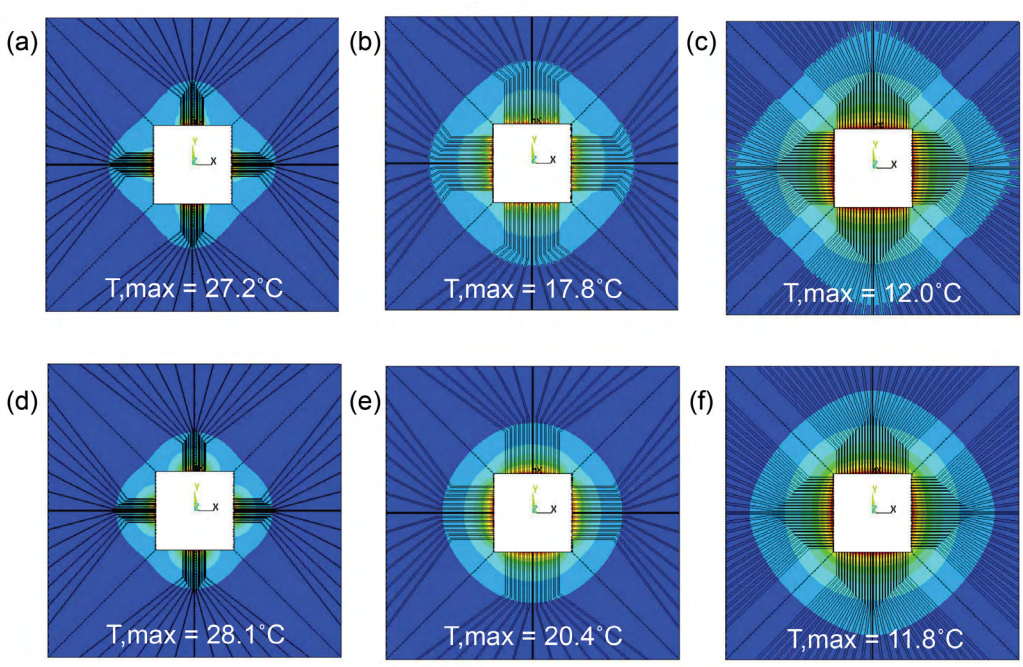

FIGURE 3 - Contour plots for three configurations (1a, 2a, and 3a) evaluated using two different methods (Detailed and #3) : a) Config 1a, detailed; b) Config 2a, detailed; c) Config 3a, detailed; d): Config 1a, Method #3; e) Config 2a, Method #3; f) Config 3a, Method #3.

It should be noted also, that the temperature of the trace approximates that of the underlying plane after a distance equal to approximately 10 times the dielectric thickness. Hence, it is the portion of the traces near the package that make the most significant contribution to the heat flow between the traces and the top plane.

The insight gained by these observations leads to the formulation of two other methods of calculation of effective thermal conductivity values that represent a derating of the thermal performance of a smeared plane, that, otherwise, would provide a much more efficient thermal path to the top plane than do the individual traces.

- Simplification Method #2: represent trace layers by a plane. Plane thickness = trace thickness. Plane effective thermal conductivity = Factor x thermal conductivity of copper. Factor = % of PCB surface occupied by the traces near the package, where the traces are parallel.

- Simplification Method #3: represent trace layers by a plane. Plane thickness = trace thickness. Plane effective thermal conductivity = Factor x thermal conductivity of copper. Factor is calculated as in Method #2. The thermal conductivity of the dielectric between the inner plane and the top plane = Factor2 x thermal conductivity of the dielectric. Factor2 = trace width/trace pitch.

Table 2: Thermal benchmarking of single-side and dual-side EICs. Characteristic elements are described in detail in [8].

Table 2 - Calculated Results							
Configuration Number	T,max Results				% Error		
	Detailed Traces	Method #1	Method #2	Method #3	Method #1	Method #2	Method #3
	(°C)	(°C)	(°C)	(°C)	(%)	(%)	(%)
1a	27.2	65.6	23.8	28.1	142%	-12%	3%
2a	17.8	30.2	16.8	20.4	69%	-6%	14%
3a	12.0	17.7	11.5	11.8	48%	-4%	-2%
1b	21.4	50.4	17.4	19.4	136%	-19%	-9%
2b	14.6	23.7	13.3	15.2	62%	-9%	4%
3b	10.1	14.5	9.4	9.6	43%	-7%	-5%
				Average	83%	-9	1%

Assumptions: $T_{Ambient}$ = 0˚C, Total Power = 1W
Heat Transfer Coef. = 10W/m^{2}K

CALCULATED RESULTS

The results of the calculations are detailed for all configurations in Table 2. The values of T,max for the 35 µm configurations are all higher than the corresponding ones for the 70 µm configurations, as expected. The values of T,max calculated using Method #1 are all higher than those calculated with the other methods. This should not be a surprise, since Table 1 indicates that the % copper averaged over the entire PCB surface is much lower that that calculated for the parallel trace region. For example, for configuration 3a and 3b, the % copper averaged over the parallel region is 75%, whereas the % copper averaged over the entire PCB is only 16.7%.

Methods #2 and 3 yielded values of T,max that are much closer to the exact values.

The graphs in Figure 2 depict the relative behavior of the different methods. Both the actual values of T,max and % error are plotted versus a parameter = total trace width per side = trace width x number of leads per side. Higher amounts of copper lead to larger values of this parameter. The graphs show that the accuracy of Method #1 improves at the higher copper levels. However, even at high copper levels, the error is still over 40%. At the lowest copper levels evaluated here, the error for Method #1 exceeds 100%.

There is much better performance with Methods #2 and #3. Averaged over all the cases studied here, Method #2 had -9% error and Method #3, 1%.

Figure 3 depicts selected temperature contour plots for all three configurations, version "a" (35 µm traces). The top row of images shows the results for the detailed trace models. The lower row depicts the results in which Method #3 was applied to the calculation of the effective thermal conductivity of the plane and the top dielectric. The values of T,Max were similar for the two approaches for each case. However, the detailed trace models clearly show the impact of the trace routing on the thermal gradients. The contours for Method #3 show, in general, more of a circular symmetry. [Note that the apparent presence of the traces in the lower set of images depicting Method #3 results is an artifact of using the same finite element mesh for all the solution methods applied to a particular PCB configuration. However, in the Method #3 models (as well as for #1 and #2) the same material properties were applied to all elements in the trace layer, making that layer truly isotropic in its thermal behavior.]

It was mentioned earlier that the assumed heat transfer coefficient equaled 10 W/m^{2}K, representative of natural convection. It should be noted that, for higher values of the heat transfer coefficient, the tendency for the heat to be transferred from the traces to the top plane in the region near the package would be even more pronounced. This would be expected to further increase the error in applying Method #1.

CONCLUSIONS

Three different strategies for using a convenient "smeared" planar layer to represent a layer of discrete traces were explored. The strategies that were most successful were based on an understanding of the local heat transfer between the traces and the top plane in the PCB that was presented in an earlier column [2]. They made use of the fact that most of the heat transfer between the traces and the top plane of the PCB occurs near the package and that the heat flow is concentrated in the vicinity of each trace and does not flow uniformly through the dielectric. Hence, the copper coverage near the package should be used in calculating the effective thermal conductivity of the smeared plane and the thermal conductivity of the dielectric should be derated by the same factor. The conventional method, which uses a value of copper coverage averaged over the surface of the PCB is much less accurate.

REFERENCES

[1] See, for example: JEDEC Standard JESD51- 9, "Test Boards for Area Array Surface Mount Package Thermal Measurements," available for free download at www.jedec.org.

[2] B. Guenin, "Entrance Effects for Heat Flow into a Multi-Layer Printed Circuit Board," ElectronicsCooling, Vol. 10, No. 4, November 2004.

[3] ANSYS®, Version15.0.

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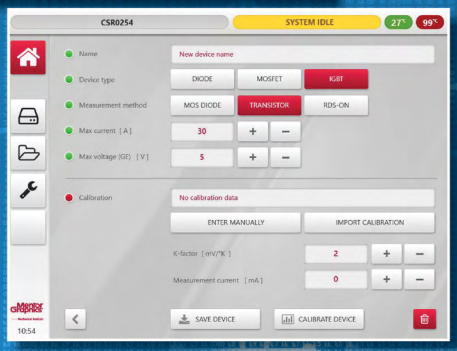

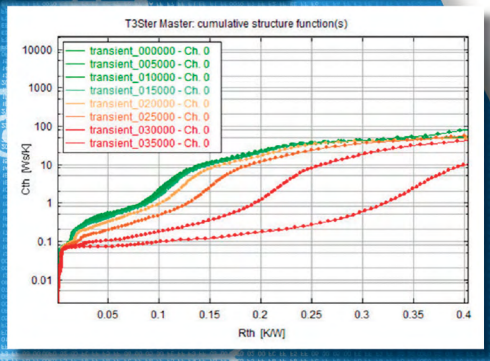

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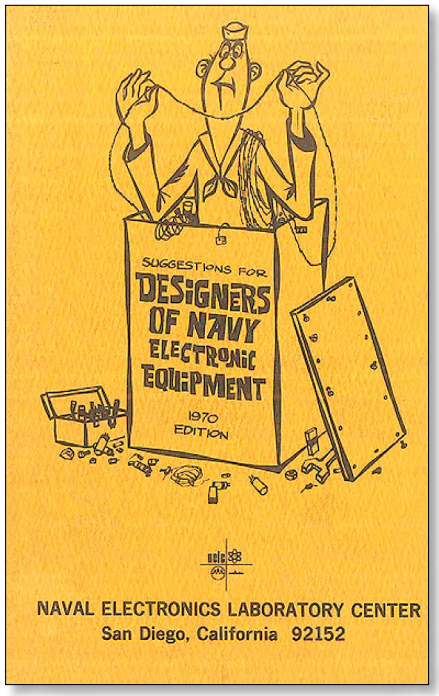
Jim Wilson
Assoc. Technical Editor

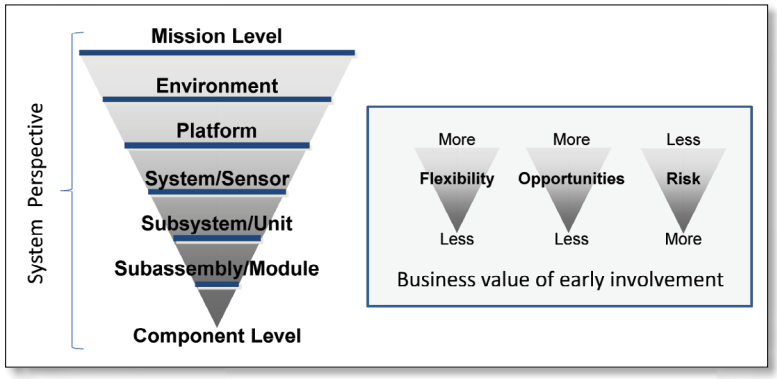
ElectronicsCooling magazine provided a technical data column from 1997 to 2009 with the intent of providing you, the readers, with pertinent material properties for use in thermal analyses. The most common materials and their associated thermal properties used in electronics packaging were covered. Table 1 lists a summary of the technical data columns divided into two categories, thermal conductivity and everything else. It is of note that thermal conductivity was the most frequent topic of interest. This is no surprise as thermal conductivity is one of the most difficult thermal properties to accurately measure. All of this data is accessible on our web site (www.electronics-cooling.com) which also includes all of the articles that have appeared in ElectronicsCooling.

Once most of the relevant thermal properties had been covered, the technical data column evolved into a "thermal facts and fairy tales" feature. This column has covered a variety of topics highlighting some of the typically overlooked or less understood characteristics of thermal management. Table 2 lists the columns in chronological order which are also available on our website. The range of topics suggests that thermal engineers often encounter complicated physics, especially when trying to match test data to predictions.

Our hope as editors is that you find these topics useful. We are always interested in feedback from our readers so feel free to contact us with your ideas and topics, especially if you have a particular thermal fact or fairy tale. This also provides an opportunity to remind the readers of how we work as an editorially independent publication. For each issue, one of the associate editors assumes the role of editor-in-chief and is responsible for either soliciting new technical articles or selecting previously submitted articles that have gone through a review process and been judged worthy of publication. The review process requires at least two favorable evaluations from independent reviewers based on criteria including technical relevance and soundness, interest to our readership, absence of commercial content, and confirmation that the work has not been previously published. We frequently receive inquiries similar to "I could provide content along the lines of …, would you be interested and/or commit to publishing this?". While we welcome the dialogue, a typical response reminds the writer that we need an article to review and that we cannot commit to publication prior to the review process. However, we never want to discourage interest in publishing and we will certainly work with potential authors to help them develop their articles.



FROM ***HISTORICAL SUGGESTIONS FOR THERMAL MANAGEMENT OF ELECTRONICS:*** May 2014



FROM ***EVOLVING THE ROLE OF THE THERMAL ENGINEER FROM ANALYST TO ARCHITECT:*** December 2013 - Levels of Thermal Management Interaction with Product Development

Topic: Thermal Conductivity	Issue	Author[1]
Pure Metals	Jan '99	C.L.
Leadframe Materials	May '97	C.L.
Liquid Metals	May '08	C.L.
Alloys	Feb '07	J.W.
Solders	Aug '06	J.W.
Silicon (erratum in Sept '98: p12)	May '98	C.L.
Various Silicon	May '06	C.L.
III-V Semiconductors	Feb '06	J.W.
Aluminum Oxide	May '99	C.L.
Ceramics	Sept '99	C.L.
Composite Materials	Jan '00	C.L.
Pyrolytic Graphite	Aug '02	J.R.
Silicon Dioxide	Aug '04	C.L.
Unfilled Plastics	May '01	C.L.
The Anisotropic Thermal Conductivity of Plastics	Aug '01	J.R.
Filled Plastics	May '09	C.L.
Rubbers/Elastomers	Nov '01	C.L.
Thermal Insulators	May '02	C.L.
Fluids	Sept '00	C.L.
Gases	Sept ' 98	C.L.
Air	Feb '01	C.L.
Air at Reduced Pressures and Length Scales	Nov '02	C.L.
Moist Air	Nov '03	C.L.
Various Topics		
Heat Transfer Coefficients	Jan '97	C.L.
The Coefficient of Thermal Expansion I	Sept '97	C.L.
The Coefficient of Thermal Expansion II	Jan '98	C.L.
The Relationship Thermal-Electrical Conductivity	May '00	C.L.
Glass, Physical Properties and Categorization by Compounds	Feb '03	J.R.
Thermal Capacitance	May '03	C.L.
Emissivity in Practical Temperature Measurements	Aug '03	J.R.
Surface Flatness	May '04	J.R.
Diamond, Synthesis and Physical Properties	Feb '02	J.R.
Thin Wires: Criteria of Choice	Aug '05	C.L.
Seebeck Coefficient	Nov '06	C.L.
Phase Change Materials	May '05	J.W.
Thermal Diffusivity	Aug '07	J.W.
Thermal Effusivity	Nov '07	C.L.
Viscosity	May '07	C.L.
Building Materials	Feb '08	J.W.
Heat of Vaporization	Aug '08	J.W.
Emissivity in Practical Numerical Modeling	Nov '08	C.L.
Antifreeze Coolants	Feb '09	J.W.

[1]C.L. = Clemens J.M. Lasance, Associate Editor, Philips Research Laboratories
J.R. = Jukka Rantala, Associate Editor, Nokia Research Center
J.W. = Jim Wilson, Associate Editor, Raytheon Company

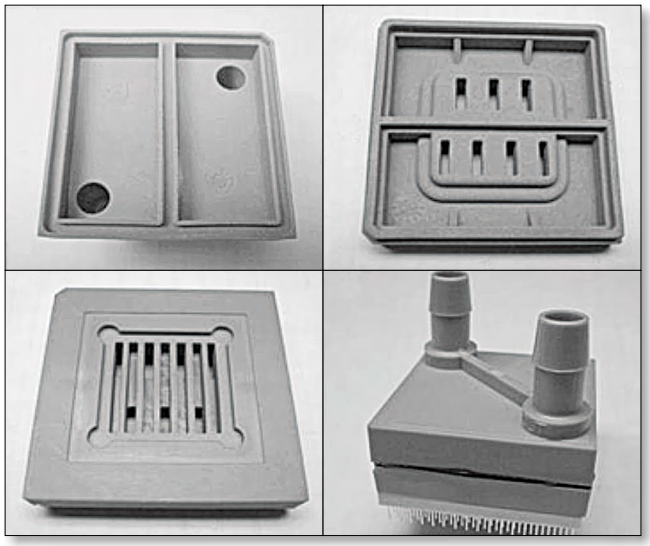
TABLE 1: Technical Data

To view all past columns, visit www.electronics-cooling.com.

Title	Issue	Author[1]
Most of Us Live Neither in Wind Tunnels nor in the World of Nusselt	April '10	C.L.
Uncertainty is Assured	July '10	J.W.
Fully Developed Channel Flow: Why is Nu Constant?	Sept '10	C.L.
Fixed Temperature and Infinite Heat Sinking	Dec '10	J.W.
Published Thermal Conductivities Values: Facts or Fairy Tales	Mar '11	C.L.
Consistency and Accuracy in Simulations	June '11	J.W.
Does Your Correlation Have an Imposed Slope?	Sept '11	C.L.
Heat Sinks, Heat Exchangers, and History	Nov '11	J.W.
Heat Spreading Revisited	Mar '12	C.L.
Time Dependent Responses and Superposition	June '12	J.W.
The Temperature Dependence of the Specific Heat	Sept '12	C.L.
Not Always Efficient	Dec '12	J.W.
Are Critical Heat Fluxes of LEDs and ICs Comparable	Mar '13	C.L.
A System Perspective for Electronics Cooling	June '13	J.W.
How Useful are Heat Sink Correlations for Design Purposes	Sept '13	C.L.
Evolving the Role of the Thermal Engineer from Analyst to Architect	Dec '13	Guest Authors
Historical Suggestions for Thermal Management of Electronics	May '14	J.W.
Virtual Prototyping	Sept '14	P.R.
Moist Air and Cooling Electronics	Dec '14	J.W.

[1]C.L. = Clemens J.M. Lasance, Associate Editor, Philips Research Laboratories
J.W. = Jim Wilson, Associate Editor, Raytheon Company
P.R. = Peter Rodgers, Associate Editor, The Petroleum Institute

TABLE 2: Thermal Facts and Fairy Tales



FROM A SYSTEM PERSPECTIVE FOR ELECTRONICS COOLING:
June 2013 - Microchannel cooling for an IC

Design Optimization of a Multi-Device Single-Phase Branching Microchannel Cold Plate

Ercan M. Dede
Toyota Research Institute of North America

INTRODUCTION

SINGLE-PHASE LIQUID COOLING is an established approach to the thermal management of highly-reliable hybrid vehicle power electronics. However, as the electrification of hybrid vehicles increases, and under-hood space becomes further constrained, semiconductor device power densities continue to rise (in excess of 200 W/cm^2) resulting in significant thermal management challenges. In response to this trend, there is sustained interest in the development of more compact, higher-performance cold plates for single-phase liquid cooling.

Fractal or branching microchannel flow networks have been identified to offer several advantages including low flow resistance [1], reduced channel wall temperatures [2], and greater overall cold plate temperature uniformity [3]. Generally, these performance benefits equate to lower system pumping power and better electronics temperature regulation. At the same time, a strategy to increase heat transfer in a more compact space is to stack multiple coolant channel layers for increased surface area and reduced unit thermal resistance [4, 5].

Building off of these two research directions, a single-device multi-pass branching microchannel heat sink was developed previously through the use of numerical gradient-based optimization techniques [6]. In this article, the design optimization of a related single-phase cold plate for the cooling of 12 large-area planar devices is briefly reviewed, and the fabrication and experimental testing of a prototype structure is described. The single-device cold plate geometry considered in [6, 7] is exploited as a periodic cooling cell in the development of a larger multi-device cooler, as described in [8], that also incorporates optimized global inlet and outlet manifold structures.

Ercan M. Dede received his B.S. degree and Ph.D. in mechanical engineering from the University of Michigan and a M.S. degree in mechanical engineering from Stanford University. Currently, he is a manager in the Electronics Research Department at the Toyota Research Institute of North America. His group conducts research on advanced vehicle electronics systems including power semiconductors, advanced circuits, packaging, and thermal management technology. He has over 20 issued patents and more than 30 articles in archival journals and conference proceedings on topics related to design and structural optimization of thermal, mechanical, and electromagnetic systems. He is an author of a recently published book entitled 'Multiphysics Simulation: Electromechanical System Applications and Optimization.'

COLD PLATE DESIGN AND FABRICATION

A sectioned perspective view of the multi-layer branching microchannel cold plate is shown in Fig. 1, where 12 local cells are placed in a periodic array for the cooling of multiple electronic devices; a cooling cell comprises microchannels arranged into two (Layer 1 and Layer 2) heat exchange passes. The optimal coolant flow paths used to develop the cold plate geometry are shown in the upper images of Fig. 1 using normalized fluid velocity vectors; note that larger velocities are shown in red. The branching channel flow maps, upper left and center images in Fig. 1, are obtained using a multiphysics topology optimization technique [6, 7], where the channel networks are found by minimizing an objective function comprising two terms related to the average temperature and fluid power dissipated in an assumed design domain. The optimization results serve as templates in the synthesis of the Layer 1 and Layer 2 microchannel designs. Alternatively, the Layer 3 (outlet) and Layer 4 (inlet) manifolds with wavy wall shape, upper right image in Fig. 1, are optimized for uniform fluid flow to the local cooling cells with minimum pressure drop [8, 9].

In the lower image in Fig. 1, the blue arrows indicate that the coolant enters through the vertical inlet of the cold plate at the right end. The coolant then travels horizontally through the inlet manifold and is evenly distributed in parallel via the first six jet nozzles to local microchannel cooling cells. From there, the coolant flows into the local

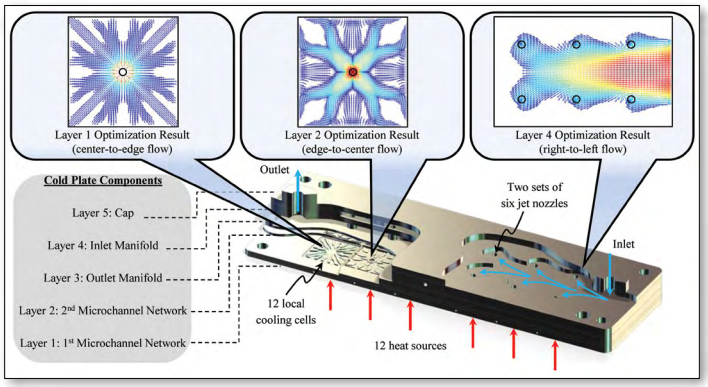


Figure 1 - Sectioned perspective view of multi-pass branching microchannel cold plate for cooling 12 electronic devices (lower image © [2014] IEEE. Reprinted, with permission, from [8]). Normalized fluid velocity vector flow maps (upper images) from structural optimization studies [6-9] with larger velocities indicated in red.

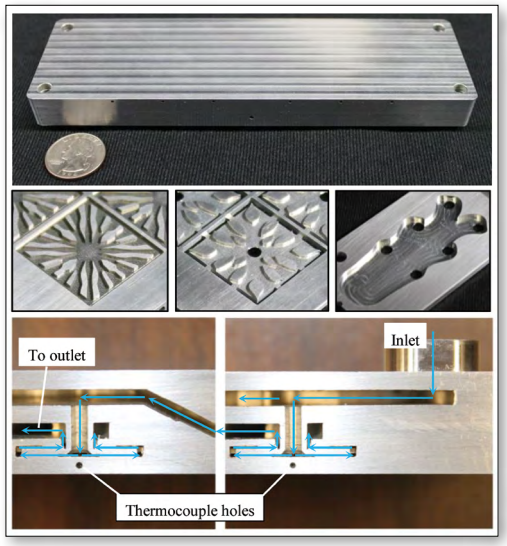


Figure 2 - Fully assembled cold plate (upper image). Zoomed views of Layer 1 and Layer 2 microchannels plus manifold geometry (middle images from left to right, respectively). Zoomed cross section views of the inlet region with a single cooling cell (lower right image) and the middle transition region with a second cooling cell (lower left image). The blue arrows in the lower images indicate the coolant flow path. © [2014] IEEE. Reprinted, with permission, from [8]

Layer 1 (outward flowing) branching microchannel system. The coolant then reverses direction to flow radially inward through the Layer 2 branched microchannel network. Finally, the heated coolant empties into the Layer 3 outlet manifold, and the entire process repeats as two sets of six local cooling cells are connected in series to increase the flow rate to all cells.

The cold plate dimensions are 50 mm x 150 mm x 12.5 mm. Each jet nozzle diameter is 2.5 mm. The third and fourth layer manifold fluid passages are 2.54 mm in height. Layers 1 and 2 have microchannels that are 0.5 mm in height. Each local cooling cell covers a footprint area of 20 mm x 20 mm.

The cold plate is fabricated out of aluminum by precision machining the individual layers and diffusion bonding them to arrive at a unified structure [7]. The end result is a cold plate with minimal interfacial thermal resistance. Figure 2 illustrates the final assembled cold plate with zoomed views of the as-built microchannel/manifold geometry (middle row images) and cross-section (lower row images). The cross-section views show the inlet region of the cold plate (lower right) and a middle section of the cooler (lower left), where the blue arrows denote the coolant flow path and highlight the global flow transition from the first set of six cooling cells to the second set of six cells. Observe in Fig. 2 that a short microchannel height minimizes fin/channel distortion, and the diffusion bonding technique results in a continuous thermal path through the thickness of the assembly. Embedded thermocouple instrumentation holes are centered directly below each local cooling cell jet orifice.

EXPERIMENTAL FACILITY AND PROCEDURE

The experimental facility used for measuring the performance of the cold plate consists of a recirculating chiller, in-line filter, rotary style flow meter, and test section. A standard 50/50 ethylene-glycol/water mix is used in all experiments. The test section comprises a 12-device heater assembly attached to the cold plate plus associated temperature and pressure drop measurement instrumentation. Flow test connectors are utilized to interface with the cold plate and provide for coolant inlet and outlet temperature measurements. A differential pressure transducer is attached to the cold plate via additional taps positioned just after the flow test connectors.

Twelve aluminum nitride ceramic (250 W, 9.4 mm square) resistive devices are solder bonded to a specially designed 3.18 mm thick copper (Cu) plate for the heater assembly, which is bolted to the cold plate with a thermal interface material (TIM) grease layer in between. To determine power dissipation accurately, each device is wired in series to a shunt resistor for precise device voltage drop measurement. Each device/resistor arm is wired in parallel to a 1.4 kW power supply. Temperature measurements are acquired for each local cooling cell using calibrated thermocouples located as shown in Fig. 2. Heater assembly temperatures on the opposite side of the TIM interface are measured at the mid-plane of the Cu plate using thermocouples positioned in line with the cold plate thermocouples. Using a calibrated infrared (IR) camera, the device temperatures are additionally measured; note that the heater assembly is coated with high emissivity flat black paint for accurate thermal imaging.

Steady-state thermal-fluid performance of the cold plate is evaluated over multiple test runs at an elevated coolant inlet temperature. Coolant flow rates ranging from 0.5 to 2.5 l/min in 0.5 l/min increments are used. The supplied heater power is adjusted at each flow rate to achieve a maximum heater device temperature of ~125 °C (as verified via IR camera). Additional details regarding the test setup and experimental procedure are found in [8].

EXPERIMENTAL RESULTS

Figure 3 shows a representative thermal image of the heater assembly and devices taken at the maximum coolant flow rate of 2.5 l/min. The corresponding bar chart in Fig. 3 shows the experimentally measured cold plate, heater plate, and device average temperatures for each numbered cell in the IR image. The bar chart indicates that the cold plate temperatures are uniform to within 3.6 °C. A periodic trend in the heater temperatures is observed between the first row of device positions (i.e., 1-6) and the second row of positions (i.e., 7-12). Logically, heater temperatures closer to the bolts (i.e., positions 1, 6, 7, and 12) exhibit lower values due to reduced grease layer thermal resistance and possible heat sinking effects from the bolts. In Fig. 3, device 4 limits the total input power to the system with a maximum temperature of 127.4 °C. Positions 2, 4, and 5 have a larger temperature differential between each device average temperature and corresponding heater temperature indicating that the large-area solder bond layers for these devices likely contain well-known process-induced voids [10] leading to increased thermal resistance; see [8] for additional discussion.

After post-processing the experimental data by calculating the device power and performing a system energy balance, the cold plate convective thermal resistance is determined. Specifically, the device power is found by calculating the current using the known shunt resistance and corresponding measured voltage drop. A system energy balance is then performed to determine the power lost to the ambient environment (i.e., power in minus power out). The total input power to the system is the sum of the measured power to each device. The power carried out of the system by the coolant is determined using the known coolant specific heat capacity, measured coolant outlet-to-inlet temperature difference, and measured system mass flow rate. The thermal resistance of each cooling cell is then calculated by dividing the measured cold plate temperature minus coolant inlet temperature difference by the known device power (adjusted for power losses). The inlet temperature to the entire cold plate is used to calculate the thermal resistance of the first six cooling cells, while the inlet temperature to the second set of six cooling cells is specified as the cooler inlet temperature plus one-half of the rise in liquid temperature as measured from inlet to outlet. The reader is referred to [8] for additional details.

In Fig. 4, the cold plate thermal resistance (primary vertical axis) and experimentally measured pressure drop (secondary vertical axis) is shown as a function of flow rate with added trend lines. The pressure drop data in Fig. 4 is averaged over two test runs, while the thermal resistance data is further averaged across all 12 cooling cells. A maximum average cold plate thermal resistance of 0.341 K/W with a minimum average pressure drop of 0.59 kPa was determined at the lowest tested flow rate of 0.5 l/min. In contrast, a minimum average thermal resistance of 0.112 K/W with a maximum average pressure drop of 9.03 kPa was measured at the highest flow rate of 2.5 l/min. Explanation of experimental uncertainties and additional design performance verification by simulation is provided in [8].

Direct comparisons of cold plate performance are often challenging due to differences in the end application including the number of power devices, selected coolant, coolant flow conditions, cold plate material selection, and cooler size/packaging constraints. However, a recent investigation of advanced liquid cooling strategies for a representative traction drive application may be used for rough comparison. Specifically, a definition of coefficient of performance (COP) similar to [11] is assumed using only convective thermal resistance. Furthermore, the parallel operation of two branching microchannel cold plates is assumed for cooling approximately the same number of power devices. Based on these assumptions, the multi-pass branching microchannel cold plate is estimated to have a COP comparable to submerged jet-impingement on a microfinned enhanced copper surface, thus outperforming a traditional aluminum channel-flow cooling approach [11]. Here, a COP benefit for the branching microchannel cold plate is realized through relatively low pressure drop at a reduced flow rate.

CONCLUSIONS

This article provided the design and fabrication details of a unique compact multi-device branching microchannel cold plate developed for hybrid vehicle electronics. An experimental facility for measuring thermal-fluid performance was briefly described. Thermal resistance and pressure drop test results were outlined, and the presented cold plate design exhibits favorable performance.

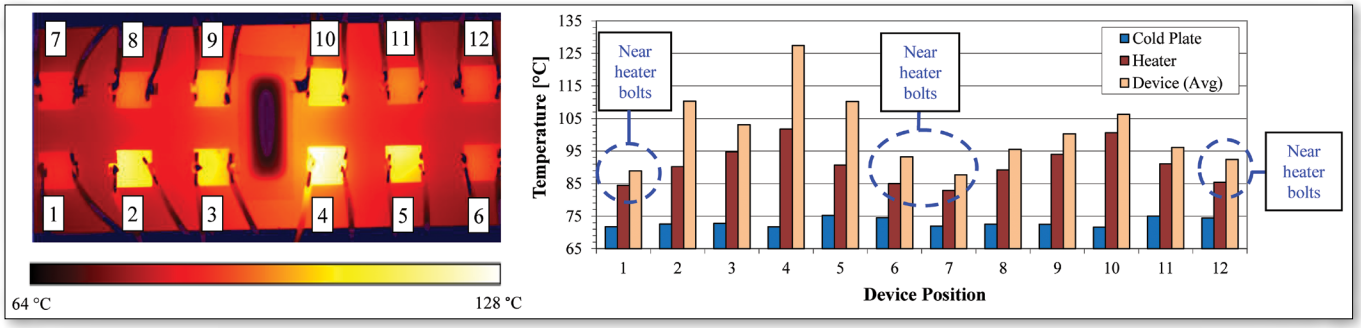


Figure 3 - Representative IR thermal image (on left) from first experimental run at a coolant flow of 2.5 l/min. Bar chart (on right) of cold plate, heater plate, and device average temperatures corresponding to the same test run. © [2014] IEEE. Reprinted, with permission, from [8]

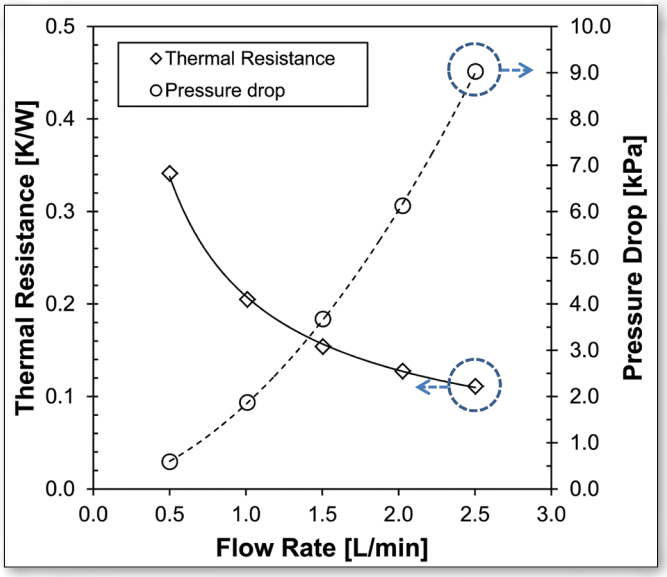


Figure 4 - Cold plate thermal resistance (average of 12 local cooling cells over two test runs) and pressure drop (average over two test runs) shown with trend lines as a function of flow rate.

While the multi-layer construction with remote cooling strategy presented here necessitates diffusion bonding, more integrated layered designs may be achieved at the electronics substrate or semiconductor device level using well established etching and deposition micro-fabrication techniques. Furthermore, the emergence of additive manufacturing technologies may further facilitate direct adoption of more complex three-dimensional cooling strategies in future electronics systems.

From a design perspective, related optimization techniques may be applied broadly to address a variety of topics including, for example, liquid manifold design for two-phase cooling, heat sink design for air cooling, and composite microstructure design for heat flow control in electronics [9]. Thus, the use of optimization methods in the early stages of the product development process holds promise as an approach to the creation of highly efficient electronics thermal energy management solutions.

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Circuit Card Assembly Heat Sinks Embedded With Oscillating Heat Pipes

Joe Boswell[1], Chris Smoot[1], Elliott Short[2], Nate Francis[2]
[1]ThermAvant Technologies, LLC
[2]Raytheon Company

INTRODUCTION

IN THIS STUDY, lightweight two-phase heat sinks embedded with the Oscillating Heat Pipe (OHP) technology are developed for the thermal management of military circuit card assemblies (CCA). OHP-embedded heat sinks efficiently transport heat generated by CCA centrally located components to the assembly's edges. Attention is paid to minimize the size, weight, cost and potential operability penalties associated with the incorporation of the OHP-embedded heat sink, to improve upon existing high performance heat sinks (e.g., Al-Be composites, encapsulated annealed pyrolitic graphite, or outfitted with Copper-Water heat pipes). This article provides a brief update on current OHP technology and summarizes initial findings from prototype OHP-embedded heat sinks.

Joe Boswell is co-founder and CEO of ThermAvant Technologies where he leads the firm's general affairs and has been Principal Investigator on a half-dozen government sponsored heat transfer research efforts. Prior to ThermAvant, Mr. Boswell was the founding CFO of InsideTrack, Inc. and before that an investment banker at JPMorgan's M&A Group. He is a graduate from the University of Pennsylvania's dual-degree M&T program; a member of the Association of Energy Engineers and ASHRAE; LEED EB certified; and co-inventor of ThermAvant's one approved and three pending patents.

Dr. Christopher Smoot (Senior Thermal Engineer, ThermAvant) leads many of ThermAvant Technologies' mechanical and thermal design efforts including finite element modeling and computational fluid dynamics simulations. In 2013, Christopher earned his PhD at University of Missouri-Columbia. Christopher has authored or co-authored seven publications related oscillating heat pipes including "Experimental Investigation of a Three-Layer Oscillating Heat Pipe, 2014, ASME Journal of Heat Transfer, "Thermal and Visual Observation of a Hybrid Heat Pipe," 2013, Heat Transfer Research, and "Robust Thermal Performance of a Flat-Plate Oscillating Heat Pipe during High-Gravity Loading," 2011, ASME Journal of Heat Transfer.

Dr. Elliott Short is a Raytheon Engineering Fellow responsible for designing, developing, and testing thermal management systems. He earned a BSME from the University of Texas at Austin in 1973, a MS in Mechanical Engineering and a MS in Aeronautical Engineering from the University of Arizona in 1977, and a Ph.D. in Mechanical Engineering at SMU in 1994. He is a registered Professional Engineer in Texas, an ASME Fellow, and an AIAA Associate Fellow.

Nate Francis is a Lead Hardware Engineer responsible for design, build, and integration of cutting edge electronics. He earned a BSME in 2003 and a MSME in 2005 from Texas Tech University.

BACKGROUND

OHPs (or Pulsating Heat Pipes, PHPs), Figure 1, were invented by Akachi in 1990 [1] and first considered for adoption in electronics cooling applications in the early 2000's [2]. They are passive two-phase cooling devices made from capillary-sized tubing that meanders in a closed- or open-loop channel pattern. This channel pattern is evacuated and partially charged with a working fluid and hermetically sealed. Heat is transferred by the working fluid's latent and sensible heat as vapor bubbles expand, contract, and in turn oscillate the liquid slugs. No wick structures are involved. OHP-embedded heat sinks have proven capable of transporting kilowatt-level heat loads at effective thermal conductivities greater than 30kW/m-K [3]; and have proven reliable when operating in adverse gravity fields (e.g. up to 10g) [4]. Despite these attractive features, OHPs are not yet widely applied in electronics thermal management due to: perceived high costs, lack of predictability or information regarding reliability, and difficulty functioning at low temperature differentials (e.g., less than 15°C) [5].

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HEAT TRANSFER MECHANISM

While OHPs are passive cooling devices, they operate like active, fluid-pumped devices wherein the kinetic energy of the fluid comes from the thermal energy of the heat source(s) themselves. When at rest (i.e., uniform temperatures across the unit), a well-designed OHP distributes its working fluid as a chain of liquid slugs and vapor bubbles throughout its channel pattern. OHPs start-up when a temperature differential is applied by heat sources (or heat sinks) and cause partial evaporation of nearby slugs (or condensation of bubbles). The fluid's phase change results in volume and pressure differentials which in turn force the slugs and bubbles from relatively warm, high pressure areas (evaporators) toward cooler lower pressure ones (condensers) where a portion of the incoming bubbles condense, reject latent heat, and contract. The relatively cool fluid originally in the condensers is dislodged toward the evaporators through the channel pattern's 180-degree turns. These movements disrupt (or oscillate) the working fluid chain, and new liquid slugs move into the evaporators, and the cycle repeats. Thus, OHPs utilize both the sensible (liquid flow) and latent (evaporation and condensation) heat of the working fluid. OHPs sustain this dual-mode heat transfer as long as the high-frequency phase change events continually disturb the system's equilibrium; and working fluid temperature is sufficiently above its triple point (to maximize saturation pressure differentials and minimize liquid viscosity and density) yet below its critical point (to maximize surface tension and volume differentials of phase change events).

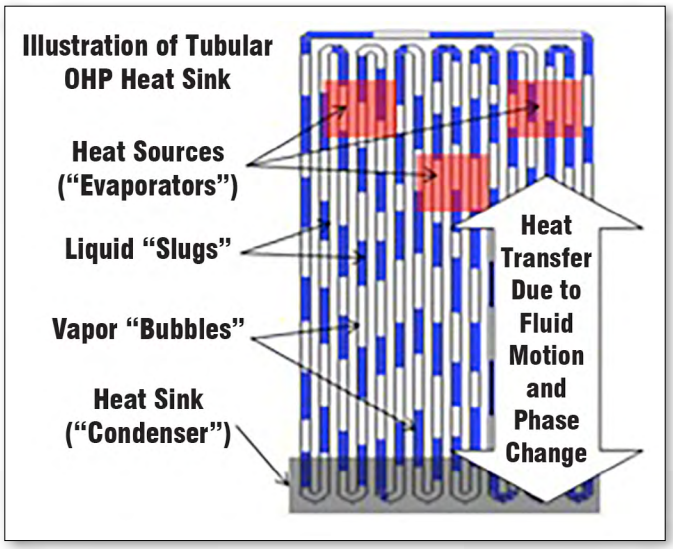


Figure 1 - Illustrated OHP with a chain of liquid slugs and vapor bubbles inside an 8-turn, closed-loop channel pattern.

Figure 2a - 6U sized (2mm thick) OHP heat sink with exposed closed-loop channel pattern.

Figure 2b - 25 x 12 x 1 mm3 Cu heat spreader

Figure 2c - 100 x 30 x 2mm3 Mo OHP micro-chip carrier

Figure 2d - 750 x 114 x 2mm3 Al OHP for heat recovery unit

MANUFACTURABILITY

Ongoing research and development is being conducted not only on OHP design and modeling but also on reliable, affordable production methods to manufacture OHPs that are integral to the base material and delivered in either flat plate and/or three-dimensional form factors. OHPs have been successfully built with thicknesses varying from 0.75mm (0.030") to 40mm (0.25"); lengths ranging from 25mm (1") to greater than 750mm (30"); manufactured from a variety of materials including Al, Cu, Ti, Mo, AlN, *etc.*; and paired with working fluids including water, acetone, common HCFCs, and nano-fluid derivatives of such fluids. Most lab-scale OHPs are made from meandering tubing that is sealed and charged with working fluid; however real-world applications require the OHP to be embedded into a flat-plate, Figure 2, or an even more complex three-dimensional shapes.

DESIGN AND PREDICTABILITY

An all encompassing mathematical model of OHPs' underlying thermo-physical events that enable their fluid oscillations and high heat transport capabilities has been an elusive goal of researchers since Akachi's invention 25 years ago [7-13]. To manage the scope of this article, a brief introduction of key OHP design variables and a simplified method for estimating the affects of embedding an OHP inside a thermal module's base material are presented.

Two primary factors in designing an OHP are: 1) working fluid selection; and 2) channel pattern design. The working fluid is selected based on its thermophysical properties, compatibility with desired heat sink material, and the heat sink's expected operating conditions (e.g., temperatures, heat loads, gravitational fields, *etc.*). Functional charging ratios vary from 10% to 90% of the OHP channel pattern's empty volume [6]. The OHP's channel pattern design considerations include: geometric constraints (e.g. external dimensions, through holes, *etc.*); turn-number [14]; relative location of heat source(s) and sink(s); manufacturing methods available for selected material; and (most notably) channel diameter such that the working fluid's surface tension [15] and wetting of the material's walls [16] maintain the chain of discrete liquid slugs and vapor bubbles.

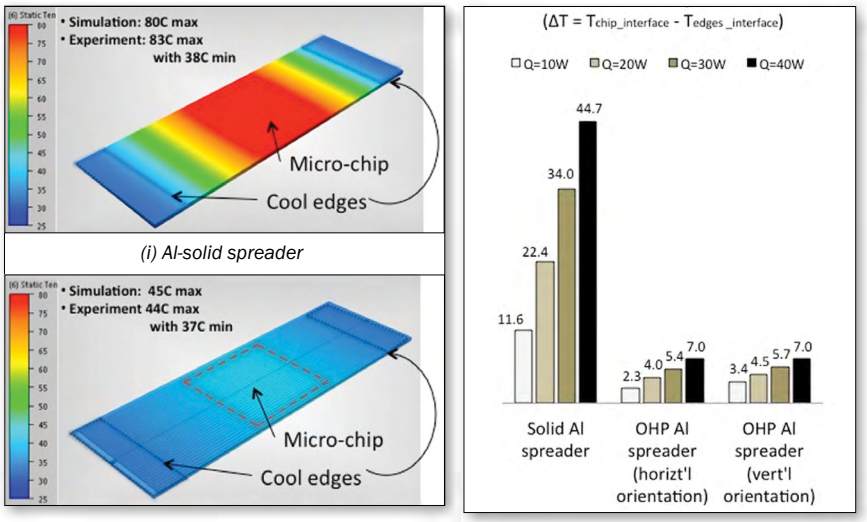


Figure 3 - Thermal comparison of Al-Solid vs OHP-embedded heat spreaders.

Once the OHP designer has completed selection of the working fluids, design of the internal channel pattern, and numerical modeling of the OHP's evaporator-to-condenser thermal resistance (if such modeling is practical), a simplified Finite Element Modeling (FEM) approach can be used to estimate the OHP's impact on the application's overall thermal resistance. For steady-state modeling, the key thermal properties to customize are axial and radial thermal conductivities ($k_{thermal}$) which can be deduced from the finite element model – or by referencing empirical results from similar OHP-embedded applications. Figure 3a is an example of how a simplified FEM approach can be used to reasonably predict an OHP's effect on a module's thermal performance. Figure 3(a,i) shows the predicted steady state temperatures of a solid Al heat spreader with three-dimensional kthermal of 167W/m-K; and figure 3(a.ii) an OHP-embedded Al heat spreader of equal dimensions and base material but embedded with a channel pattern with an axial-wise kthermal 5kW/m-K and a radial kthermal of 1W/m-K. Both units were simulated when attached to a 40W central heat source and two cold blocks at the units' distant edges. Simulations predicted solid Al heat spreader maximum temperature of 80°C (or 44°C above its cold block interface); and the OHP-embedded unit's maximum temperature of 45°C (or 7°C above its cold block interface). Prototype units were then fabricated and experimentally measured with a centrally located heat source and two cold blocks on each edge to match the operating conditions used in the simulations. The OHP unit was tested in both horizontal and vertical orientations to evaluate performance through a 1g field. Experimental results presented in Figure 3(b) closely match FEM predictions: at 40W of input heat, the solid Al unit's measured maximum temperatures varied from 83-84°C (45°C above its cold block interface temperatures); and the OHP unit's measured maximum temperatures were 44-45°C (7°C above its cold block interface temperatures) in both horizontal and vertical orientation. This modeling approach has proven predictive in other development efforts, including CCA heat sinks.

FIELDED APPLICATION

Based on the OHP's inherent thermal features and recent manufacturing and design advancements, prototype OHP-embedded heat sinks have been produced for high power density military platform CCAs. In Figure 4 the top diagram illustrates the basic arrangement of the CCA and prototype heat sink which is comprised of a Bottom Unit and Top Unit that sandwich the CCA to acquire heat from the CCA's devices and then conduct it to the Bottom Unit's rails. Heat is rejected by the Bottom Unit's rails which are in contact with the ultimate heat rejection medium (e.g. pumped liquid, forced air, *etc.*).

Prior to prototyping, FEM predictions of a solid Al unit performance were compared to an OHP-embedded model. These initial models predicted that if the embedded channels assumed an axial-wise effective thermal conductivity of 1kW/m-K, then the maximum temperatures at the heat sink would drop by 2.5°C (compared to solid Al); and if the channels reached a 10kW/m-K effective thermal conductivity then the maximum temperatures would drop by 6.2°C. These levels of channel volume effective $k_{thermal}$ are within the bounds of previously achieved results of prior efforts of the authors (Figure 3) and other researchers [3, 5, 8, 17].

With these targets in place, prototype Bottom Units and Top Units were fabricated, both from solid Al 6061 ($k_{thermal}$ = 167W/m-K) and from Al 6061 embedded with OHP channels as shown in Figure 4. The per unit price of the OHP-embedded units compared favorably to alternative high performance heat sink solutions.

Initial test results for the thermal characterization of the OHP-embedded heat sink are presented in Figure 5(b.ii) with the corresponding performance of the Al-Solid sink given in figure 5(b.i). Figure 5(a) shows the locations of the heat sources (test cards 1 and 2) and of the thermocouples (TCs) measuring the surface temperatures of the heat sinks. In all tests, the total power dissipated by the test cards was 80W, and the heat dissipated through the heat sink into the cold blocks which were cooled by incoming 20°C coolant. The Al-Solid heat sink assembly was tested repeatedly to set a baseline (or control) for the OHP-embedded heat sink's performance. Both the Al-Solid heat sink and OHP-embedded heat sink had similar boundary conditions (e.g.

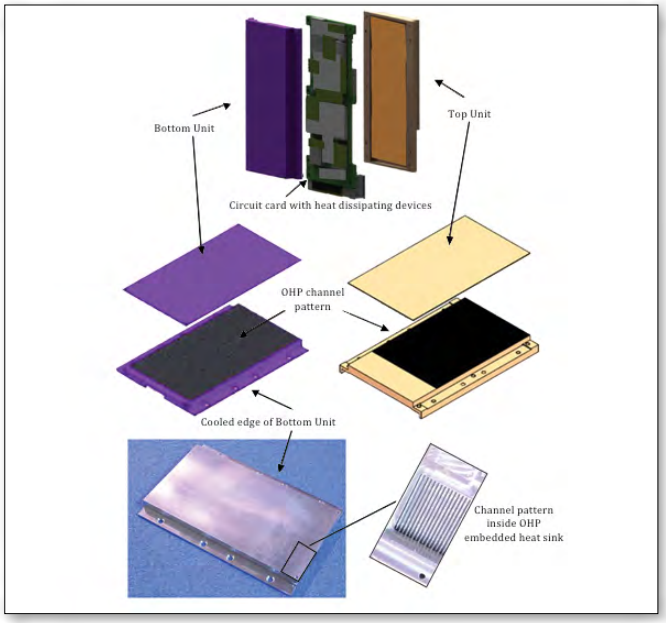
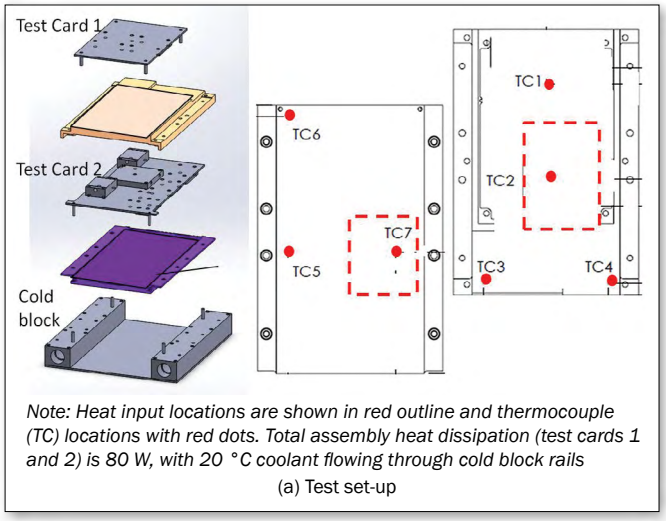
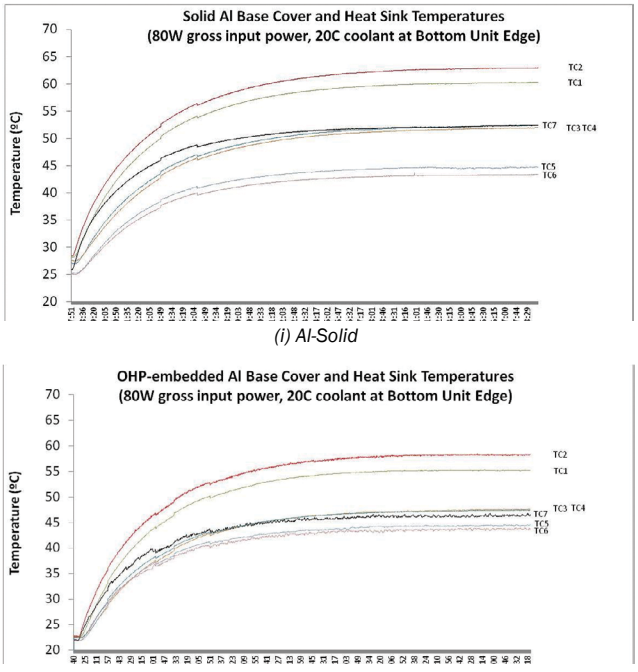


Figure 4 - Cold plate thermal resistance (average of 12 local cooling cells over two test runs) and pressure drop (average over two test runs) shown with trend lines as a function of flow rate.



Note: Heat input locations are shown in red outline and thermocouple (TC) locations with red dots. Total assembly heat dissipation (test cards 1 and 2) is 80 W, with 20 °C coolant flowing through cold block rails

(a) Test set-up



(b) Measured heat sink temperatures during 30-minute tests

Figure 5a-b - Measured thermal performance of Al-solid versus Al OHP heat sink.

lowest measured surface temperatures on Bottom Unit near the cold block interface were 43° and 44°C, respectively).

From Figure 5(b.ii), the OHP-embedded heat sink had a 5°C lower maximum temperature than the solid Al heat sink. The performance increase of the OHP was attributable to the 67% lower thermal resistance across the Bottom Unit's surfaces. The temperature difference (dT) between the Bottom Unit's hottest location (TC7) to its coolest (TC6) reduced from 9°C in the solid Al unit to 3°C in the OHP embedded unit; and the working fluid's oscillations are evident in the second-to-second temperature variations (i.e., the OHP's TC7 varied by +/- 0.30°C over last 100 readouts whereas the solid control only varied by +/- 0.05°C over its last 100 readouts). On the other hand, the OHP in the "Top Unit" had minimal temperature improvement across its surfaces when compared to the solid Al unit. Both solid and OHP Top Units had temperature rises of 11°C across their surfaces (i.e., as measured from hottest location (TC2) to the coolest location (TC4) on the Top Unit). Oscillations are evident in the second-to-second temperature profiles of the OHP Top Unit (i.e., TC2 varied by +/- 0.2°C over its last 100 readouts), though such oscillations and temperature variations were less pronounced than in the OHP Bottom Unit. As of the date of this article, new OHP channel patterns are in development for the Top Unit to address its relatively large temperature rise to lower maximum temperatures across the heat sink by yet another 5°C.

CONCLUSION

OHP technology is maturing as a real-world thermal management solution for engineers to consider as they seek to better control the temperatures across their electronics systems. Whereas OHPs from years past were unable to reliably operate with low temperature differences, today's OHPs can provide outstanding effective thermal conductivity when operating with less than 3°C temperature difference between evaporator and condenser areas while still operating across a range of power levels and gravitational fields. OHPs are especially useful when the spatial distance between one or more heat sources and the heat sink(s) is at least 25mm – and OHPs have been proven effective at lengths as great as 750mm. Recent advancements in manufacturing and design, have enabled OHPs to be embedded inside

a wide range of materials at production costs that are in-line or below (depending on the application) other high performance thermal management technologies. Ongoing research by the authors is investigating how to apply OHP-embedded solutions across range of military platforms and to further research the effects of long-term exposure to extreme thermal, vibration, shock and other environmental conditions.

ACKNOWLEDGEMENTS

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Thermal Power Plane Enabling Dual-Side Electrical Interconnects for High-Performance Chip Stacks

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ABSTRACT - In this article the design and performance of a thermally enhanced laminate called thermal power plane (TPP) is reported. It enables dual-side electrical interconnects to a chip stack and thus supports increased communication bandwidth and power density. In addition, in a two-die stack, all through-silicon vias for power can be eliminated, with the advantage of gained silicon active area. The use of two laminates also allows individual test and burn-in of the dies prior to stack formation.

The TPP must provide efficient heat removal and current feed in the out-of-plane and the in-plane direction, respectively. An 8+1 core-less build-up laminate with aligned and stacked thermal laminate vias (TLVs) was designed and implemented. Rail-shaped solder interconnects join the TPP to the top side of the chip stack, achieving better heat dissipation capability than solder balls. In principle, the solder interface and the TPP with their thermal impedances of 4.8 and 7.4 K-mm^2/W, respectively, represent an electrical functional thermal interface material1 (TIM1) and lid, with a performance that is equivalent to that of electrical non-functional TIMs and lids used in state-of-the-art packages.

INTRODUCTION

VERTICAL INTEGRATION OF integrated circuits (ICs) by through-silicon vias (TSVs) provides the prospect of high interconnectivity and close

proximity of circuit elements in individual tiers. Therefore, compute performance improvements and efficiency scaling can be expected [1, 2].

Current approaches to interface to chip stacks are equivalent to traditional packaging topologies of a single die with single-side electrical interconnects (SS-EIC) at the bottom side and heat dissipation through the top face of the chip stack (Figure 1a). However, the interface area stays constant irrespective of the number of integrated dies, and hence, may not satisfy the power delivery, signaling and heat removal requirements of high-performance chip stacks [3]. Power delivery is a challenge already in current single-die microprocessor packages, requiring up to 80% of the electrical interconnects available [4, 5]. In addition, a large number of power TSVs are needed in the bottom dies of a chip stack, resulting in significant silicon real-estate losses [6, 7].

Therefore, we proposed a novel dual-side electrical interconnect (DS-EIC) packaging concept [8]. The number of EICs to the chip stack can be doubled, and all power TSVs in a two-die stack can be eliminated by means of back-to-back bonding (Figure 1b). The enabling element is an additional laminate assembled at the top side of the chip stack (Figure 1b, orange layer). This element must be capable of providing power, while imposing a low thermal resistance for the heat dissipated to the back-side cold plate. Hence, it is referred to as thermal power plane (TPP). Moreover, the integration of two lami-nates enables individual test & burn-in of dies prior to stack formation.

SINGLE- VS. DUAL-SIDE ELECTRICAL INTERCONNECT BENCHMARK

To demonstrate the benefits of the dual-side EIC approach, a high-performance core–cache stack is considered. The high-power die (250 W, 6.8 cm^2) is placed close to the cold plate to meet the temperature budget available [3]. Therefore, the 16 cores are implemented in the top chip (TC), assembled on the bottom chip (BC) with integrated L3 cache.

An interconnect count analysis considering typical off-chip and core-to-cache interconnect counts was performed to benchmark individual packaging topologies [8]. Five arrangements were compared, namely, single-side (SS) EIC with face-to-face (F2F) and face-to-back (F2B) and dual-side (DS) EIC with F2F, F2B and back-to-back (B2B). The bottom

laminate provides signals and power to and through the BC, whereas the top laminate (TPP) only delivers power to the TC.

The largest numbers of BC TSVs and µ-C4s are required in the single-side F2F case, closely followed by the F2B configuration, as all powering and signaling is performed through the bottom laminate (Figure 2). However, in contrast to the dual-side topologies, those configurations require no TSVs in the TC. The power to the cores in the TC is provided through the TPP in the dual-side EIC, which allows a doubling of the C4 interconnections to the chip stack. However, the dual-side F2F option still needs a large number of TSVs. For the dual-side F2B case, all power and signal TSVs can be separated to the TC and BC, respectively, which would allow an optimized TSV design depending on their functions, while maintaining only one TSV type per chip. The lowest number of TSVs results in the dual-side B2B case: The remaining TSVs only serve signaling purpose. Compared with the SS-F2F option, the silicon real-estate loss in the bottom die for the DS-B2B option can be reduced from 3.7% to 0.4% at a TSV keep-out zone of 30 × 30 µm^2.

DESIGN OF THE THERMAL POWER PLANE

The physical implementation of the dual-side EIC concept relies on three essential packaging elements: 1) the thermal power plane (TPP), 2) elongated solder top interconnects, called rails, and 3) an on-module voltage-regulation module (VRM) (Figure 3a). The TPP needs to be a substrate with excellent lateral power delivery and vertical heat dissipation capabilities so that currents are conducted at minimal voltage drop and the heat is dissipated efficiently to the back-side liquid cold plate (Figure 3b). These two properties can only be achieved at the price of compromised electrical functionality. Hence, in the TPP, only lateral power feed with V_{dd} and GND domains is considered. Signaling and power feed to the bottom chip are provided by the bottom laminate (Figure 1b).

This constraint allows the implementation of a regular array of thermal laminate vias (TLVs) in the substrate without congestion of the signal wires. Copper-filled thermal vias can be achieved in coreless built-up laminates. TLVs are formed by laser drilling and subsequent electroplating. The vias are connected to individual copper planes in the laminate. The current feed capability of the laminate can be adjusted by the number of copper planes implemented, which are separated by organic dielectric layers.

Three different plane patterns are considered: bar, mesh (Figure 3b) and mesh (Figure 4). Bars run straight from one side of the laminate to the other and hence conduct the current only in north-to-south direction. The chevron and

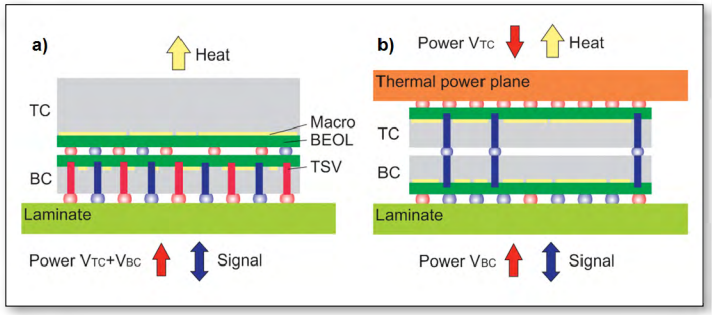

Figure 1 - Cross-sectional view of a module with a two-die chip stack. a) Single-side EIC, b) dual-side EIC. Color coding: red: power, blue: signals, yellow: heat.

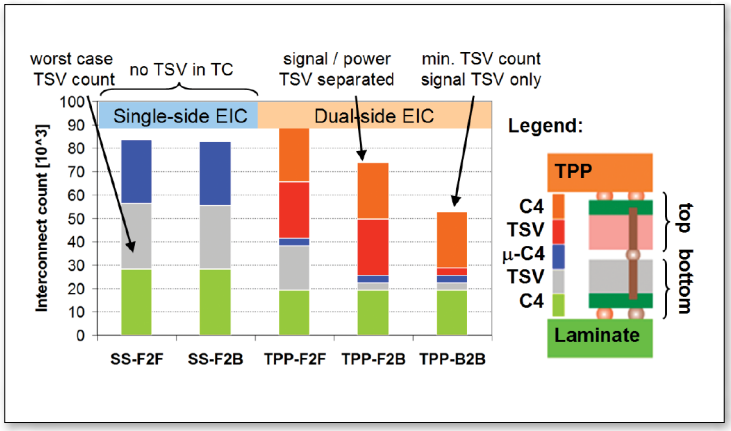

Figure 2 - Interconnect count for the single-side and dual-side EIC options considered.

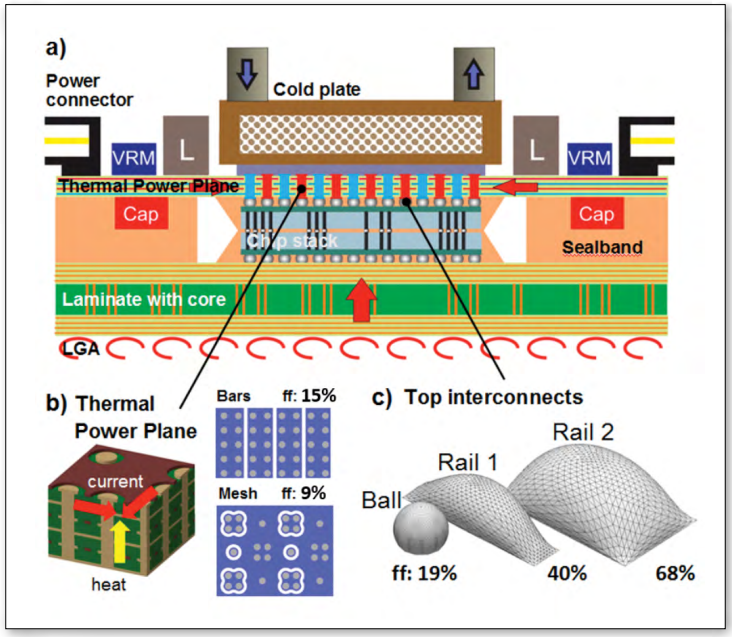

Figure 3 - a) Physical implementation of the dual-side EIC module. b) Thermal power plane topology considering bars and mesh planes. c) Top interconnect options from solder ball-to-rail arrays. (ff: fill fraction)

mesh design in contrast, support two-dimensional current feeding from any in-plane direction. The implementation of solder rails, improves the thermal coupling from TC to TPP [9]. Solder Rail1 spans 3×1 solder ball locations; Rail2 spans 6×2 locations (Figure 3c).

IMPLEMENTATION OF THE THERMAL POWER PLANE

The cross section of the coreless TPP 8+1 laminate with 18-µm-thick copper planes and 33-µm-thick dielectric layers is shown in Figure 4b. The total thickness of the laminate is 400 µm. TLVs with an average diameter of 65 µm are implemented at a pitch of 151 µm. Pairs of via rows are connected to the same domain to comply with the ground (GND) and supply voltage (V_{dd}) patterns of current microprocessors. This is visible in the top view of the outermost copper plane of the laminate (Figure 4a), which will later interface to the cold plate through TIM2. The underlying TLVs cause a change in the color of the copper surface and can hence be identified in pairs. In the thermal zone, solder was applied in the Rail 2 shape (Figure 3c) on the bottom side of the 50×50 mm² TPP laminate (Figure 4c,d).

CHARACTERIZATION OF THE THERMAL POWER PLANE

The effective thermal resistance characterization of the TPP laminates and solder interconnects was performed with a self-made bulk thermal tester [9, 10]. The TPP and solder specimens are wetted on both surfaces with liquid metal to obtain a thermal contact between two copper rods. A uniform heat flux is introduced, and the thermal gradient across the specimen and the heat flux are determined by thermocouples in the rods to derive the thermal resistance of the specimen [11].

As expected from the copper via fill fraction, the effective thermal resistance of the mesh sample (5 vias per unit cell) is with 13.6 K-mm²/W substantially higher than that of the bar and chevron designs with 8 vias per unit cell resulting in close to 8 K-mm²/W (Figure 5, Table 1). Raleigh's derivation, which was used as the analytical model and a finite-element analysis (FEA) were applied to compare the experimental results with the modeling results. Both models correctly predict the experimental values within the error margin of the experiment. Overall, the TPP thermal resistance of 7.4 to 13.6 K-mm²/W outperforms the benchmark of a thick-core laminate with annular thermal vias [12] by three to five times (Table 1).

The thermal characterization of the solder interface resulted in quite a large uncertainty for the low resistances of the Rail1 and Rail2 designs. Hence, the experimental results were again supported with analytical and FEA models (Figure 6). Compared with the solder-ball array, the improvement for the Rail1 and Rail2 designs is twofold and more than threefold, respectively.

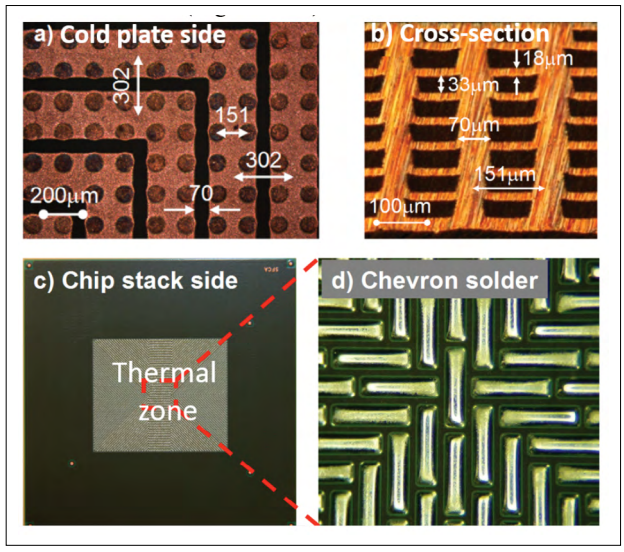

Figure 4 - Photographs of a TPP with chevron design and solder Rail2: micrographs depicting TPP a) top side and b) cross section. c) Bottom view of the entire TPP laminate (50x50 mm²) and d) the close-up of the solder rail array, with rail length and width of 900 µm and 250 µm, respectively.

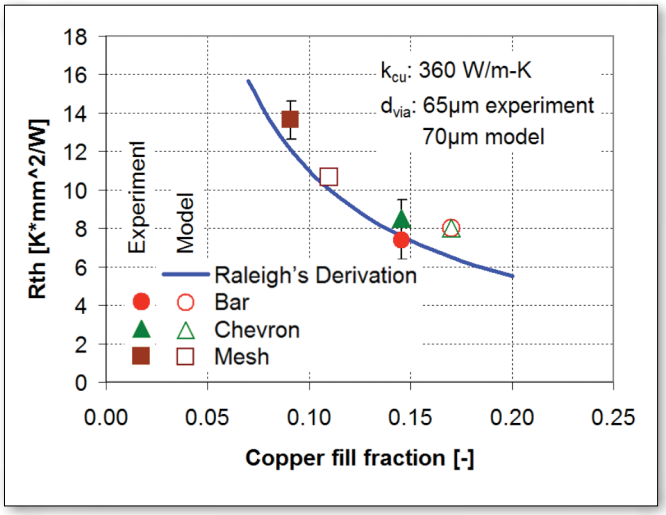

Figure 5 - TPP thermal conductivity of the bar, chevron and mesh type designs: Experimental (filled symbols) and modeling results [empty symbols: FEA; blue line: analytical equation].

Table 1 - Thermal conductivity of TPP laminate. The core laminate with annular vias from [12] is listed as benchmark case.

TPP Type	Copper fill fraction [%]	Thermal resistance [K-mm²/W]	Thermal conductivity [W/m-K]
Bar	15	7.4	53
Chevron	15	8.5	47
Mesh	9	13.6	30
Annular via [12]	9	39.7	34

THERMAL PERFORMANCE BENCHMARKING

A benchmarking study of the thermal performance of the single- vs. dual-side EIC package can be performed with the available measurements (Table 2). For the single-side EIC concept, heat dissipation from top chip to cold plate occurs through the silicon die and a copper lid into the cold plate. The interfaces between the chip and lid and the lid and cold plate are filled with a TIM1 and a TIM2, respectively. In contrast, for the double-side EIC concept, heat needs to be dissipated through the wiring layers of the top chip, the solder bond-line, the TPP, and through a final TIM2 to the cold plate. The lid, TIM1 and silicon die of the single-side EIC package correspond to the TPP, the solder bond-line and the wiring layers of the top chip of the dual-side EIC package. The TPP introduces a slightly higher thermal resistance, which is compensated by the low solder thermal resistance of Rail2-type interconnects. The wiring layers of the top chip impose a similar impedance as the silicon die. In conclusion, the sum of the thermal resistances of the various elements yields a slightly lower thermal resistance in the case of the dual-side EIC approach when bar-like copper planes and Rail2-shaped solder interconnects and a gel-type TIM1 are used, as predicted in [8].

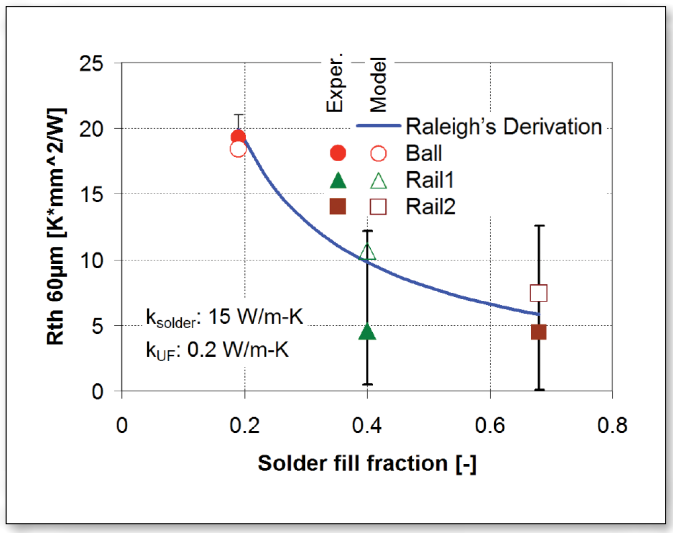

Figure 6 - Experimental and modeled effective thermal resistances of the solder joints of different solder geometries at 60-µm bond-line thickness, resulting in various fill fractions (solid symbols: experiment, open symbol: FEA model; blue line: analytical equation)

Table 2 - Thermal benchmarking of single-side and dual-side EICs. Characteristic elements are described in detail in [8].

Element	Single-side EIC		Dual-side EIC	
	Comp.	Thermal resistance [K-mm²/W]	Comp.	Thermal resistance [K-mm²/W]
Lid	Cu lid 2 mm	5.6	TPP bar 400 µm	7.4
Inter-connect	TIM1 gel	13	Solder Rail2	4.8
Top chip	Silicon 780 µm	5.6	Wiring layer	5.0
Total		24.2		17.9

CONCLUSION

The benefits of the dual-side electrical interconnect topology for a core-on-cache stack were identified. They are

- twice the number of electrical interconnects to the stack, enabling larger off-stack communication bandwidth
- elimination of all power TSVs, freeing up 3.3% silicon area, allowing optimization of the TSV design for signaling and minimization of the need for a re-design of existing macros
- individual test and burn-in of top and bottom chip, followed by stacking of known good dies, with a concomitant yield improvement

The three main elements to implement the dual-side electrical interconnect topology were identified. They are 1) t thermal power plane, 2) solder rails and 3) on-module VRM. The thermal performance of the 8+1 coreless TPP with a thickness of 400 µm and TLVs with a mean diameter of 65 µm at a pitch of 151 µm and the solder Rail2 interconnects was identified to be as low as 7.4 and 4.8 K-mm²/W, respectively. These values are equivalent to state-of-the-art lid and TIM1 components and thus prove the thermal feasibility of the concept.

This article demonstrates the opportunities enabled through advanced thermal packaging in system design and electrical performance of a chip package. We hope we were able to inspire thermal engineers to think in a more holistic approach in order to achieve better performance of the entire system and enable novel functionalities. Why not adding electrical functionality to a lid and to the TIM interface? That's what the TPP and solder rails represent: they are just electrical active lids and TIMs.

ACKNOWLEDGEMENTS

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Liquid Immersion in the Data Center:
A Modular Approach for Cooling High-Performance Microelectronics

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INTRODUCTION

WHILE DATA ENTER ENERGY consumption is already significant, the growth of a global cloud-based economy along with society's need for constant social networking connectivity will cause this number to rise even further. The world's Information-Communications-Technologies (ICT) infrastructure, a general representation of cloud-based computing, is estimated to consume 1,500 TWh of electricity, roughly 10% of global usage [1]. Data center power draws in the U.S. rose from 9,900 MW to 10,560 MW between 2012 and 2013, representing a 7% increase [2]. With the average American household consuming roughly 10,000 kWh of energy annually, the previously cited 2013 number represents nearly 3.8 million homes. Consumer demand for information, only part of why this number is increasing, shows no signs of slowing either. An interesting infographic published by Intel [3] shows how internet traffic is distributed in any given minute. Over 1,500 TB of data is distributed per minute globally with video streaming, primarily in the form of YouTube and Netflix, accounting for half of that traffic. All indications are that demand for social network connectivity and use of streaming video services will grow, resulting in even more requirements for data centers worldwide. The current study seeks to illustrate how data center power density, efficiency and reliability can be increased through the integration of a two-phase liquid immersion cooling approach into a small form factor electronics enclosure meant to simulate a modular high performance server assembly. The results, analyses and conclusions of this work were presented at the 2014 SEMI-THERM conference in San Jose, CA [4].

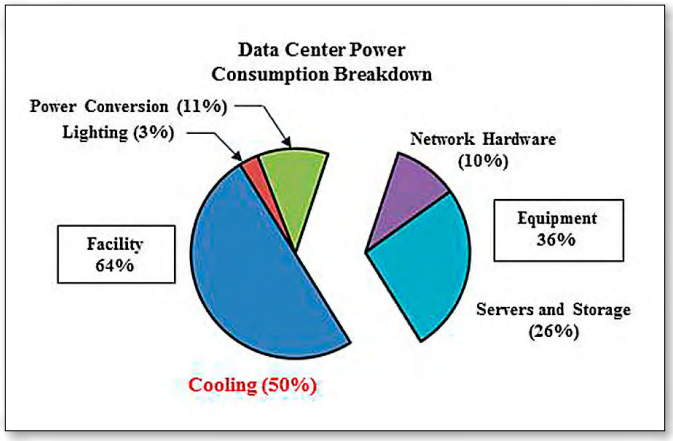

Figure 1 - Chart showing the significant resources a data center dedicates to the thermal management solution employed. [5]

As shown in Figure 1, half of the power consumed by a conventional air-cooled data center is dedicated to the thermal management solution utilized. Two-phase liquid immersion cooling techniques offer the opportunity to reduce cooling power consumption significantly through the use of the orders of magnitude increase in heat transfer coefficients (HTC's) available with this solution [6]. Higher HTC's result in lower thermal resistances, which can play a beneficial role in the overall system efficiency. Increasing the HTC also reduces the driving temperature difference from ambient necessary to remove the heat generated. Reducing this temperature promotes the reliabil-

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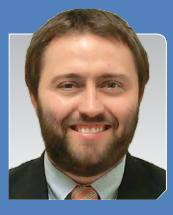

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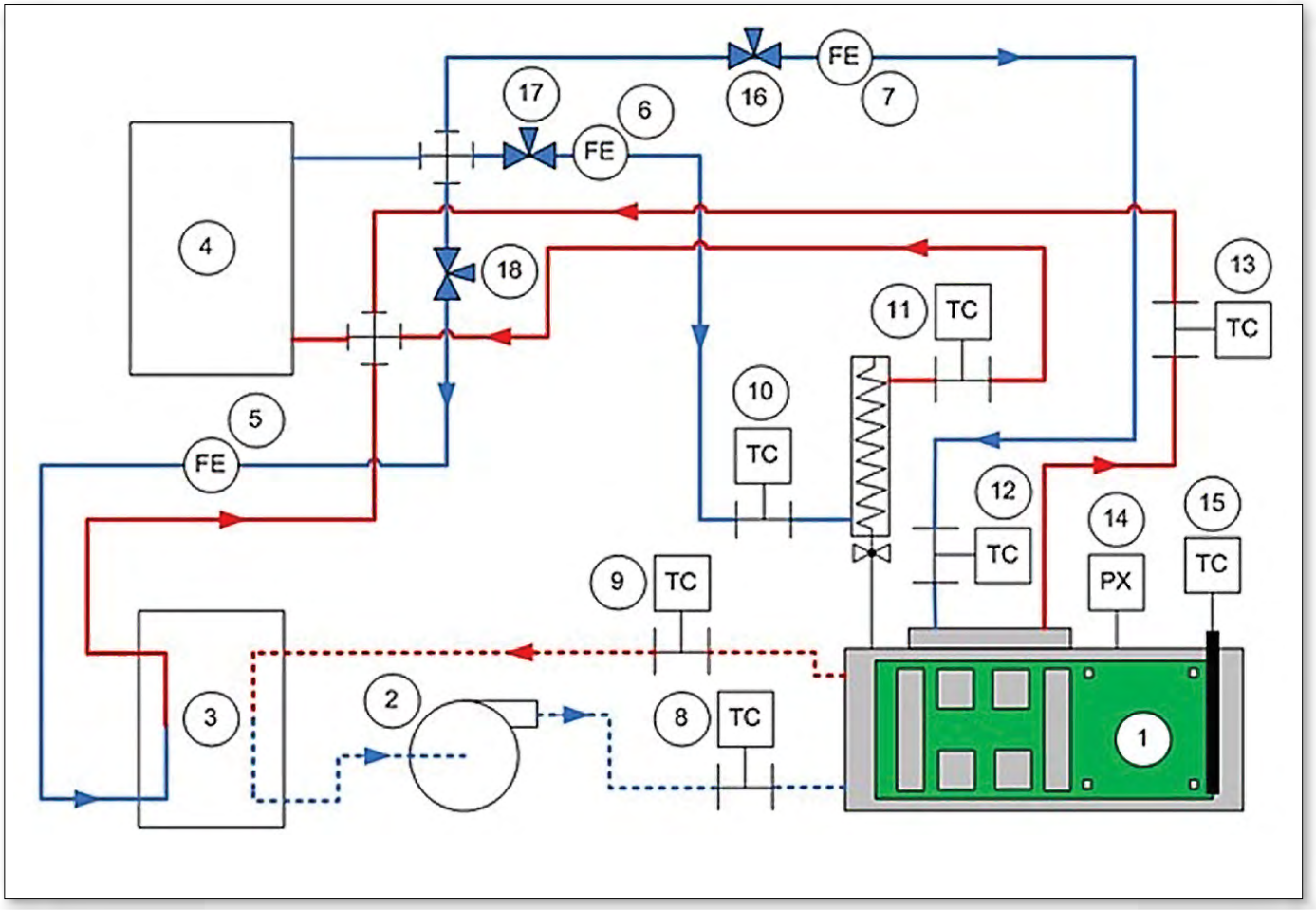
ity of the system as the failure rate of a processor is tied to the chip's operating temperature. These significant increases in heat transfer coefficients are experimentally documented in practical applications with boiling from both bare silicon as well as from microscale surface enhancements attached to the wall of the heated element [7,8]. The translation of these performance parameters to power savings is also well documented. A data center in Hong Kong used dielectric fluids from the Novec family as part of a two-phase immersion solution based on an Open Bath Immersion (OBI) approach. This facility reported a cooling electricity savings of 95% and a Power Usage Effectiveness (PUE) of 1.02 [9]. Using a similar approach, a team of SGI and 3M have partnered to construct a facility to cool the former's ICE X supercomputing hardware [10]. While these two-phase approaches are very much in the development stage, solutions where the immersion coolant is kept as a liquid are mature and commercially available. Companies such as Iceotope, LiquidCool Solutions, and Green Revolution Cooling all offer suitable single phase immersion cooled solutions for current generation computing applications.

EXPERIMENTAL FACILITY

Figure 2 is a schematic of the entire experimental facility used for the current work. The schematic also represents the framework of a liquid cooled data center's coolant delivery system.



LEGEND

Dielectric Fluid Return Line
Dielectric Fluid Supply Line
Chilled Water Return
Chilled Water Supply

1 Experimental Cartridge Assembly
2 Dielectric Fluid Pump
3 Liquid-Liquid HX
4 Chiller
5 CW Flow Meter (HX)
6 CW Flow Meter (GC)
7 CW Flow Meter (CW Header)
8 Thermocouple (DF Inlet)
9 Thermocouple (DF Outlet)
10 Thermocouple (GC Inlet)
11 Thermocouple (GC Outlet)
12 Thermocouple (CW Header Inlet)
13 Thermocouple (CW Header Outlet)
14 Cartridge Gage Pressure Transducer
15 Cartridge Pool Temperature TX
16 Header CW Flow Needle Valve
17 GC CW Flow Needle Valve
18 Liquid-Liquid HX Flow Needle Valve

Figure 2 - Schematic illustrating the primary flow loops and components within the overall experimental setup. [4]

Many of the elements one would find in such an installation are represented here such as a chiller for system level heat extraction, heat exchanger for immersion/external coolant interfacing as well as critical flow characteristic monitoring subsystems. All of these elements are identified within the schematic by the associated Find Numbers (FN's) shown on the table within Figure 2. FN 1 represents the experimental cartridge assembly, the primary component within the facility as it houses the heated elements meant to simulate high performance processing elements. These elements are sealed within an aluminum housing that has dimensions of 150 mm x 300 mm x 38 mm (H x L x W). Located at the top of the assembly is the chilled water header which is directly attached to a 4 x 21 array of fins that protrude down from the top inside face of the housing. The direct attachment is achieved through the machining of the aluminum housing out of a solid aluminum block, thus eliminating the need for a Thermal Interface Material (TIM) attaching the fins to the exterior header channels. This method of manufacture also reduces the number of potential leak points from which the dielectric fluid could dissipate as dielectric fluids have been known to escape from cracks as small as those made by welded joints. The internal fins capture the heat generated by the rising vapor from the boiling elements via condensation. The heat is then conducted into the walls of the chilled water header and subsequently convected away via the flow of an 80/20 by volume mixture of deionized water and Dowtherm SR-1 respectively being pumped through the channels. The chilled water header acts as the primary means by which is heat is removed from the cartridge under pool boiling conditions but can act as a supplement when subcooled dielectric fluid is pumped through the cartridge via the inlet and outlet ports shown to the left of FN 1 on Figure 2. Under this flow boiling scenario, the heat that is gained by the dielectric fluid flowing through the cartridge is extracted from the system by a liquid-liquid heat exchanger that interacts with a second branch of the previously mentioned coolant mixture. All of the facilities chilled water mixture is distributed and maintained to within a 0.1°C set point for all of the experiments conducted within this study by a primary chiller unit, shown as FN 4 on Figure 2. To maintain the intent of modularity in the design and the overall Line Replaceable Unit (LRU) approach, all connectors are of the quick disconnect style from the Colder Products LC Series. In order to maintain a good seal around the visualization windows of the enclosure, EPDM gaskets were used with great success over hundreds of hours of testing for both the Novec 649 and FC-72 fluids used. The fluid inventory sealed within the enclosure is minimal, slightly under 1L for pool boiling conditions. Attention must be paid as well to the sealing of the electrical I/O. Therefore, a Glenair hermetic connector from the 177-705H series was selected for this critical interface. This connector is located on the same plane as the dielectric fluid inlet and outlet ports. It is also important to ensure that the pressure within the electronics enclosure is monitored and maintained within an acceptable limit. Increasing the pressure within the assembly raises the saturation point, or boiling point, of the fluid which in turn increases the temperature necessary to initiate boiling. As mentioned previously, this increase in operating temperature will have a deleterious effect on the overall system reliability. The pressure for the current study is maintained at atmospheric conditions by a vented Graham condenser but, in an actual installation, could be done with a dedicated bellows as well.

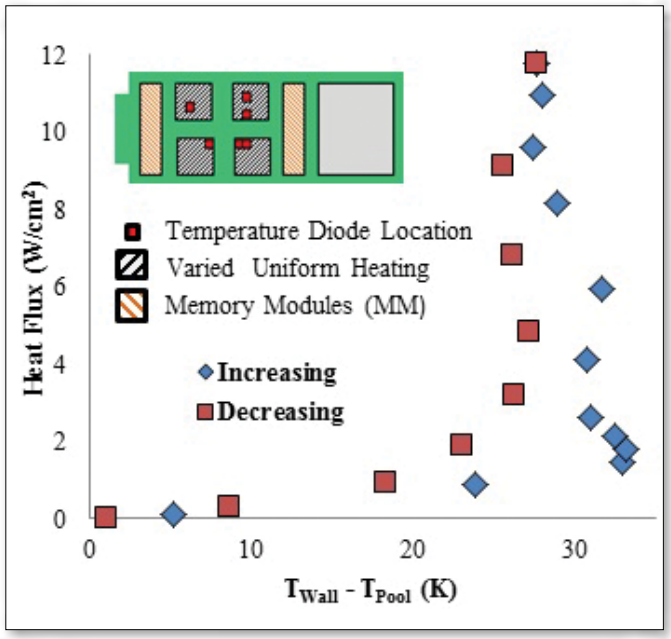


Figure 3 - Plot showing the pool boiling results as heat flux is increased and decreased with FC-72 as the working fluid and 7°C as the facilities chilled water set point. The red squares on the image to the top left of the plot indicate where temperatures were measured for calculation of the average value presented. [4]

POOL BOILING RESULTS

Figure 3 shows the variation of heat flux from the four primary bare silicon die with respect to the driving temperature difference, that between the average surface temperature of the heated elements and the pool temperature. Heat was applied to the elements and temperatures were measured using thermal test cells from the PST4 series by Kokomo Semiconductors. The maximum heat flux achieved is roughly 12 W/cm2. Remarkably, this number was achieved from a bare silicon surface facilitating the integration of any number of Commercial Off-The-Shelf (COTS) available processing elements into the electronics enclosure. The hysteresis one would expect from a traditional pool boiling curve is evident in Figure 3 but with a slight variation. The double hitch is more than likely attributable to two factors. The first is the wide distribution of pore sizes one will find on a bare silicon surface and their consequent variation in activation in accordance with Hsu's model. Secondly, the top die begin nucleation before the bot-

tom die which would cause two distinct hysteretic phenomena as shown in Figure 3. A potentially more useful result was attained when pool testing was extended to four other facilities chilled water set points, namely 11°C, 15°C, 18°C and 22°C, with Novec 649 as the working fluid. Formulation of the data into power dissipated or heat transfer coefficient variation with respect to average surface temperature yielded no noteworthy differences. However, the data was compared to the well-known Rohsenow correlation using a Csf value of 0.0051 obtained from a more conventional pool boiling study [11]. Using this value, which is very close to the 0.0054 value found by Geisler [12] for bare silicon and FC-72, along with the properties shown in Table 1, the Rohsenow correlation predicted the heat fluxes yielded in the fully developed boiling regime from the current study for all of the chilled water set points to within ±40%, a generally accepted margin for two-phase correlations. It should be noted that the Rohsenow correlation is for a single heat source. The work of Kim et al. [13] was used to resolve the four die arrangement used in the current study into the single heat source geometry necessary for integration into the correlation.

FLOW BOILING ENHANCEMENT

As shown in Figure 4, by introducing 660 mL/min of subcooled dielectric fluid flow, the maximum power dissipation achieved increases by over 100W, or approximately 40%, at the same chip operating temperature. For the results in Figure 4, the working dielectric fluid was subcooled by the facilities chilled water distributed by the chiller at a set point of 15°C. While adding pumping power increases the energy consumption of the overall thermal management solution, the increase in power density capabilities possible by adding this flow loop cannot be ignored.

Increasing the dielectric fluid flow rate under the flow boiling scenario should have no effect on the fully developed boiling regime as the two-phase heat transfer occurring at the surface is dominant when compared to that attributable to forced convection. This concept is experimentally verified in the results of Figure 5 as the thermal performance curves merge for primary die power dissipations that are associated with fully developed boiling conditions across all of the dielectric fluid flow rates tested. While not experimentally illustrated as part of the current study, increasing the dielectric fluid flow rate in a flow boiling scenario does increase the maximum power dissipation that a heated surface can achieve before burnout. This has been shown in a recent work by the authors of the current study, and power dissipations in excess of 600W have been achieved from four similarly sized heated surfaces to the current study with the use of microporous surface enhancements [7].

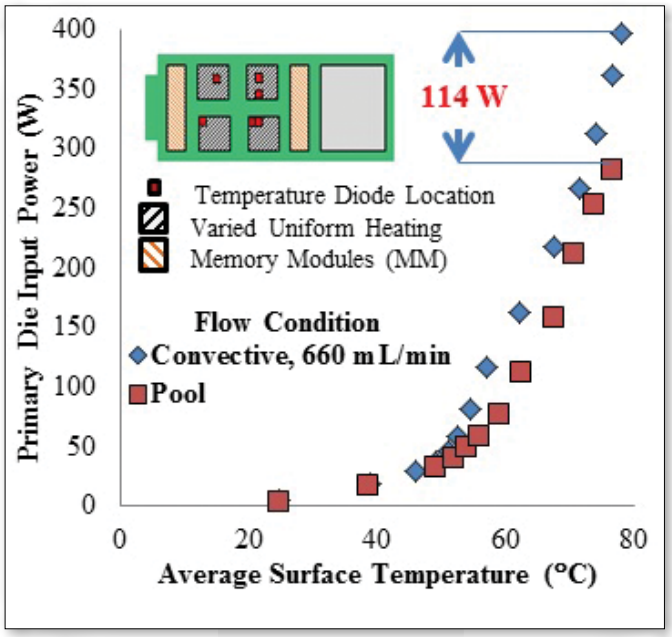


Figure 4 - Plot showing the increase in maximum power dissipation available with the pumping of a slight amount of subcooled FC-72 fluid within the electronics enclosure. The red squares on the image to the top left of the plot indicate where temperatures were measured for calculation of the average value presented. [4]

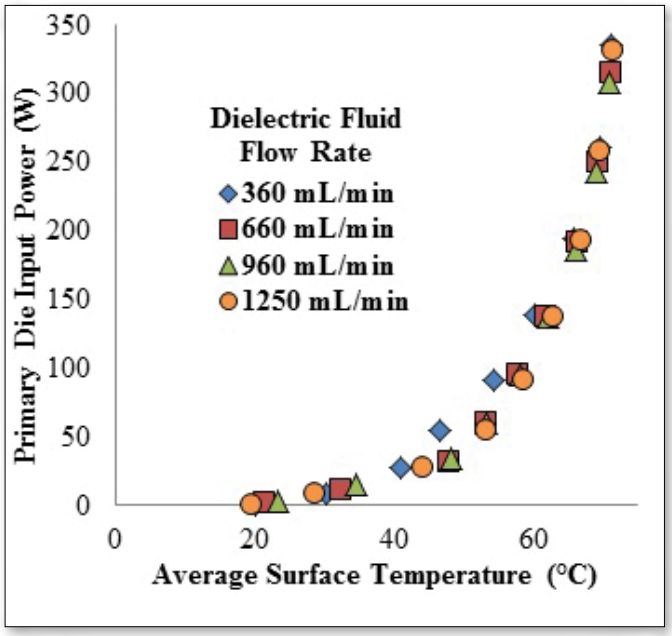


Figure 5 - Plot showing the negligible effect of increasing the dielectric fluid flow rate on the average surface temperature of the primary die within the range of total power dissipations associated with the fully developed boiling regime. [4]

CONCLUSIONS

The current study shows the practical application of liquid immersion cooling techniques to a high performance server model with a limited footprint both in terms of volume occupied and fluid reservoir required. Under pool boiling conditions a maximum power dissipation of slightly over 300W was achieved while over 100W more is available with the introduction of only a modest amount of subcooled dielectric fluid flow within the enclosure. The study has shown that power densities on the order of current generation processing elements and beyond can be easily handled at a significantly lower operating temperature than many of the more conventional air-cooled techniques can achieve. As consumer demand drives electronics into more compact form factors, the evolution of immersion cooled studies will become increasingly important as resulting heat fluxes will necessitate a matriculation to some form of two-phase liquid cooling.

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The Products & Services Index contains many categories to help find the products and services you need. Details of all the suppliers listed within each category can be found in the company directory, starting on page 40. To learn how to be included in this directory, e-mail editor@electronics-cooling.com.

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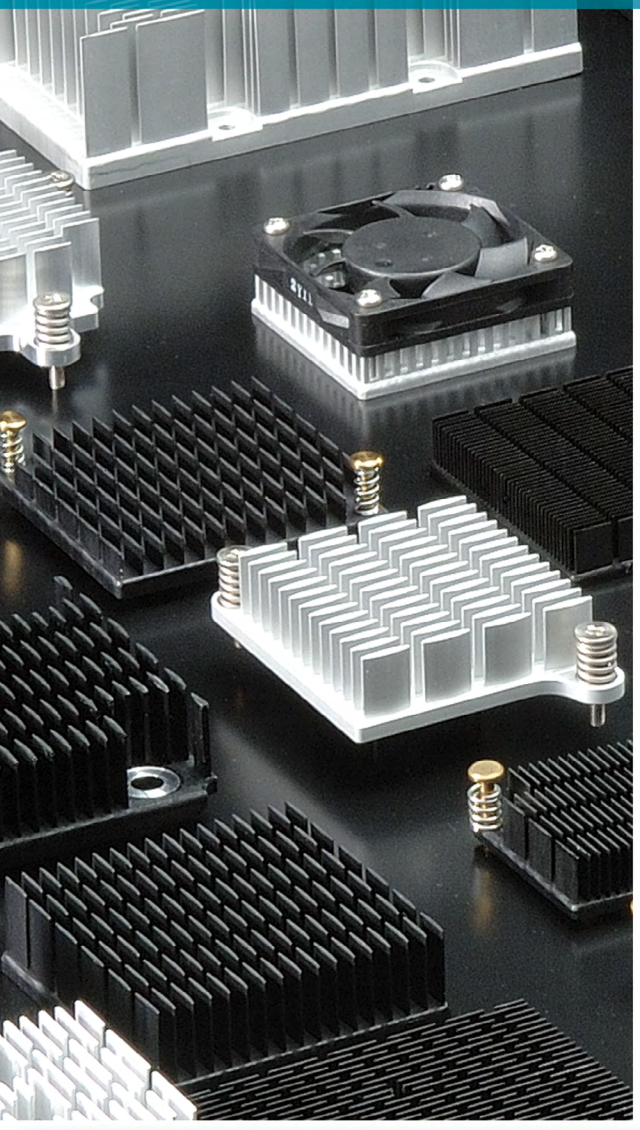

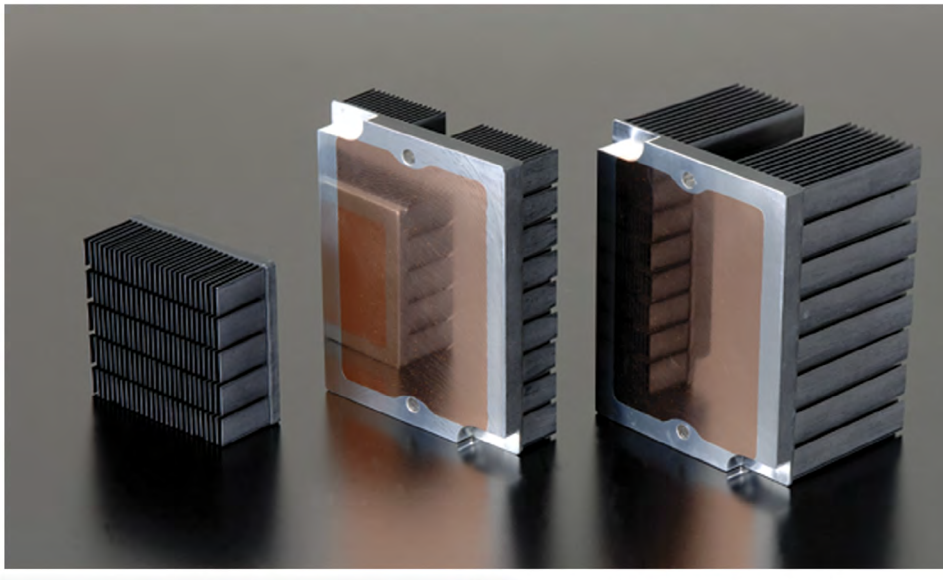

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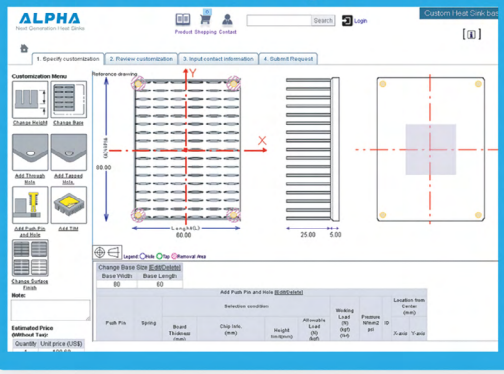

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