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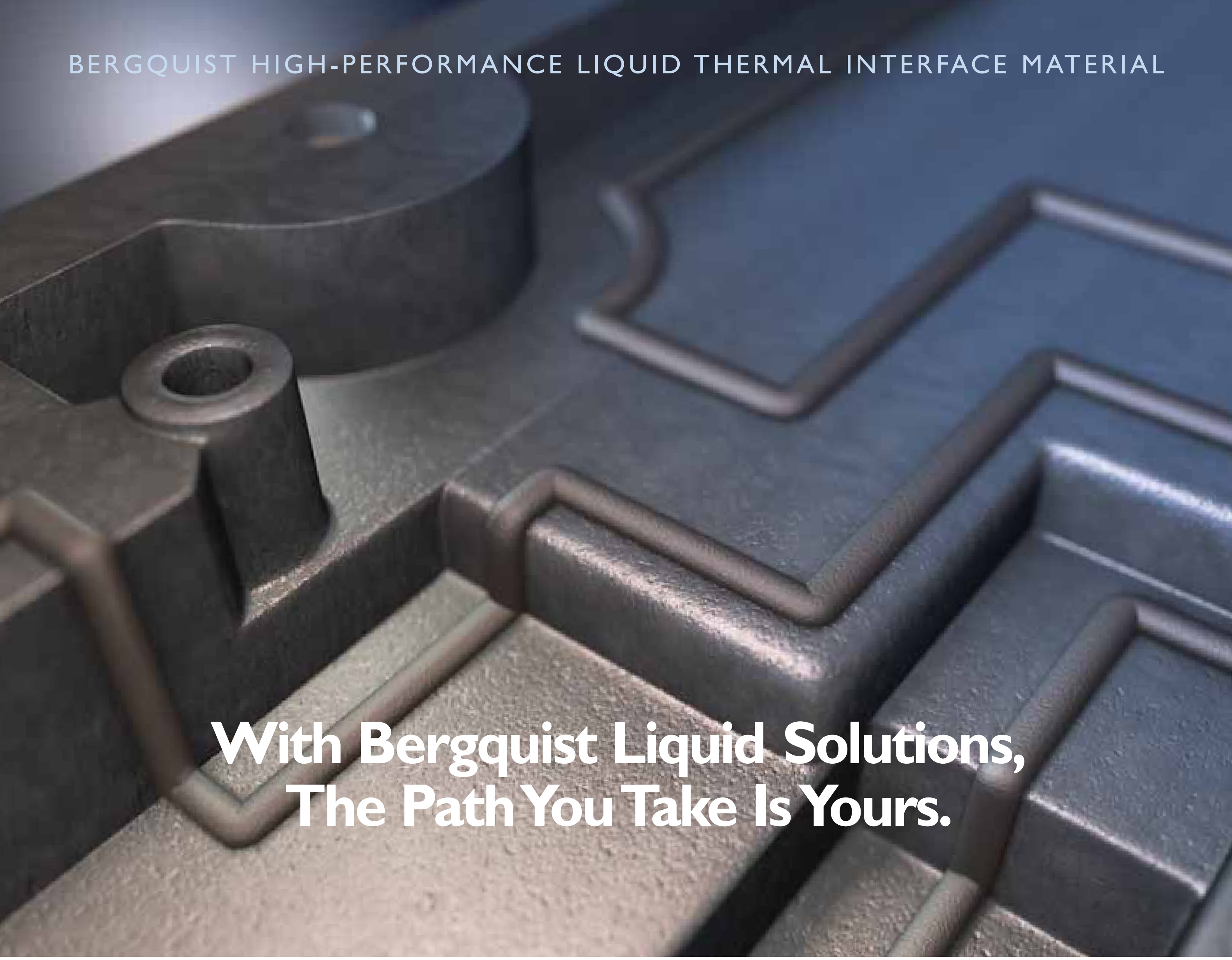

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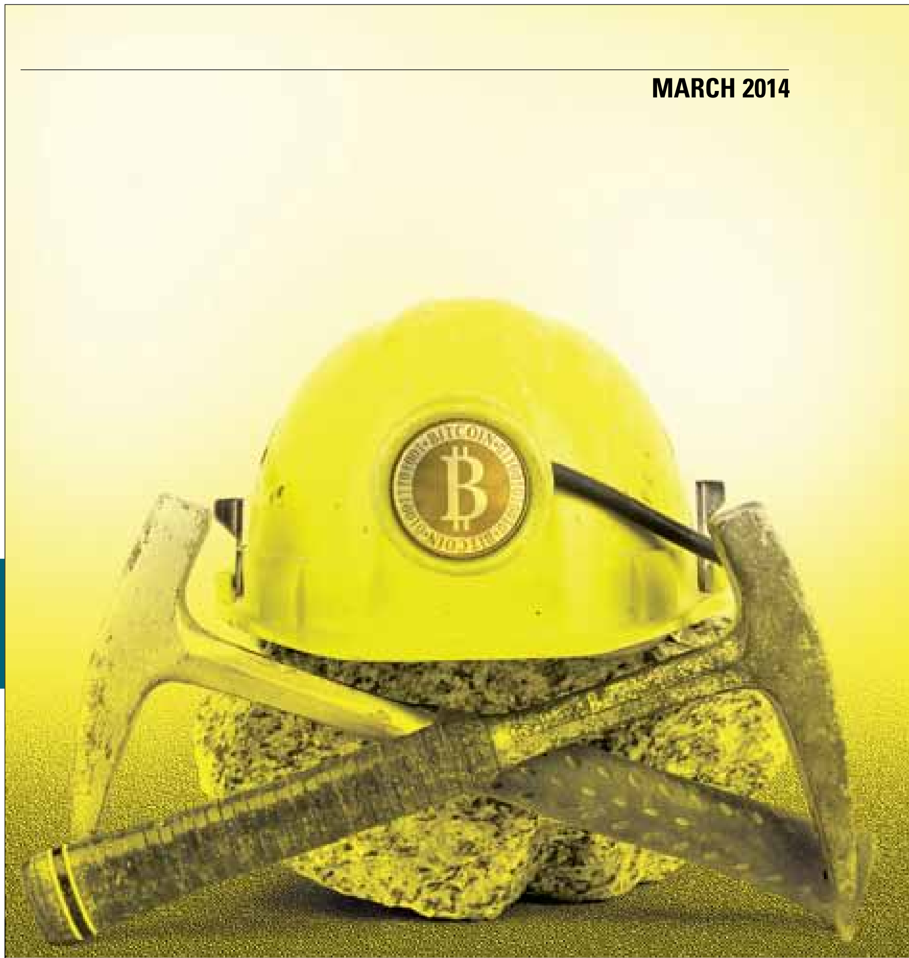

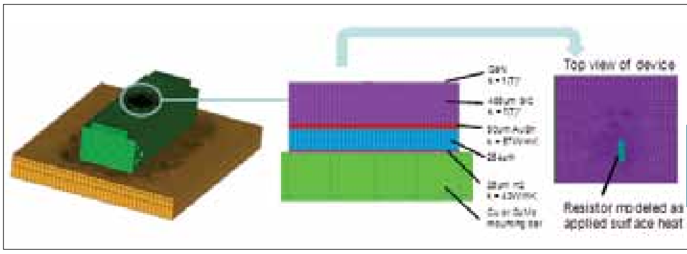

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2014 BUYERS' GUIDE

Editorial

Understanding Capacitance and Time Scales

Jim Wilson, Editor-in-Chief, March 2014

WATCHING THERMOCOUPLES SLOWLY change temperature was one of those important tasks I was given as a new thermal engineer. We were required to test some avionics hardware at the extremes of a large ambient temperature range and one of my responsibilities was to determine when we were close enough to steady-state conditions.

The test plan indicated we would verify that thermocouples mounted to the system were changing at a rate of less than a certain temperature change/hour (one degree C if I remember correctly) but what I do remember is the test going into the late hours and wanting to calculate the temperature/time derivative over shorter and shorter time scales so we could execute the test and go home. This particular system was somewhat insulated from the external environment to mitigate aerodynamic heating effects and also had significant thermal capacitance. Establishing equilibrium between the thermal mass of the system and the ambient required a long time scale so we learned patience and an appreciation for thermal capacitance. This lesson has found application over time when interpreting thermal test results, especially when insulation is used to mitigate heat loss from part of the system.

An understanding of capacitance, or inertia to be more precise, and appropriate time scales is also important for effectively participating and functioning in a work environment. As thermal engineers, we should well understand an analogy between the inherent inertia of a well-functioning design team and the appropriate time scale of measuring team performance. A common conflict is that management desires a measure of performance over a time scale that may not be consistent with long term needs. For example, training and overhead support costs can be reduced and the team inertia will most likely assure that for a short term, the team is achieving good performance at a lower cost.

Unfortunately, a frequent scenario is the eventual decrease in team performance does not show up until the responsible manager has been promoted for his ability to reduce expenses. Efforts by a future manager to improve the team's performance are complicated by the team inertia, which is initially trending towards deterioration, and results from corrective training are not apparent in the short term.

A reasonable question is what is the right time scale for assessing team performance? While the answer is complicated and beyond my engineering skill set, it is helpful for us as thermal engineers to recognize at least two factors influencing a desire for short term measurements. One is the business cycle and the need to show money is being made on a scale consistent with investor expectations. The other is the desire for quick feedback. It is not easy for us to learn when the outcome is not apparent or the outcome is measured on a scale that is longer than desired. For example, telling a child to eat vegetables so they will be healthy 50 years later is rather hard for them to learn. A time scale of that duration is just not relevant to their experience. We naturally desire quicker feedback so it is not unreasonable that the manager funding increased training wants to know how soon it will show benefits.

While it is easy to find faults with management decisions, I would like to make this editorial a bit more personal. Since this is the first issue of 2014, it is a good time to assess your own career development and make sure you are continually finding opportunities to learn and improve your skills. If you were fortunate to have a good year in 2013, remember that we all have a risk of relying on past accomplishments and assuming that our credibility, or inertia, will carry us forward. Finding the right time scale for self-assessment can be difficult but it does need to be long enough to assure you are improving your skills.

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Cooling Matters

Applications of thermal management technologies

ELECTRICAL FIELD FACILITATES BETTER HEAT TRANSFER

The application of an electric field to a condenser could double the efficiency of surface heat transfer in power plant and high performance computing cooling systems, according to new research released by scientists at MIT.

The discovery builds upon previous research completed last year, in which the team found that a superhydrophobic surface produced via a specific nanopatterning of condenser surfaces caused water droplets to combine and leap from those surfaces as the result of a release of excess surface energy.

According to the researchers, the phenomenon improved the efficiency of heat transfer from condenser surfaces by 30 percent. Upon further examination, the team also noticed that the water droplets acquired a positive electric charge as they jumped away. "We found that when these droplets jump, through analysis of high-speed video, we saw that they repel one another midflight," one researcher said. "Previous studies have shown no such effect. When we first saw that, we were intrigued."

Source: MIT

RESEARCH COULD LEAD TO NEW THERMAL FLOW CONTROL DEVICES

Researchers have proposed a new method of controlling heat flow similar to the way electronic components handle electrical current that could deliver more efficient thermal management in a variety of applications.

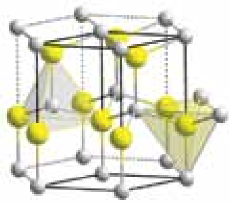
Developed by scientists at Purdue University, the technology utilizes tiny triangular or T-shaped structures made of graphene nanoribbons to control phonons, quantum mechanical phenomena that illustrate how vibrations travel between atoms and can be used to determine the rate of heat flow throughout a system.

Advanced simulations conducted by the Purdue team have shown the triangular structures offer a way to control this heat flow through a process known as "thermal rectification," which allows heat to flow more efficiently in one direction.

It could also provide a breakthrough in the development of thermal transistors. Engineers have begun to design and test thermal transistors with some success in recent years, but overall the work remains in its infancy. Unlike conventional transistors, thermal transistors would not require the use of silicon, are based on phonons rather than electrons and may make use of the waste heat already generated by most electronic devices.

Source: Purdue University

GALLIUM NITRIDE CONTRIBUTES TO LASER COOLING BREAKTHROUGH



Researchers have discovered a new method of engineering gallium nitride that could help eliminate the need for current heat dissipation methods.

Considered one of the most important semiconducting materials after silicon, GaN's hardness, crystalline structure and wide bandgap make it ideal for a variety of applications in the optoelectronics industry.

Now, researchers at Lehigh University believe GaN can be engineered so that light passing through the compound cools it instead of heating it, a phenomenon known as laser cooling or laser refrigeration that would eliminate the need for expensive cooling methods currently in use.

The technique relies on a phenomenon known as anti-Stokes photoluminescence, which refers to the small fraction of photons whose frequency increases after hitting a material.

Source: Lehigh University

Datebook

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NASA FIXES BROKEN COOLING LOOP ON INTERNATIONAL SPACE STATION

Astronauts recently successfully installed a replacement ammonia pump assembly aboard the International Space Station this week in a major step towards restoring a malfunctioning coolant loop to normal operation.

According to NASA, the pump module inside one of the space station's two external cooling loops, which circulate ammonia outside the space station to keep both internal and external equipment cool, automatically stopped working when it reached a pre-set low temperature limit. The problem was linked to a malfunctioning flow control valve, which reportedly stopped "positioning itself properly" resulting in the temperature drop.

Source and image: NASA

CARBON NANOTUBES OFFER THERMAL STRESS RELIEF AT CRITICAL JUNCTIONS

Scientists at Stanford University have released new findings that demonstrate the benefits of using carbon nanotube arrays at critical junctions between two materials to help better relieve thermal stress.

Thermal stress, often caused by the joining of two materials that expand and contract at different rates as temperatures change, can lead to unnecessary strain and component damage if not mitigated properly.

Research indicates it has grown less-densely together, seemed to have the best combination of flexibility, heat conductivity and strength for use in electronics and other industrial applications where thermal stress is expected.

Source: Stanford

MAGNETIC NANOPARTICLES PREVENT HOTSPOTS IN COOLING SYSTEMS

An international team of researchers has discovered a way to enhance heat transfer using magnetic fields, a method they say could prevent hotspots that can lead to system failures.

The new system, which relies on tiny particles of magnetite, a form of iron oxide, is the result of several years of research on nanofluids and could be used to cool everything from small electronic devices to advance fusion reactors. The recent work involved experiments where magnets were placed on the outside of tubes containing magnetite nanofluid, increasing the heat transfer coefficient of the nanofluid up to 300 percent that of plain water.

Source: MIT

NEW ULTRATHIN MATERIAL LEADS TO BETTER THERMALLY CONDUCTIVE COATINGS

Scientists at Kansas State University have discovered a new ultrathin electrically conductive material they say may lead to advances in the efficiency of electronic and thermal devices.

They found that manipulating molybdenum disulfide (MoS_2)—a three-atom-thick inorganic compound material—with gold atoms improved its electrical characteristics significantly.

The discovery is the latest step in the team's research on the synthesis and properties of next-generation atomically-thick nanomaterials, such as graphene and boron-nitride.

MoS_2 was recently shown to have better transistor-rectification than that of graphene, which is a single-atom-thick sheet of carbon atoms.

Source: Kansas State

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Use of JEDEC Thermal Metrics in Calculating Chip Temperatures in Packages with Attached Heat Sinks

Bruce Guenin
Assoc. Technical Editor

INTRODUCTION

THE PREVIOUS COLUMN (from Dec. 2013) dealt with the application of JEDEC thermal metrics to IC packages that do not have heat sinks attached to them [1]. The methods are applicable to prediction of the junction temperature before the system is built and also to determining it from temperature measurements in the completed system.

When no heat sink is attached to a package, in a typical system, the dissipated heat is removed from t he package and its associate printed circuit board (PCB) by a convection process (either natural or forced) supplemented by radiation cooling. Since, typically the PCB has a much larger surface area than the top of the package, most of the heat flows to the air via the PCB, as illustrated in Figure 1a. The figure identifies the relevant temperatures and their location to be used for calculating the appropriate thermal metrics, as described in the previous column. These temperatures are measured at the following locations: incoming air (T_A), package top center (T_T), board (T_B), and the junction (T_J).

However, when a heat sink is attached to the top of the package, it enhances the flow of heat from the top of the package to the air, as shown in Figure 1b. In addition to the temperature locations measured when no heat sink is present, the temperature on the bottom of the heat sink, T_S, is also measured. Note that, when a heat sink is present, it is customary to refer to the temperature of the top center of the package as the case temperature (T_C).

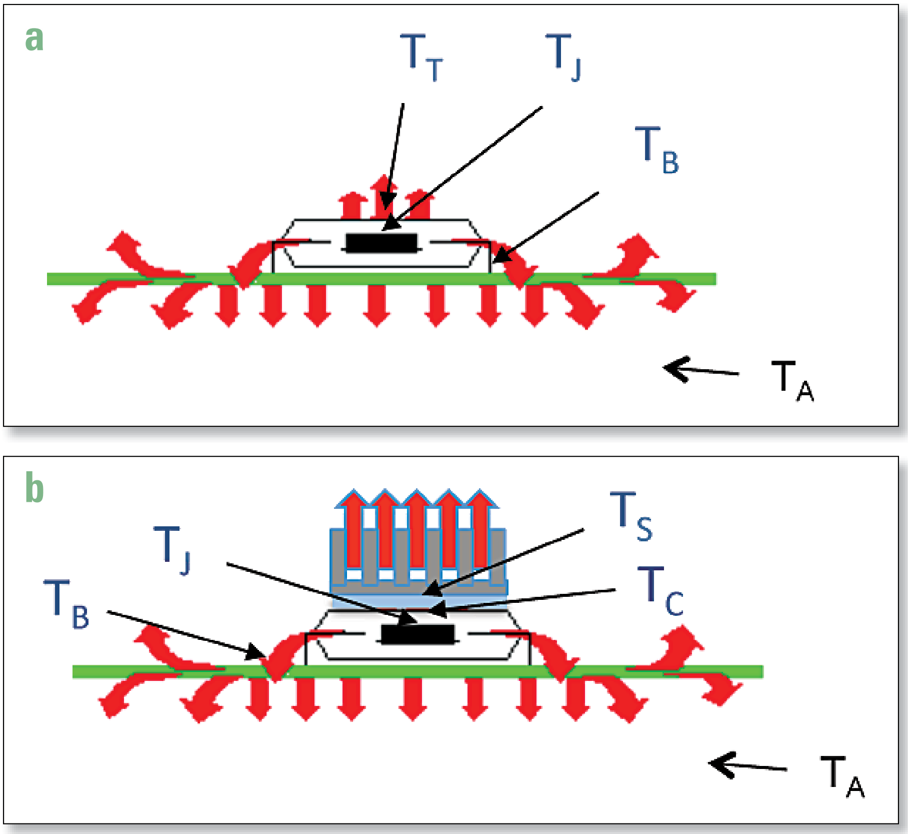

FIGURE 1: Diagrams representing typical heat flow paths for a package mounted to a test board in natural or forced convection, **(a)** no heat sink, and **(b)** heat sink attached. The indicated temperature measurement locations are those specified by the JEDEC respective test standards for each configuration.

Figure 2 depicts a thermal resistance network representing the two primary heat flow paths. The upward path has two thermal resistances in series: Θ_{JC}, the junction-to-case thermal resistance and a second one representing the heat flow path from the top of the package to the air. When no heat sink is present, this resistance is Θ_{CA}, the case-to-air thermal resistance. When a heat sink is attached to the top of the package, then this resistance is represented by Θ_{SA}, the sink-to-air thermal resistance.

The downward heat flow path also has two resistances in series: the junction-to-board thermal resistance, Θ_{JB}, and the board-to-air thermal resistance, Θ_{BA}.

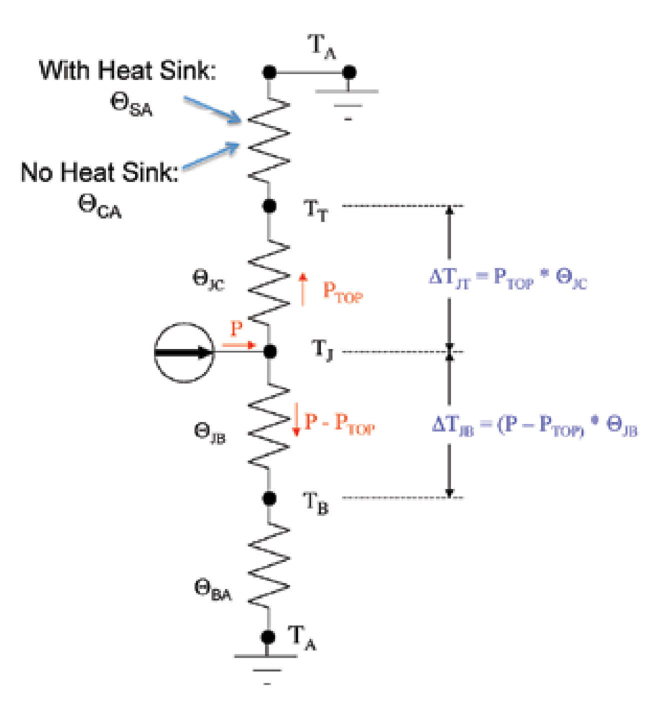

FIGURE 2: Thermal resistor network representing junction-to-board-to-air path and junction-to-case-to-air path. Resistor between top of package and air may represent either case-to-air thermal resistance when there is no heat sink or sink-to-air thermal resistance when there is a heat sink.

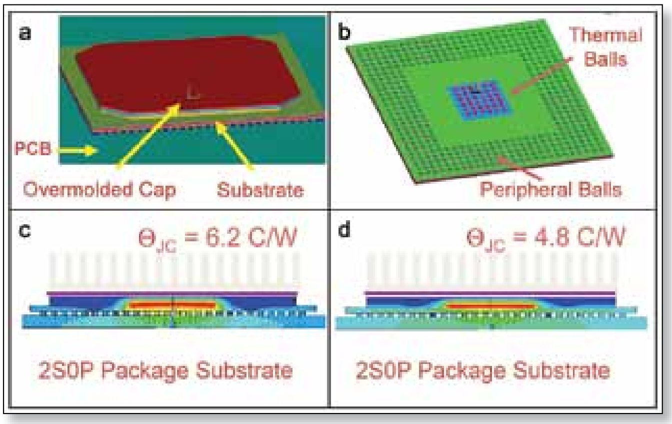

FIGURE 3: Graphical outputs from thermal simulation of 35 x 35 mm, 388 ball, PBGA packages. Views of solid model: **(a)** top view closeup of the package attached to a PCB and **(b)** bottom view of package only, depicting the solder ball configuration. Simulation results for packages in Θ_{JC} test environment with two different laminate configurations: **(c)** 2S0P and **(d)** 2S2P.

TABLE 1: DETAILS OF PACKAGE, TEST BOARD, AND HEAT SINK	
Package Type	PBGA
Pkg Size	35 x 35 x 2.33 mm
Die Size	10.2 x 10.2 x 0.3 mm
Ball Count / Pitch	388 / 1.27 mm
Thermal Ball Count	36
Laminate Stackup	2S0P and 2S2P
t_{EMC} (mm)	0.74
k_{EMC} (W/mK)	0.7
Test Board Size	100 x 100 x 1.6 mm
Board Stackup	2S2P, JEDEC Std.
Heat Sink #1	28 x 28 x 6 mm / 8 x 8 Pin Fin Array
Heat Sink #2	28 x 28 x 15 mm / 7 x 8 Pin Fin Array

METHOD OF CALCULATING Θ_{JA} WITH HEAT SINK ATTACHED

This column explores a method for predicting Θ_{JA}, with a heat sink attached, using the metrics measured on the package without the heat sink attached (Θ_{JA}, Ψ_{JB}, and Ψ_{JT}), the junction-to-case thermal resistance (Θ_{JC}), and the sink-to-air thermal resistance (Θ_{SA}), normally measured by the manufacturer.

Two different package configurations are evaluated: The first with two metal layers on the top and bottom surfaces of the package substrate. These are both signal layers. There are no metal planes. This nomenclature to describe this substrate stackup is: 2S0P. The second has two metal planes in addition to the two signal layers of the previous package. These planes provide much more efficient lateral spreading of heat than do the discontinuous signal layers. The stackup of this substrate is typically referred to as 2S2P. The thermal performance of the 2S2P package was studied in the previous column. Other details of the packages, test board, and heat sinks are provided in Table 1.

The packages are each attached to a four-layer JEDEC-standard board, containing two metal planes, for testing. In performing the Θ_{JC} tests, the top of the package is pressed into contact with a water-cooled cold plate. A compliantly-mounted thermocouple measures the case temperature.

Figures 3a and 3b illustrate the construction of the package. Figure 3a shows a top view closeup of the package attached to a PCB. The substrate is shown with the overmolded cap covering the IC. When the heat sink contacts the package, it is pressed against the top surface of this cap. The cap is made of low-thermal-conductivity molding compound, which makes a significant contribution to the measured value of Θ_{JC}. Figure 3b depicts the peripheral rows of solder balls that connect to the surface traces of the test board and the 6 x 6 array of thermal balls that are routed by vias to one of the two internal planes in the board to further enhance the thermal performance of the package. Figures 3c and 3d show the results of simulations of the Θ_{JC} test with each of the two package configurations. The temperature contours show clearly the superior heat spreading ability of the 2S2P substrate compared to that of the 2S0P one, leading to a lower value of Θ_{JC} for the 2S2P package. [Note that the cooling effect of the cold plate was represented in the model by impos-

TABLE 2: MEASURED VALUES OF THERMAL METRICS WITH CALCULATED VALUES OF h AND POWER PARTITIONING.

Package Laminate	V_{air} (m/s)	P (W)	Θ_{JA} (°C/W)	Ψ_{JB} (°C/W)	Ψ_{JT} (°C/W)	Ψ_{BA} (°C/W)	Θ_{JC} (°C/W)	h, Top (W/m²K)	P_{Top} (W)	P_{Board} (W)
2S0P	0.5	3	20.2	14.5	0.4	5.8		18.0	0.11	2.89
	1	3	18.9	14.2	0.5	4.7		26.4	0.15	2.85
	2.5	3	17.1	13.8	1.0	3.3		53.0	0.26	2.74
	N/A	6					6.1			
2S2P	0.5	3	16.6	10.7	0.4	5.9		22.4	0.11	2.89
	1	3	15.4	10.6	0.5	4.8		32.3	0.14	2.86
	2.5	3	13.7	10.4	0.9	3.3		61.2	0.24	2.76
	N/A	6					5.5			

TABLE 3: FINAL THERMAL RESISTANCE VALUES FOR INPUT INTO THERMAL RESISTANCE NETWORK. FINAL UP-PATH AND DOWN-PATH RESISTANCES. % HEAT FLOWING OUT TOP.

Package Laminate	V,Air (m/s)	Power (W)	HS, Thk (mm)	Θ_{CA} (°C/W)	Ψ_{SA} (°C/W)	Ψ_{JC} (°C/W)	Ψ_{JB} (°C/W)	Θ_{BA} (°C/W)	$\Theta_{Up Path}$ (°C/W)	$\Theta_{Down Path}$ (°C/W)	% P_{Top} (%)
2S0P	0.5	3	0	555	N/A	6.1	15.0	6.0	561	21.0	4%
			6	N/A	12.4	6.1	15.0	6.0	18.5	21.0	53%
			15	N/A	5.5	6.1	15.0	6.0	11.6	21.0	64%
2S2P	0.5	3	0	446	N/A	5.5	11.1	6.1	451	17.2	4%
			6	N/A	12.4	5.5	11.1	6.1	17.9	17.2	49%
			15	N/A	5.5	5.5	11.1	6.1	11.0	17.2	61%

ing a very large heat transfer coefficient on the top of the package (40,000 W/m²K). The heat sink was not explicitly included in the model.] These results were reprinted from a previous installment of this column, which provides an extensive discussion of their significance [2].

Table 2 lists all the package metrics measured for each of the two package configurations. Note that apart from Θ_{JA} and Θ_{JC}, all the other metrics are not thermal resistances, but the thermal characterization parameters, Ψ_{JT}, Ψ_{JB}, and Ψ_{BA}. Note that they have to converted into their equivalent thermal resistance values before they can be input into the thermal resistance network in Figure 2. This will then enable the calculation of Θ_{JA} for the package with the heat sink attached. In order to be able to perform this conversion, one must know the actual power flowing along the upward path to the heat sink (P_{Top}) and a separate value of power flowing to the PCB (P_{Board}).

The following equations may be used to calculate P_{Top} and P_{Board}:

$$P_{Top} = h \bullet A_{Die} \bullet \Delta T_{TA} \quad \textbf{(1)}$$

where h is the heat transfer coefficient on the top surface of the package, A_{Die} is the area of the die, and ΔT_{TA} is the temperature difference between the top of the package and the ambient air. It is assumed that most of the heat will flow to the top surface of the package directly from the die and a much smaller amount from the surrounding substrate.

The value of h can be calculated from the following expression, which is a rearrangement of terms of Eqn. 3 in the previous column [1]:

$$h = \frac{\Psi_{JT} \bullet \kappa_{EMC}}{\Theta_{JA} \bullet t_{EMC}} \quad \textbf{(2)}$$

where κ_{EMC} and t_{EMC} are the thermal conductivity and thickness above the die of the epoxy molding compound comprising the overmolded cap. Specific values of these parameters are provided in Table 1.

ΔT_{TA} can be calculated as follows:

$$\Delta T_{TA} = P \bullet (\Theta_{JA} - \Psi_{JT}) \quad \textbf{(3)}$$

where P is the total power dissipated in the chip." Next, P_{Board} is calculated from

$$P_{Board} = P - P_{Top} \quad \textbf{(4)}$$

Finally, any thermal characterization parameter (psi value) can converted into the equivalent thermal resistance (theta value) using the following relationship:

$$\Theta_{XY} = \frac{P \bullet \Psi_{XY}}{P_{XY\,Path}} = \frac{\Delta T_{XY}}{P_{XY\,Path}} \quad \textbf{(5)}$$

Thus, $\Theta_{JB} = P \bullet \Psi_{JB} / P_{Board}$.

RESULTS AND DISCUSSION

Table 2 presents all of the theta and psi value test results for the package without the heat sink attached. It also provides the calculated values of h, P_{Top}, and P_{Board}. One notes that the measured values of Θ_{JC} are close to the simulated ones. The calculated values of h are consistent with handbook values [3]. Also, it is notable that the heat out of the top of the package increases with air velocity and is less than 10% of the total in all cases. This is consistent with the image in Figure 1a, which depicts the board functioning as an extended fin to transfer most of the dissipated power to the air.

Table 3 lists all the thermal resistance values needed for input into the thermal resistance diagram of Figure 2. It includes the calculated values of Θ_{CA} for the package without a heat sink. Note that the values of these resistances are quite high, owing to the very small area of heat exchange at the top of the package (~ 100 mm^2). It is a very interesting contrast in the % of heat flowing out of the top of the package: no heat sink – 4%; with heat sink – 49-64%. The latter result would be expected since the thermal resistance for the up and down heat paths are nearly equal for the 6mm heat sink. For the 15 mm heat sink, the resistance for the up path is about ⅔ of that for the down path.

Table 4 lists the final calculated values of Θ_{JA} for the situations in Table 3 and compares them to the actual test values. The calculated and test values for the packages without a heat sink are nearly equal. This is an simply an indicator that the arithmetic for these cases was correct. The results for the cases with the heat sinks are much more interesting. The model consistently predicts a value of Θ_{JA} that is about 30% lower than the test value.

That there is such a large difference should not be much of a surprise. The model is explicitly based on the assumption that Θ_{JB} is invariant, independent of the partitioning of the heat between the up and down paths. This is clearly not the case. As more heat is drawn out of the top of the package, more heat flux lines that had been flowing from the die to the board are diverted toward the top of the package. This would, essentially, leave a smaller number of flux lines flowing to the board. This modified path to the board would have a higher thermal resistance since the cross-sectional area of the metal participating in transmitting a smaller number of flux lines would be less, leading to a higher thermal resistance of this path.

It should be noted that the error is exacerbated by the fact that the up and down path thermal resistances are roughly comparable. If one of the resistances were dominant, then the error would be reduced.

A second effect is that the presence of the heat sink would divert the air flow from the top surface of the board downstream from the heat sink. This would reduce the effective heat transfer coefficient, leading to a higher Θ_{BA} than that assumed in this model.

TABLE 4: COMPARISON OF TEST AND CALCULATED VALUES OF Θ_{JA} WITH HEAT SINK ATTACHED TO PACKAGE TOP

Package Laminate	Heat Sink Height	Θ_{JA} TEST	Θ_{JA} CALC	$\Delta\Theta_{JA}$	
	(mm)	(ºC/W)	(ºC/W)	(ºC/W)	(%)
2S0P	0	20.2	20.2	0.01	0.03%
2S2P	0	16.6	16.6	0.01	0.04%
2S0P	6 mm	13.9	9.8	-4.1	-29%
2S2P	6 mm	11.8	8.8	-3.0	-26%
2S0P	15 mm	11.5	7.5	-4.0	-35%
2S2P	15 mm	9.9	6.7	-3.2	-32%

CONCLUSIONS

A method was demonstrated to integrate package-level and heat sink thermal measurement results in the calculation of the thermal performance of a package with the heat sink attached. The method has the benefit of being straightforward and intuitively satisfying. However, in the case explored here, the error was about 30% and overpredicted the final level of performance.

The fact that the competing heat flow paths were similar in magnitude exacerbated the error. Nonetheless, the user should be cognizant of the possibility of errors of this magnitude resulting from the use of thermal metrics that are not boundary-condition independent and exercise appropriate caution in interpreting the results.

The use of boundary-condition-independent thermal compact models involves more complexity. However, it is a much more robust method and is recommended for use in critical applications [4].

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Potential Pitfalls of Hybrid Electrical-Thermal Measurements for Thermal Characterization

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INTRODUCTION

ELECTRICAL RESISTORS are often used to simulate heat-dissipating electronic devices in thermal characterization of semiconductor devices. This article describes a study in which test measurements and analysis were conducted in steady-state conditions to characterize the thermal performance of an RF device stack-up using resistance thermometry. Discrepancy between the test-measured and numerically predicted thermal resistance results was traced back to the potential presence of an extraneous electrical resistance in the resistor circuit, or an unexpectedly poor thermal interface, with the two being indistinguishable from the data. This intertwining of electrical and thermal resistance can make accurate thermal characterization of devices and their constituent components difficult under steady-state conditions and illustrates the pitfalls of this methodology.

EXPERIMENTS

The purpose of the study was to characterize the thermal performance of the constituent components of an RF device package, as shown in Figure 1(a). The device, comprising of the resistive heater, was bonded to a metallic heat spreader with gold/tin (AuSn) solder. The spreader, in turn, was bonded to a Copper or a Copper-Molybdenum mounting bar with indium solder [1]. The mounting bar tab was bolted on to an Al baseplate. The objective of the test configuration was to characterize various spreader and thermal interface material (TIM) combinations to verify the optimal thermal packaging configuration. The resistive heater was used both as a heat source and a thermometer, the schematic of which is shown in Figure 1(b)

Three tests were conducted, with the details for different configurations given in Table 1. Test configuration 1 involved a 121μm x 350μm resistor, while tests 2 and 3 had larger resistors, 355μm x 5000μm each.

The temperature-resistance relationship of the heater was calibrated from 20°C to 120°C by adjusting the baseplate temperature while passing a small current through the resistor so not to generate appreciable self-heating. The resistance of the heater was calculated by the measured voltage drop and current for each test temperature, thereby establishing the temperature coefficient or resistance. As anticipated, the measured electrical resistance-temperature curve for these Pt resistors was essentially linear. Each R vs. T curve was represented as:

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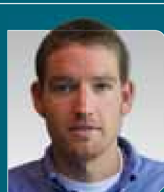
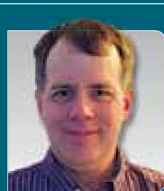


Daniel P. Resler is currently a senior principle engineer with Raytheon Integrated Defense Systems in Andover MA where he develops high power devices for fast, wide angle beam steering and adaptive optics. Resler specializes in thin film design and deposition, semiconductor processing, and physical optics. A current topic of his work is the use of polarization gratings for high efficiency beam deflection. He holds six US patents and is the author of 20 peer reviewed papers. Resler received a BS in Materials Science from Cornell University in 1980, and the MSEE from Northeastern in 1985.



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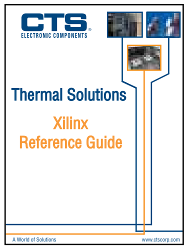

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$$R = R_0 [1 + \alpha(T - T_o)] \quad \textbf{(1)}$$

with R_0 being the nominal resistance at room temperature, T_o, of approximately 20ºC; and α, the derived constant from calibration. Table 2 shows the measured quantities used to establish the R vs. T curve. The values of α are in reasonable agreement with the reported numbers for thin Pt films [2].

With this relation established, testing was performed for the test configurations presented in Table 1. Each test involved gradually increasing the heat dissipation in the resistor in several increments such that the lowest applied heat load resulted in minimal ohmic heating, while the highest applied load maintained the resistor operating temperature at 130ºC. For all tests, a temperature of 30ºC was maintained at the thermocouple in the mounting bar for all power levels. The measured thermal resistance (mm²-ºC/W) was calculated using equation (2), normalizing for device footprint and enabling comparison of data collected with devices of varying footprint.

TABLE 1: DEVICE HARDWARE CONFIGURATION FOR TEST CASES

		Footprint (µm)	Thickness (µm)
Resistor	Pt		
	Test configuration 1	121 x 350	0.095
	Test configuration 2	355 x 5000	0.095
	Test configuration 3	355 x 5000	0.095
Device	GaN-on-SiC		
	Test configuration 1	1980 x 1730	485
	Test configuration 2	5970 x 5540	485
	Test configuration 3	5970 x 5540	485
	AuSn solder (80/20)		50
	Spreader		254
	In/Pb/Ag (80/15/5)		25
		Footprint (mm)	**Thickness (mm)**
Mounting Bar			
	Cu, Test 1	45 x 17	12
	CuMo, Test 2	45 x 17	12
	Cu, Test 3	45 x 17	12
Baseplate	Al	62 x 50	6.3

$$\text{(Device footprint area)} * \frac{T_{resistor} - T_{mounting\ bar\ thermocouple}}{\textit{Input power}} \quad \textbf{(2)}$$

ANALYSIS

Detailed finite element (FE) models were created to represent the set-up described in the "Experiments" section with the goal of replicating the experimental data and verifying understanding of constituent thermal properties. Figure 2 shows the details of the FE modeling performed with a commercial software [3].

Material properties were applied and heat load was modeled as a uniform heat flux over the resistor area. The Al baseplate fixed-temperature boundary condition was adjusted until the thermocouple location in the mounting bar matched the test temperature of 30°C.

RESULTS

Experimentally measured and numerically predicted thermal resistance results are compared in Figure 3 for three test configurations under consideration. Applied power has been normalized by the nominal electrical resistance at 20ºC to enable comparison of device testing with different power dissipations. Observed experimental and analytical trends are as expected, with thermal resistance increasing due to the decreasing thermal conductivity of SiC with increasing temperature. However, analytical predictions consistently under predicted the experimental data, requiring further investigation into potential discrepancies.

The experimental and analytical set-ups were carefully evaluated to establish repeatability. The following potential causes were investigated as a cause of the difference between the measurement and analysis.

TABLE 2: MEASURED ELECTRICAL RESISTANCE AS A FUNCTION OF TEMPERATURE FOR TEST RESISTORS 1, 2 AND 3

	Device footprint (µm)	Mounting bar thermocouole (ºC)	R (ohms)	α (calculated) (ohm/ohm/ ºC)
Resistor 1	1980 x 1730	20.0	4.1	0.003
		109.5	5.3	
Resistor 2	5970 x 5540	21.6	20.5	0.029
		124.9	26.6	
Resistor 3	5970 x 5540	20.9	20.0	0.029
		119.0	25.8	

ANALYSIS INDUCED POTENTIAL ERRORS:

1) Modeling errors, software issues, inadequate mesh density – Analysis was conducted in two different software packages [3, 4]. Model predictions were mesh independent and results were replicated between the two software packages.

2) Application of power as uniform heat flux on the resistor area – Multi-physics electro-thermal modeling [5] confirmed a non-uniform distribution of heat flux over the resistor area due to the temperature-dependent electrical resistance of the heater. Figure 4 shows the results for Test 1 configuration at approximately 8 volts or, 11W of heat. Non-uniformity in current density is observed to be within a ±1.5% band around a mean of 1.275e+11 A/m², and ±6% for heat flux around a mean of approximately 3e+8 W/m². Larger current flow resides around the edges, producing a large heat flux along the periphery.

Despite a small non-uniformity in heat flux, the temperature profile predicted at the resistor was very similar between the thermal-only and electro-thermal models. Hence, treating the heat flux as uniform in thermal simulations was deemed adequate.

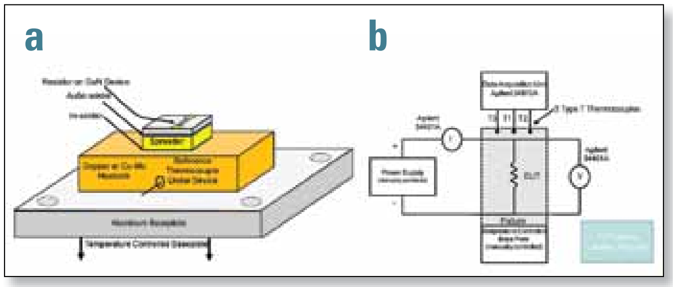

FIGURE 1: (a) Device and carrier stack-up, **(b)** schematic of resistance thermometry.

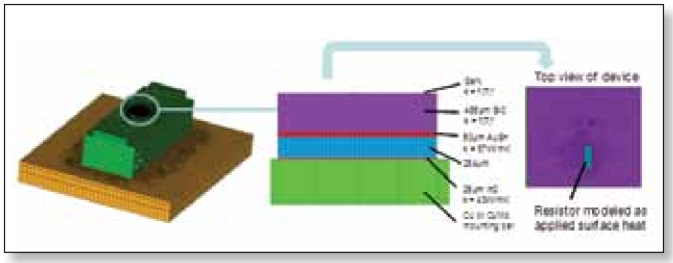

FIGURE 2: Details of the FE model.

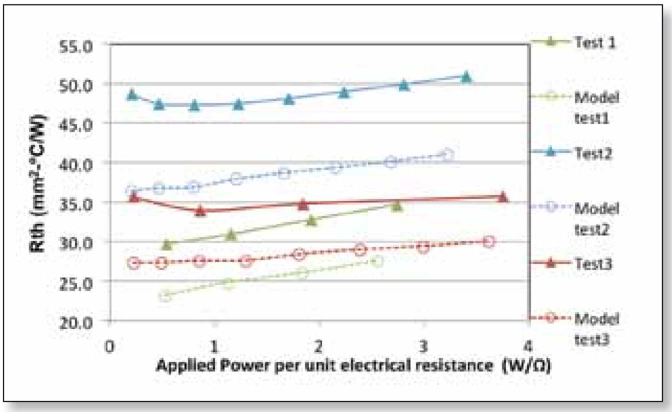

FIGURE 3: Comparison of measured and numerically predicted thermal resistance for three test configurations.

3) Uncertainty in the knowledge of material properties – Indium solder was estimated to be the primary contributor, and was a source of investigation as discussed below.

TEST INDUCED POTENTIAL ERRORS:

1) Heat loss from the test set-up to the environment – Any uncharacterized heat loss in equation (2) would result in the measured thermal resistance being lower rather than being higher than the model. Natural convection losses were assessed based upon a conservative heat transfer coefficient of 10W/m^{2}K and found to be negligible. There were no parasitic conduction paths present in the experiment.

2) Unintended introduction of electrical resistance or leakage current - This was illustrated by electro-thermal modeling conducted two ways, 1) keeping the electrical voltage the same as tests and computing the electrical current, and 2) keeping the electrical current the same as tests and computing the voltage drop across the resistor. The results are shown in Figure 5 for test 1 only, but the behavior remained similar for all tests.

As evident in Figure 5, models predicted a larger current for the same applied voltage as compared to tests. One potential explanation for this result is current leakage, perhaps to another electrical resistance in parallel. This is also consistent with the prediction of a lower voltage drop for the same current, as if an unintended electrical resistance was introduced in series with the Pt resistor. The reader may note that although the V-I behavior of tests and model looks similar in Figure 5, even a small difference can be quite substantial in terms of temperature due to the very small temperature coefficient of resistance of 0.003 Ω/Ω/ °C (Table 2).

If it is assumed that the same-voltage model (same as tests) best represents reality, an extraneous electrical resistance can be synthesized as a function of the missing current. This would, for example, be an electrical resistance due to poor electrical contact between the resistor and the underlying GaN layer to which it interfaces, among other possibilities. Figure 6 shows the predicted behavior of the potential extraneous electrical resistance, which exhibits good qualitative and quantitative correlation for all tests. On the other hand, if it is assumed that the same-current model represents reality, an additional resistance in series with the Pt resistor can be modeled, again shown in Figure 6. The behavior of the extraneous resistance appears to be consistent across different tests. The resistance in each case shows a strong non-ohmic behavior in which the slope of V-I curve is not constant.

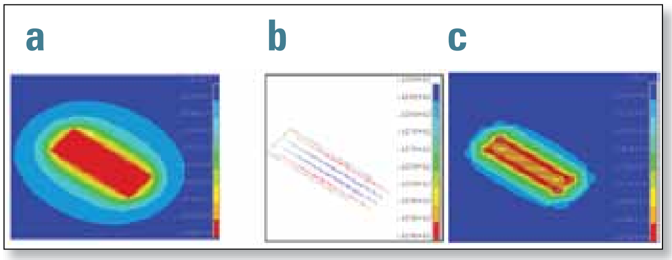

FIGURE 4: (a) Applied uniform heat flux in thermal only model (W/m^2), **(b)** computed non-uniform current density through the resistor from electro-thermal model (A/m^2), and **(c)** resulting non-uniform heat flux in electro-thermal model (W/m^2).

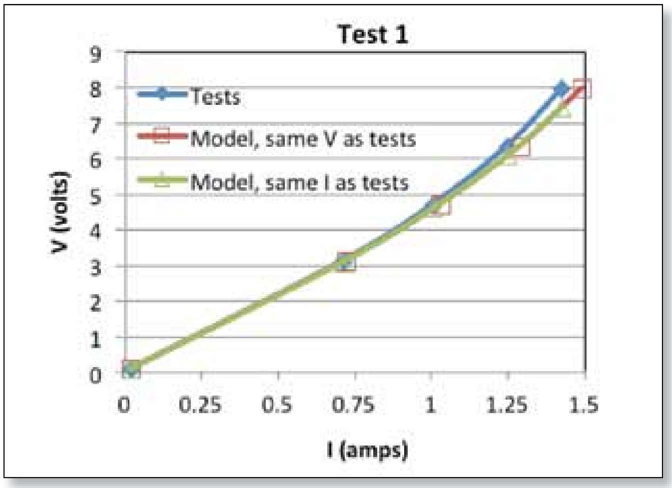

FIGURE 5: Comparison of measured and analytically predicted resistor V-I behavior for test configuration 1.

Alternatively, if a similar curve for thermal resistance is presented, as in Figure 7, a fairly constant missing thermal resistance of 6 mm^2-°C/W is observed for tests 1 and 3, and about 10 mm^2-°C/W for test 2. The electrical resistance in Figure 6 (a) and (b) and the thermal resistance in Figure 7 are all equivalent from the standpoint of explaining the discrepancies between the experimental data and analyses. Any of those could be the source of observed discrepancy in Figure 3.

Figures 6 and 7 illustrate that electrical resistance can appear as thermal resistance in tests and vice-versa. There

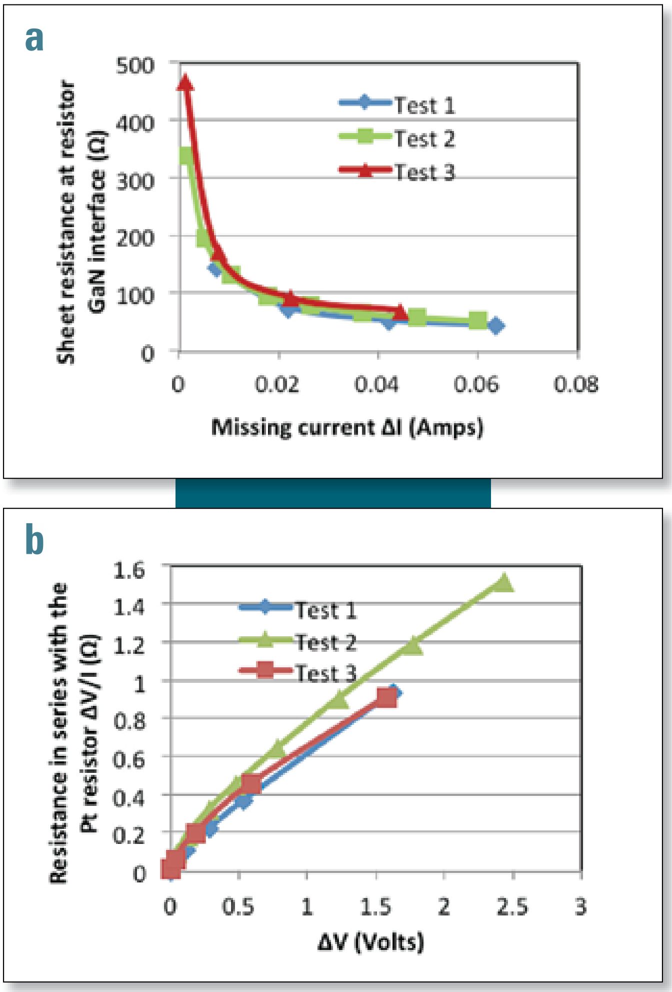

FIGURE 6: Extraneous resistance calculations based on electro-thermal modeling for each test case, **(a)** same-voltage model prediction, and **(b)** same-current model predictions

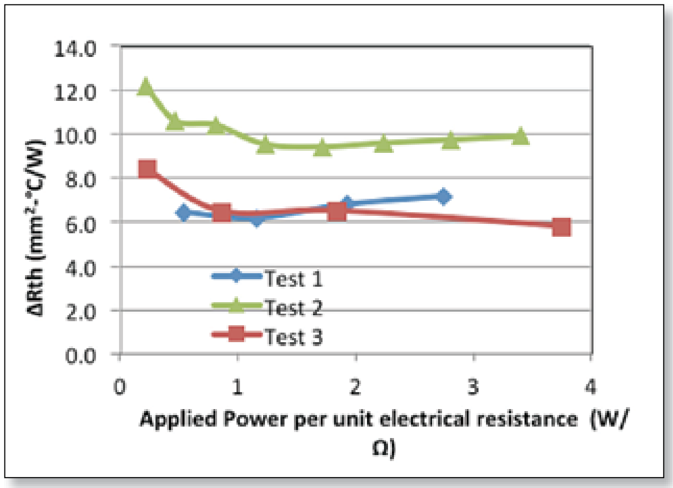

FIGURE 7: Thermal resistance delta between the test-measured and model-computed values

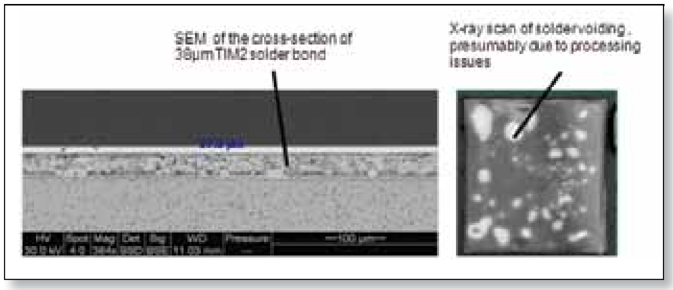

FIGURE 8: SEM picture of the cross-section through TIM2 solder and X-ray scan of the plan view.

is no easy way of distinguishing between the two, which leaves the experimentalist with the question as to whether thermal or electrical phenomena are responsible for the measured result, and therefore an inability to draw the desired conclusions on thermal performance.

To resolve this, SEM images of the device cross-section and X-Ray inspection was performed to evaluate the quality of the indium solder bond. As Figure 8 shows, indium solder was observed to be about 1.5-2X the expected thickness, was porous and exhibited voiding over approximately 50% of the area. These results and subsequent testing strongly pointed to a degraded thermal interface to be the most likely cause; however, it was not possible to definitively rule out the possibility of electrical phenomena influencing the measured thermal performance in experiments conducted using these custom resistor-thermometer devices.

CONCLUSIONS

The use of electrical resistance is prevalent as means to simultaneously dissipate heat and measure temperatures of simulated micro-electronic devices in their packaged environment. It's a time-tested technique that is robust and provides meaningful answers. However, just like any metrology method, it is not fool proof and there are pitfalls that an engineer must consider. This article summarizes some of the potential pitfalls, such as the intertwining of electrical and thermal resistance in certain situations, possibly leading to erroneous conclusions about thermal performance.

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Towards Reproducible ASTM D5470 Measurements at Lower Cost

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INTRODUCTION

ASTM D5470 (updated to ASTM D5470-12 in 2012) [1] remains an industry standard for characterizing thermal interface materials (TIMs) despite some drawbacks. Ultimately, a TIM must be tested in its application to conclude its merits. Standardized testing is useful, however, for comparing TIMs in research and development. It is also useful for customers to validate data provided by vendors. Several modifications to ASTM D5470 have emerged to improve the accuracy of TIM measurements, and to increase measurement precision [2, 3]. Such improvements, however, usually come with increased equipment cost, and they do not eliminate the need for testing in-applications, so the total cost for testing can be high. Further, reproducible measurements based on ASTM D5470 remain challenging to achieve, and recent studies to improve the accuracy of this standard have not focused on quantifying measurement reproducibility with large sample sets. The need for improved measurement reproducibility (e.g., a type of sample is measured, removed from the apparatus, and measured over many cycles with very similar results) is known to the community, and continues to limit cost-effective TIM development.

The approach to calculate the specific thermal resistance of a TIM based on ASTM D5470 measurements is

$$R = \frac{\Delta T}{Q} A_c, \qquad \textbf{(1)}$$

where ΔT is the difference between the upper interface temperature and the lower interface temperature of the sample, Q is the average heat rate through the TIM, and A_c is the effective contact area between reference bars and the TIM. The heat rate and interface temperatures are calculated from temperature measurements in the reference bars in contact with the TIM. The typical practice with ASTM D5470 is to use reference bars of equal cross sectional area [1]. The temperature profile in these bars is linear when they are insulated well, so a simple one-dimensional heat conduction analysis is used. But the simplified heat transfer analysis comes at the cost of making it difficult to align the reference bars with each other and the sample – four surfaces must be aligned. Misalignments reduce the effective contact area between the sample and the reference bars as shown in Figure 1a. Misalignments as low as 1% often go undetected and are difficult to control, yet they can propagate significant errors through the system, and make reproducible

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measurements difficult to achieve.

Because possible misalignments are usually neglected in uncertainty analysis, we could not find published experimental data that quantifies the role misalignments have in measurement uncertainty (this is done numerically in [4]). But our colleagues in industry and academia tell us that their data scatter for a large set of the same type of sample is often much larger than what their measurement uncertainty analysis predicts, even when considering reasonable variations in the properties of the samples. This is especially true for delicate nanomaterials (e.g., carbon nanotube TIMs [5]) and other samples that can be damaged while trying to optimize alignment of the reference bars.

This article highlights the "stepped-bar" modification of ASTM D5470 shown in Figure 1b. The modification can improve measurement reproducibility, while also reducing system cost. A comprehensive uncertainty analysis derived from the Kline and McClintock method for the stepped-bar ASTM D5470 is presented in [4]. This analysis shows that, in addition to high reproducibility, the stepped-bar approach can produce lower measurement uncertainty than the standard ASTM D5470 when very precise thermocouples (± 0.001 K) are used, and the mismatch in reference bar area alignment is greater than 1% in the standard approach. The reader is referred to [4] for a comprehensive description of the stepped-bar ASTM D5470 technique.

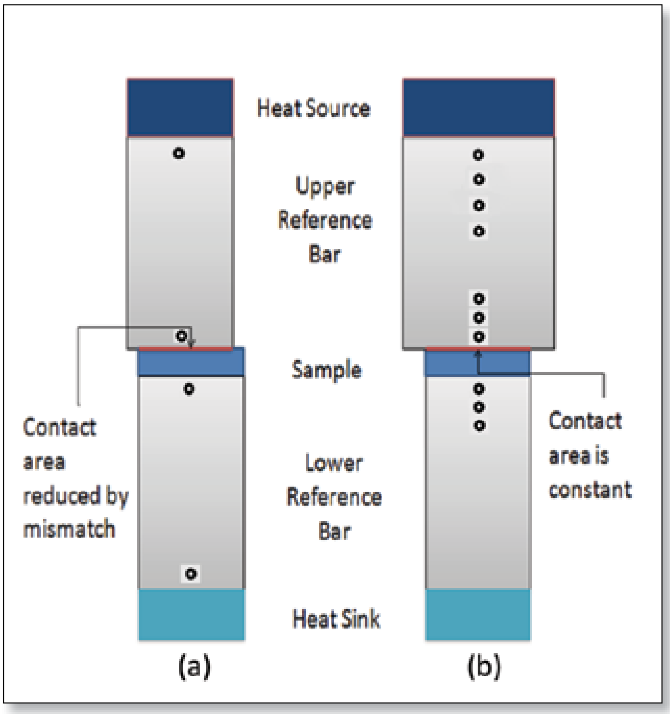

FIGURE 1: (a) Schematic of a standard ASTM D5470 apparatus. The contact area with the sample is reduced when the bars are not aligned. **(b)** Schematic of a stepped-bar ASTM D5470. The contact area with the sample is constant. The holes in **(a)** and **(b)** represent the suggested thermocouple placement (for accurate scale and additional details on thermocouple placement see [4]).

STEPPED-BAR ASTM D5470

The stepped-bar design oversizes the upper reference bar (URB) as shown in Figures 1b and 2. This modification allows machining errors and bar misalignments without a reduction in the contact area between the URB and the TIM. The operator only has to align the TIM to the lower reference bar (LRB) – a two surface alignment – rather than aligning the sample to both reference bars – a four surface alignment. This obviates the need for expensive bar alignment and loading mechanisms, which can often be the largest component costs in the system.

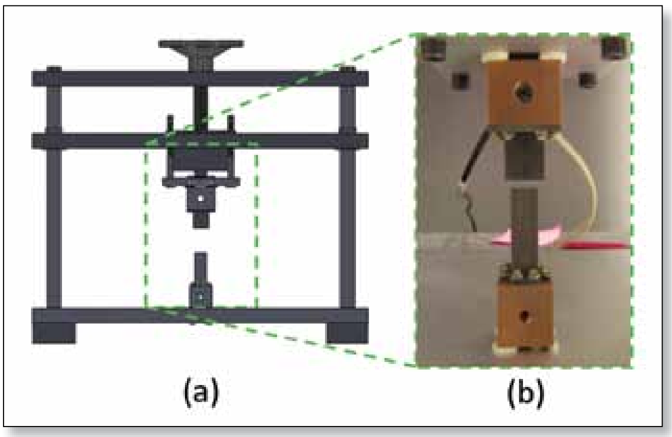

FIGURE 2: (a) Schematic of a stepped-bar ASTM D5470 apparatus. **(b)** Photo of the stepped-bar apparatus.

A mechanical transducer, comprised of a threaded rod and steel hand wheel, applies pressure to the TIM under test in the stepped-bar approach. The use of a mechanical transducer can greatly lower the cost (~50%) of the entire apparatus in comparison to a stepper motor or pneumatic-based loading system. Because instabilities of the threaded rod introduce imprecision in aligning the URB with the LRB, the oversized URB ensures that these misalignments do not reduce the contact area of the sample and introduce errors into the thermal resistance measurements. In the design shown in Figure 2, the URB has a square cross-sectional area measuring 1.4 cm to a side. And the LRB has a square cross-sectional area measuring 1.0 cm to a side. The URB and LRB are 1.5 cm and 3.0 cm long in the axial direction, respectively. Additional details of this design are reported elsewhere [4].

The major drawback of the stepped-bar approach is that heat flow is constricted from the URB to the TIM, resulting in a nonlinear temperature profile in the URB, so a simple one-dimensional heat conduction model cannot be used to determine the upper interface temperature. But this is addressed by fitting a 2nd order regression line through thermocouple readings near the TIM interface. Placement of several thermocouples near the TIM interface as shown in Figure 1b minimizes additional measurement uncertainty that could be introduced by the nonlinear regression near the interface.

Based on a numerical heat transfer analysis of the stepped-bar [4], the URB can be divided into two parts for curve fitting: 1) a linear fit to the top part of the URB, and 2) a 2nd order fit through the bottom of the URB. The linear fit to the top part of the URB is used to determine the rate of heat flow and the 2nd order fit extrapolates the upper interface temperature of the TIM. An example of this curve-fitting procedure is shown in Figure 3. The error bars arise from the precision of the thermocouples and their placement.

The oversized geometry of the URB, and dividing the URB into 2 regions for curve fitting are the major differences between the stepped-bar ASTM D5470 and the standard ASTM D5470. The temperature profile remains linear in the LRB for both approaches.

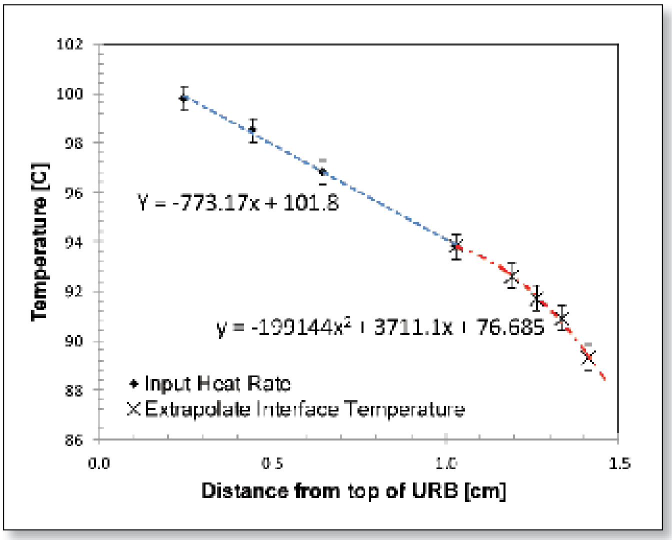

FIGURE 3: Curve-fitting procedure in upper reference bar of the stepped-bar ASTM D5470 for a representative measurement. The slope of the blue dashed line is used to determine the input heat rate. The red curve is used to extrapolate the interface temperature. This figure is reproduced from [4] with permission form ASME.

STEPPED-BAR MEASUREMENTS OF TIMS

The stepped-bar ASTM D5470 (aluminium 2024 reference bars with Ra ~ 0.5 μm, flatness = 0.1-0.3 μm) was used to characterize Arctic Silver 5 and Ceramique thermal paste [4]. A small amount of spacer-grade, soda lime glass microspheres (22-25 μm) from Cospheric was added to these pastes to maintain a constant bond-line thickness. Thermal resistances of 32 ± 4.5 mm^2K/W and 41 ± 4.5 mm^2K/W were measured at an

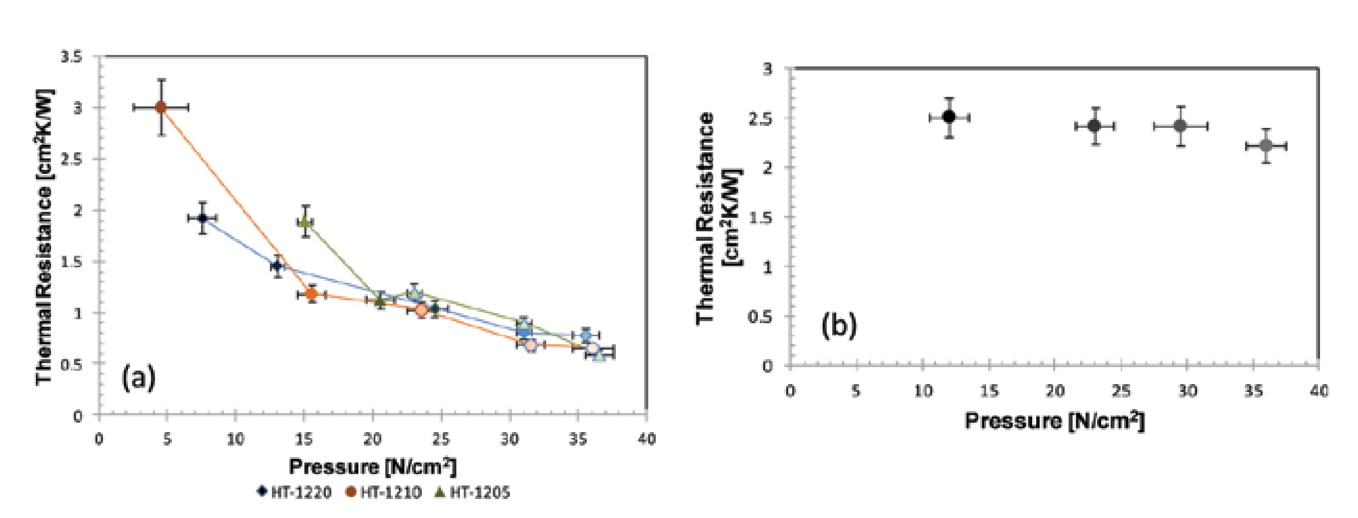

FIGURE 4: (a) Thermal resistance versus applied pressure for three different graphite pads from GrafTech.
(b) Thermal resistance versus applied pressure for aluminum foil 10 microns thick.

applied pressure of 300 kPa for Arctic Silver 5 and Ceramique, respectively. The United States National Renewable Energy Laboratory (NREL) reported a resistance of 30.9 mm^{2}K/W for Arctic Silver 5 with a bond line thickness of 23.5 um [6], which is similar to the value measured with the stepped-bar. The NREL study used an experimental apparatus based on the standard ASTM D5470 with reference bars polished to 0.5 µm. This result indicates that the stepped-bar approach can be implemented with no significant loss in measurement accuracy.

The thermal resistance of aluminium foil 10 microns thick and three graphite samples from GrafTech (HT-1220, HT-1210, and HT-1205) were also measured with the stepped bar. The thermal resistance versus applied pressure for these samples is shown in Figure 4. The measurements on thermal paste, graphite, and aluminium foil span an order of magnitude in thermal resistance, and show a range of practical resistance that can be characterized with the stepped-bar approach.

Stockwell Elastomeric TC100 thermal gap (1.575 mm thick, manufacturer's reported resistance of 12.12 cm^{2}K/W [7]) pad was also tested. The gap pad was tested at the manufacturer's specified pressure of 690 kPa. For each measurement, the sample was removed from the apparatus and reinserted to account for operator error in aligning the sample to the LRB. Figure 5 shows the frequency histogram for all measurements of the TC100 gap pad using the stepped-bar ASTM D5470 with stainless-steel reference bars. The average specific thermal resistance measurement was approximately 12.09 cm^{2}K/W. The standard deviation of the eighteen measurements was 0.38 cm^{2}K/W. A confidence interval based on the student's T distribution suggests that 95% of all measurements of the TC100 gap pad fall within 6.4% of the mean value. These results imply excellent repeatability of the stepped-bar

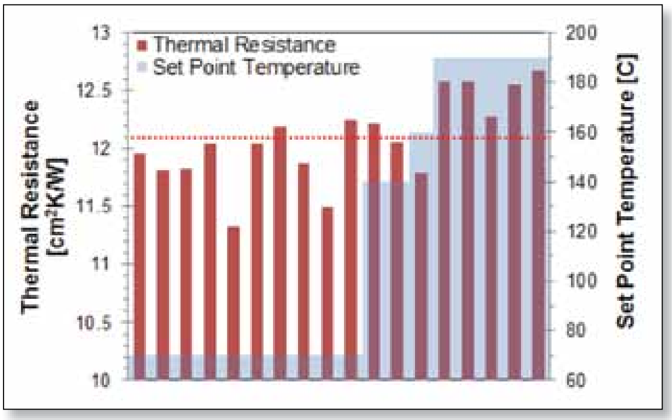

FIGURE 5: Frequency histogram of 18 independent thermal resistance measurements (red) of TC100 TIM. The sample was removed and reloaded in the system after each measurement. Manufacturer-specified thermal resistance of TC100 TIM is 12.12 cm^{2}K/W. The dotted red line indicates the average value of the thermal resistance measurements. Also shown is the upper set point temperature (blue) used in each measurement. This figure is reproduced from [4] with permission from ASME.

ASTM D5470 under these testing conditions. Likewise, the manufacturer-specified thermal resistance value of 12.12 cm^{2}K/W falls within this 95% confidence interval, suggesting excellent measurement accuracy.

CONCLUSION

This article highlights the importance of accounting for reference bar alignment for reproducible TIM measurements. A stepped-bar modification to ASTM D5470 [4] is discussed and shown to produce very reproducible and accurate measurements of a commercial thermal gap pad. The thermal resistance of Arctic Silver 5 was also measured to be in good agreement with other reports, which used the conventional ASTM D5470.

In order for the stepped-bar apparatus to achieve the same uncertainty as that of a conventional ASTM D5470 apparatus, more temperature probes are required. Each additional temperature probe increases the cost of the apparatus. However, the stepped-bar apparatus offsets this marginal expense because it utilizes an inexpensive mechanical transducer instead of more costly pneumatic-based alignment mechanisms that are required to precisely align reference bars of equal cross-section area. The stepped-bar ASTM D5470 is simple enough for a skilled technician to set up in one day when all parts are available, and the total cost of the parts is about $9,700 (for a parts list see [4]). This cost is about 3-5 times less than the cost of several commercial systems based on ASTM D5470.

A round robin of tests in different labs, and with several different TIMs, is ultimately required to conclude the superior reproducibility of stepped-bar ASTM D5470 approach. But there is a clear cost advantage, which could save resources for increased testing of TIMs in their application.

ACKNOWLEDGEMENTS

Assistance with data collection and analysis from Dakotah R. Thompson is appreciated.

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GREEN TECH
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Bitcoin 2-Phase Immersion Cooling
and the Implications for High Performance Computing

Alex Kampl
Allied Control Company

ABSTRACT

RECENTLY, BITCOIN and Bitcoin mining have aroused international interest. This article describes the cooling challenges faced by Bitcoin miners and discusses the implications on the future of cooling for supercomputers, HPC clusters and other high density electronics. We explain the inner workings of the first commercial open bath immersion cooling systems and how Bitcoiners seemingly refine the technology used to create high powered ASICs, and keep them cool.

BITCOIN

Bitcoin is a peer-to-peer payment system and cryptographic currency introduced as open-source software in 2009 [1]. Users install a free client (the wallet) onto their computer, which allows them to send and receive payments using Bitcoin addresses. At the time of this writing, more than 50,000 payments are sent on a daily basis. Participants known as "miners" verify transactions into blocks and broadcast them to the public block chain by employing a proof-of-work concept using a secure hashing algorithm (SHA-256). Miners get rewarded with 25 new Bitcoins in return for each block. To stabilize the block creation rate at one block about every 10 minutes, the network self-adjusts the difficulty of the hashing calculations. The cost of verifying transactions is the capital cost plus the power consumption of the hardware in use. The more computational power is employed to do the "hashing", the bigger the share of the reward that goes to the miner.

Miners initially employed conventional CPUs to perform the SHA-256 hashes. When GPUs (graphics processing units) were found to be more efficient, the cost to run CPUs quickly exceeded the profits that could be made with them. As Bitcoin grew in popularity, gamers realized that they were in possession of "money making machines", and the arms race for the most efficient mining hardware was on. What is now known as the "Bitcoin mining industry", moved through several hardware generations within two short years. This included FPGA educational kits, custom FPGA hardware with "beefier" power supplies, low-end ASIC chips working in parallel, to arrive at high-end 28nm and 20nm ASIC chips we see today. Power consumption per chip now exceeds that of high-grade gaming GPUs and supercomputer CPUs and accelerator cards (Table 1).

Today, mining is often conducted by industrial mining farms, with densely packaged hardware that becomes outdated within months of coming online as electricity costs exceed profits. The rapidly evolving power density of mining clusters coupled with their short life cycle makes deployment in conventional air cooled data centers challenging.

2-PHASE IMMERSION

2-phase immersion thermal management, Figure 1 is viewed by many as a viable technology for meeting the power density and energy efficiency needs of the high performance computing market. Power densities up to 100 times higher than a typical air cooled server have been cooled this way with efficiency superior to direct water cooling [2]. Though new technical approaches [3] simplify its adoption, 2-phase immersion cooling has been slow to catch on in the risk-averse IT industry.

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TABLE 1: EVOLUTION OF BITCOIN MINING HARDWARE

Type	Make / Model	Year	MH/s	W
CPU	Xeon E5530 2.40GHz	2009 Q4	7.14	80
GPU	ATI Radeon HD 5890	2010 Q1	245	192
GPU	ATI Radeon HD 6990	2011 Q1	800	450
FPGA	Xilinx Spartan-6	2012 Q1	245	10
FPGA	Xilinx Spartan-6 (4)	2012 Q2	850	40
ASIC	ASIC 130nm (32)	2013 Q1	12k	75
...	...	...	...	...
ASIC	ASIC 28nm (single)	2014 Q1	500k	500
ASIC	ASIC 20nm (single)	2014 Q2	750k	???

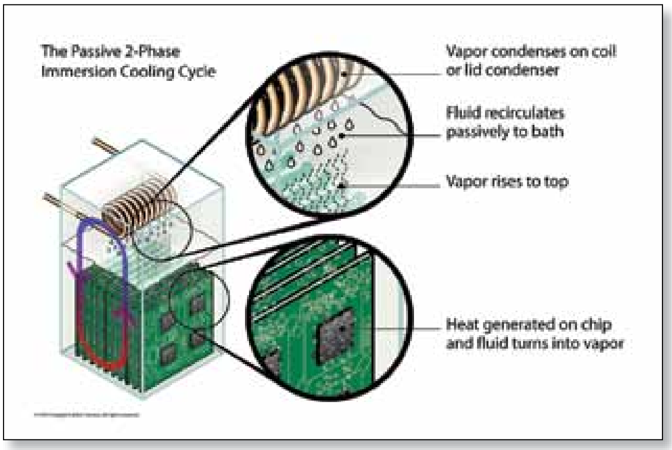

FIGURE 1: The passive 2-phase immersion cooling cycle.

FIGURE 2: A 28nm mining device to be connected to an external power supply.

FIGURE 3: A 500W 28nm ASIC mining chip, cooled by a PC water cooling system with a waterblock, pump, custom radiator and external cooling fans.

A primary hurdle to its adoption is the lack of energy-dense hardware. The cost and weight of fluid needed to fill a server chassis that is 95% air or more is prohibitive. Yet commodity hardware does not lend itself to density increases. Air cooling constrains the area of a motherboard and DIMMs, capacitors and connectors restrict the pitch between boards. For this reason, technology demonstrations to date have only been able to showcase the energy efficiency merits of the technology. Hardware sufficiently dense to showcase the density and resulting cost advantages has not been available except in specialized applications such as Bitcoin mining.

HEAT TRANSFER CHALLENGES

Keeping hardware cool, Figure 2, has proven to be a challenge right form the early days of custom Bitcoin mining hardware. FPGA chips used at or over the manufacturer specified limits down-clocked when overheating, resulting in lower hash rates. A number of commercial mining hardware manufacturers were forced to make last minute changes, such as adding unplanned additional fans and heat sinks, before delivering hardware to customers [1]. While the market has somewhat matured in the meantime, this remains a continuing trend.

As they are approaching the limits of traditional cooling methods, the latest high powered ASIC devices face a new problem altogether. Power trains and mining chips are exceeding heat dissipated by commercially available computer hardware, creating a significant amount of engineering overhead, and hardware often ships with throttled performance due to thermal constraints. Removing these thermal bottlenecks, and reducing the associated engineering overhead, is central to the value proposition of 2-phase immersion, Figure 3.

FIGURE 4: 3 tanks per 19-inch rack.

TABLE 2: IMMERSION-2 CONDENSER SPECS AT 30 LITER / MIN WATER FLOW			
Q (kW)	**Tin (ºC)**	**Tout (ºC)**	**DP (PSID)**
30.22	32	46.58	<0.5
26.09	36	48.6	<0.5
21.96	40	50.62	<0.5

IMMERSION-2 500KW BITCOIN MINING CLUSTER

Hong Kong, with its hot and humid climate, is a particularly challenging environment for data centers. With average Power Usage Effectiveness (PUE) of 2.52 [4] being the norm and pollution on the rise, companies need to be creative when it comes to IT cooling. The city is home to Immersion-2, and it comes as no surprise that its first large-scale implementation was a 500kW Bitcoin mining cluster.

Immersion-2 has a footprint smaller than a shipping container and is comprised of 20 conventional 19-inch racks, each housing 3 separate tanks or "baths", as shown in Figure 4. The computational hardware is comprised of 80W boards originally cooled with a large aluminum heat sink to which two fans would be attached. When deployed in the insulated stainless steel immersion tanks, 92 boards are stacked vertically on a backplane with less than 10mm board-to-board pitch (Figure 5). To reduce space and fluid usage, boards are arranged in pairs with component sides facing each other and through-hole components (i.e. fan connectors) are left unpopulated during production. The weight of the original 92 heat sinks is roughly the same as the weight of an empty tank that contains about 2.75liters of fluid per kW during operation.

CONDENSER FOR HOT WATER COOLING

When the system was put into operation, the 92 boards and 4 power supplies in each tank dissipated about 8kW, but the condenser in each bath is designed to accommodate 25kW at Hong Kong's hottest temperatures (Table 2), making it simple for the client to move through hardware generations. With possible water temperatures of 50°C or higher, the system can be run year-round with simple free cooling equipment. There are ports for two more condensers in each bath, allowing up to 75kW per tank or 225kW per rack. Baths of this density have already been demonstrated [5], as have boards packaged at up to 4kW per liter [3].

This scalability is central to the value proposition of 2-phase immersion. With the addition of more commodity dry tower hardware outside of the datacenter, the mechanical infrastructure can accommodate newer mining hardware with higher power densities. With boiling enhancement, emerging 1000W ASICS can be accommodated with the same fluid boiling temperature T_f=60C, allowing the facility to continue operating at PUE<1.02 in Hong Kong's hot summers. This efficiency is central to the value proposition, for its direct effect on income and hardware lifespan.

The custom tank condensers use enhanced tubes borrowed from the refrigeration industry. Each is fed facility water directly from a four module dry tower sized for Hong Kong's hot and humid weather (Table 3). The data center requires only a small air-conditioning unit for comfort cooling when people are present.

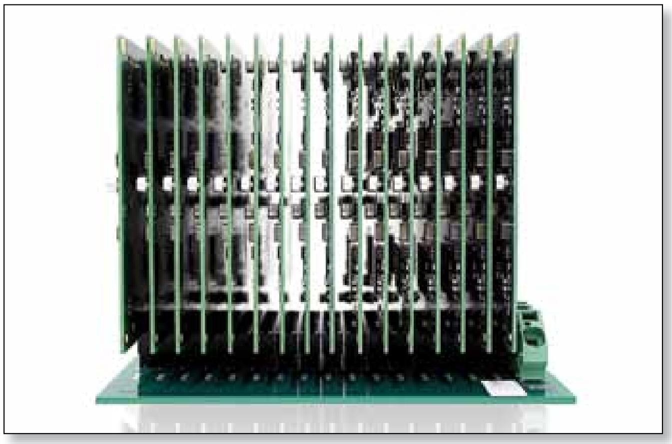

FIGURE 5: 92 boards on similar backplanes with less than 10mm distance board to board.

TABLE 3: 1.5kW COOL HUNDREDS OF KILOWATT ON 30 JANUARY 2014	
Outdoor Temperature:	24ºC
Relative Humidity:	64%
Water-In Temperature:	39.9ºC
Water-Out Temperature:	45.4ºC
Room Temperature:	27.6ºC
Radiator Power:	0.4kW
Pump Power:	1.1kW

FACILITY MANAGEMENT

Since the cooling system is operating isolated from the indoor environment, and the hardware is submerged in a constant temperature fluid, facility management and maintenance are reduced to a minimum. Without chillers or air handlers, there is no raised floor or dust that needs to be taken care of, and no static electricity that needs counter measures such as humidification. Environmental monitoring is carried out merely for statistical reasons. Instead vital water-in and out temperatures are monitored.

Though the hydrofluoroether working fluid is non-flammable, the buildings original water sprinkler system was kept in place for regulatory reasons. Should the sprinklers go off, the hardware is shielded from water, whereas the "outside" electrical wiring is well protected. Data centers using water sprinkler systems traditionally have to replace hardware after a catastrophic event. Ironically, after a fire in one of Google's data centers in 2010, it was reported that the sprinkler system did more damage than the fire itself [8].

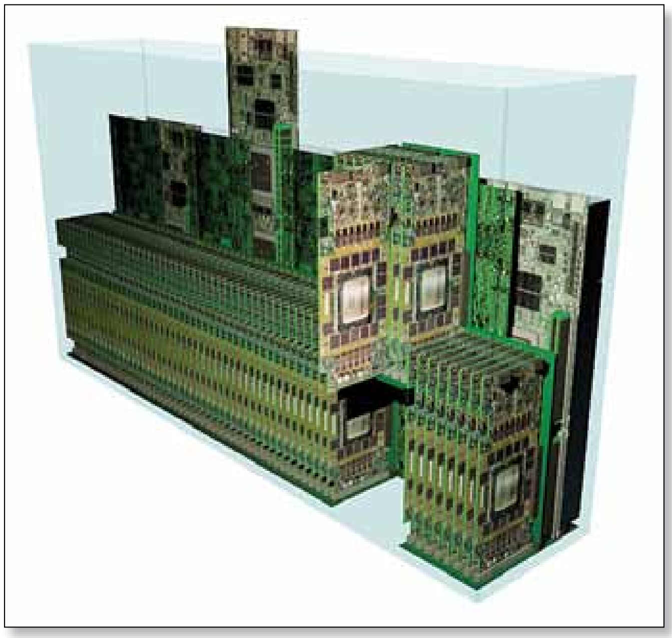

FIGURE 6: 2013 Immersion cooling concept for 64 Intel® Xeon Phi™ and 8 Intel® HPC mainboards with Infiniband® in a 3U "suitcase" form-factor (25kW)

POWER DELIVERY AND CABLING CHALLENGES

Some of the challenging aspects of the first installations were unrelated to cooling. In Bitcoin mining, power hungry ASICs are often restrained by thermal limitations in the power delivery portions of the system. Concerned about overheating, the primary manufacturer was unwilling to provide a backplane with sufficient power density. As with many other components for such an unusual application, the backplane was eventually designed and assembled in-house. Tasks like LAN wiring can become an art form when 92 Ethernet cables need to go in the smallest space possible without obstructing the way in and out for hardware. Standard RJ45 connectors suddenly seem oversized, leading to the idea of stacking boards face to face and removing the outer cable jacketing. It is these small take-home lessons that will prove invaluable when designing dense immersion hardware for HPC or cloud computing. Large-size connectors and cables don't seem to be the way forward, creating an opportunity for new connector and power solutions.

MATERIAL COMPATIBILITY

When Immersion-2's predecessor went into operation in 2012, it consisted of 24 tanks totaling 70kW of FPGA hardware, and relied on power and USB cables for its operation. Each tank contained over 2 kg of off-the-shelf, polyvinylchloride (PVC)-clad USB cables. Upon dismantling the system the following year, it was observed that the dioctyl phthalate (DOP) oil used to plasticize the insulation had been extracted. This caused the cables to become thinner and more rigid in the vapor region above the fluid, although no failures were ever observed. 20 grams of DOP were absorbed by passive carbon filters inside each tank, and a similar amount of DOP was later extracted from the fluid, with no degradation of boiling performance observed during the system's lifespan.

Full immersion has a positive impact on hardware reliability, due to hardware not being exposed to temperature fluctuations, uniform temperature across components, and elimination of the risk of electrostatic discharge in dry air. Without doubt, hardware failure will never be completely eliminated. Designing power supplies and backplanes without heat constraints can be less of a headache, but practical considerations need to be taken into account: the rules of hot swapping, redundancy, and systems protection are changed, due to the increased number of nodes.

HARD DRIVES AND IMMERSION

Another challenge has been building systems with the requirement for external storage. Traditional HDDs and immersion systems don't get along well due to the mechanical structure of HDDs. In prototype setups the easy fix has been the use of solid state drives (SSDs) or leaving storage devices in adjacent air cooled enclosures. Experiments have been performed with keeping spinning hard drives in the head space of immersion tanks. The latest advances in HDD development may solve this challenge altogether. The first generation of hermetically sealed Helium-filled hard drives, aiming for increased capacity and speed, became available at the end of 2013.

THE PATH FORWARD (SUPERCOMPUTERS)

Though the hardware replacement cycle tends to be faster in the mining world, there are strong parallels between this market and the high performance computing market. Tianhe-2, the world's fastest supercomputer, is comprised of 16,000 nodes, each containing two Intel™ Xeon™ Ivy-Bridge processors and three 250W Xeon™ Phi co-processors, Figure 6 It consumes 17.8MW with an additional 6.4MW reported for cooling, resulting in a calculated PUE of 1.36. If this could be reduced to 1.05, Tianhe-2 would save 48 million kWhr per year with the potential to boost its 40th place standing in the Green 500 [6]. The resources that went into the development, validation and deployment of the closed loop water-air hybrid cooling system could have been avoided [7]. If conventions were established, Tianhe-3 might be deployed more rapidly with the same mechanical infrastructure and increased reliability. Immersion systems have already been built that show the functionality of high speed copper and optical interconnects in the immersion environment.

CHANGING THE RULES

Bitcoin is perhaps an ideal incubator for 2-phase immersion. With a basic system, developers have the luxury of quietly (both literally and figuratively) refining the technology on their own terms while exploring the reliability, serviceability and safety of the technology. It might seem unlikely that Bitcoin miners would be the ones to redefine thermal limits, but there's an interesting precedent in the Bitcoin hardware industry. Professor Michael Bedford Taylor, who heads the Center for Dark Silicon at the University of California at San Diego (UCSD), is the author of a paper describing how Bitcoiners have disregarded all traditional rules of chip design, "leading to the development of machines that had orders of magnitude better performance than what Dell, Intel, NVidia, AMD or Xilinx could provide" [1]. Taylor, who was among the developers of the TILERA many-core computing architecture, says this path was "unheard of in modern times, where last-generation chip efforts are said to cost $100 million or more and the number of ASIC starts drop yearly."

FULL DISCLOSURE

Alex and his company have no horse in the Bitcoin race, other than building systems and consulting for a client in the Bitcoin industry.

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Relationship between Supply Flow Rate of Small Cooling Fans and Narrow Flow Passages in High-Density Packaging Electronic Equipment

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INTRODUCTION

FORCED CONVECTION driven by cooling fans is widely used for removing heat from electronic equipment. A net cooling performance of the cooling fans is significantly dependent on a supply flow rate. Therefore, accurate prediction of cooling fan performance is extremely important in the thermal design of fan-cooled electronic equipment.

Generally, the supply flow rate of the fans is decided by the intersection of its pressure (ΔP) – *flow rate* (Q) characteristic curve, which shows the relationship between the pressure rise at the fan (ΔP) and the supply flow rate (Q), and a flow resistance curve of electronic equipment. In recent years, electronic equipment has become smaller and thinner while their performance increases and their functions become more complex. As a result, a lot of electrical devices are mounted in electronic equipment and the airflow passage in high-density packaging electronic equipment such as SMPS (Switched-Mode Power Supply), laser printers, lap top computers and servers becomes narrow and complex because gaps between mounted components generally become the flow passage. The pressure drop characteristic in such equipment may not be predicted easily by using well-known basic pressure drop characteristics [1]. In addition, several components such as heat sinks, capacitors and an enclosure are installed near the fan as shown in Fig. 1. This may affect the fan performance itself [2]. Several researchers have evaluated the fan performance when the components are mounted near the fan [3-5]. Therefore, the accurate prediction of the supply flow rate of the fan mounted in equipment is generally difficult. A further investigation of how the accurate supply flow rate of the fan mounted in electronic equipment is predicted rapidly and easily is required in order to shorten a design period while maintaining reliability of products.

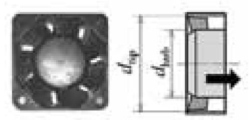
With this as a background, this present study focuses on an investigation of the supply flow rate in electronic equipment [2, 6]. In this article, the relationship between the supply flow rate of the small axial fan which is mounted at the outlet of the enclosure and the flow passage area in electronic equipment is reported as an example of our investigation. To investigate a change of the fan's flow rate in high-density packaging electronic equipment, a test enclosure which includes a test fan and an obstruction was prepared. The obstruction simulated electrical components in front of the fan. A change of

TABLE 1: DETAILS OF TEST FANS.

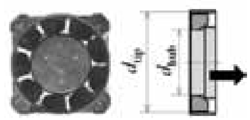
Parameter	Fan (A)	Fan (B)
Number of blades	7	9
Tip diameter d_{tip} [mm]	38.0	38.3
Hub diameter d_{hub} [mm]	26.8	25.1
Hub: tip ratio d_{hub}/d_{tip} [–]	0.71	0.66
Thickness of fan case [mm]	15.4	10.0
Normal speed [rpm]	7700	5700
Normal voltage [V]	12	24

➡ : flow direction

(Fan (A))



(Fan (B))



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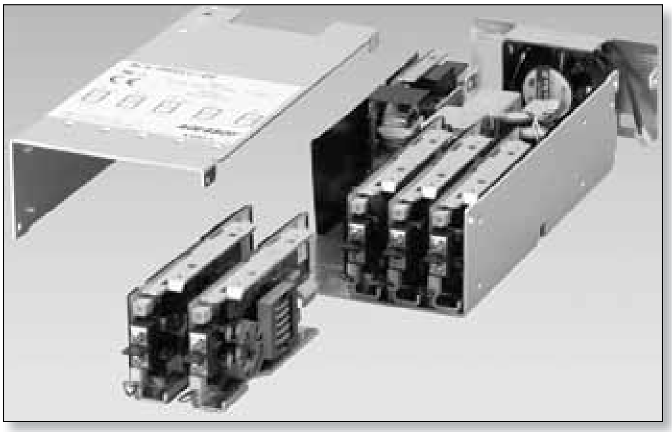

FIGURE 1: High-density packaging electronic equipment with axial fan (SMPS).

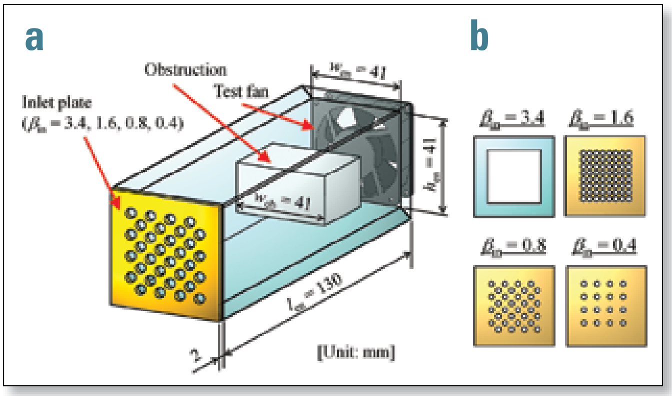

FIGURE 3: Schematic of test enclosure. **(a)** Test enclosure with fan **(b)** Inlet plate geometry.

the supply flow rate of the fan was measured while changing the obstruction and an opening area of an air inlet of the enclosure. We then explored the relationship between the supply flow rate and the flow pass area in order to obtain information for estimating the supply flow rate easily. Here, in this article, we investigated the supply flow rate when electronic equipment is mounted at the upstream side of test fans. Moreover we assumed that one axial fan is mounted at the air outlet of electronic equipment and fan-mounted electronic equipment operates in ambient atmosphere.

MEASUREMENT SYSTEM OF SUPPLY FLOW RATE

Figure 2 shows the schematic of our system for measuring the supply flow rate of the fan mounted in the test enclosure. It comprises an enclosure part that models the external enclosure of electronic equipment and the fan performance measurement system designed by Nakamura and Igarashi [7] based on JBMS-72-2003 [8]. This system is made up of an enclosure part with a test fan, a chamber part, an orifice, a valve, and an assist fan. Removal of the enclosure converts the system to the JBMS-72-2003 measurement system. The flow rate, Q, is measured at the orifice. An analog valve and the assist fan can be used for controlling the static pressure in the chamber. As mentioned

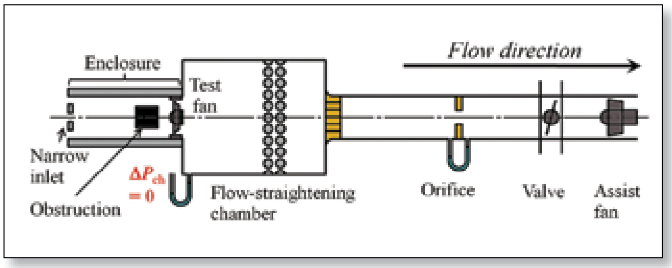

FIGURE 2: Schematic of the wind tunnel for measuring the supply flow rate.

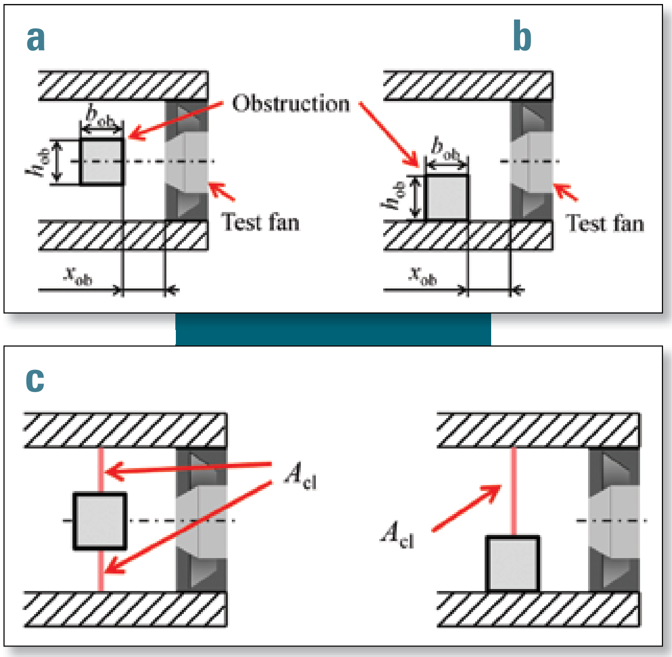

FIGURE 4: Mounting position of obstruction. **(a)** At the center of the test enclosure **(b)** On the bottom of the test enclosure **(c)** Position of A_{cl}

above, we investigated the supply flow rate of the fan when the fan-mounted electronic equipment operates in ambient atmosphere. Therefore in this study, the supply flow rate of the test fan when ΔP_{ch} = 0 Pa was measured while changing the opening area of the narrow inlet and the obstruction. The static pressure difference ΔP_{ch} was measured with a highly accurate differential pressure gauge (Shibata Kagaku, ISP-350, range; 0 – 500 Pa).

TEST FANS

Table 1 shows the details of the test fans. In this study, two types of 40 mm-scale fans, with a fan case of about 40 mm × 40 mm, were measured. Here, d_{tip} is a fan tip diameter and d_{hub} is a fan hub diameter. When we conduct the measurement, the voltage was adjusted to run the fan at a rated rotation speed, which was checked by a stroboscope.

TEST ENCLOSURE

Figure 3 (a) shows a schematic diagram of the test enclosure used in this study. Air flows into the enclosure from the surroundings through an inlet and exhausted to the atmosphere

TABLE 2: OPENING AREA OF ENCLOSURE INLET.		
β_{in}	Hole Number	A_{in} [mm²]
3.4	-	1681
1.6	64	804
0.8	32	402
0.4	16	201

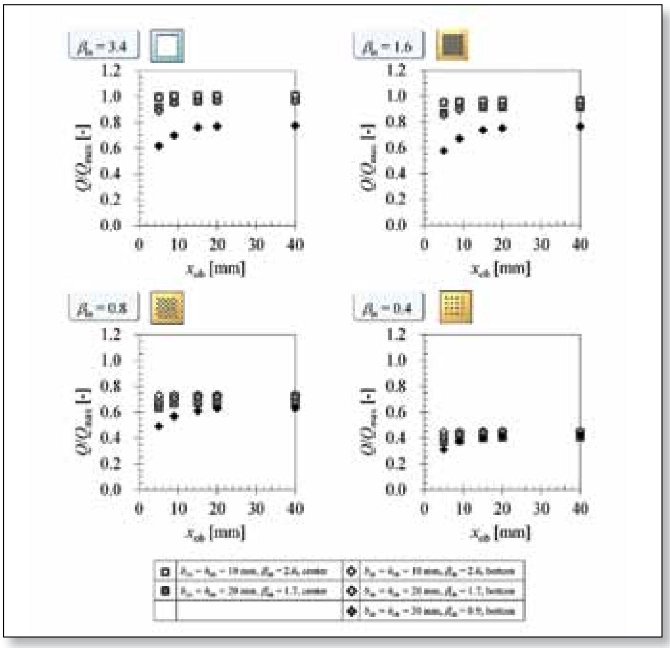

FIGURE 5: Supply flow rate of fan (A) versus distance of obstruction from fan inlet (x_{ob}) for different values of obstacle dimensions.

TABLE 3: CONDITIONS OF OBSTRUCTION.		
β_{ob}	β_{ob}, h_{ob} [mm]	x_{ob} [mm]
2.6	10	5, 9, 15, 20, 40
1.7	20	
0.9	30	

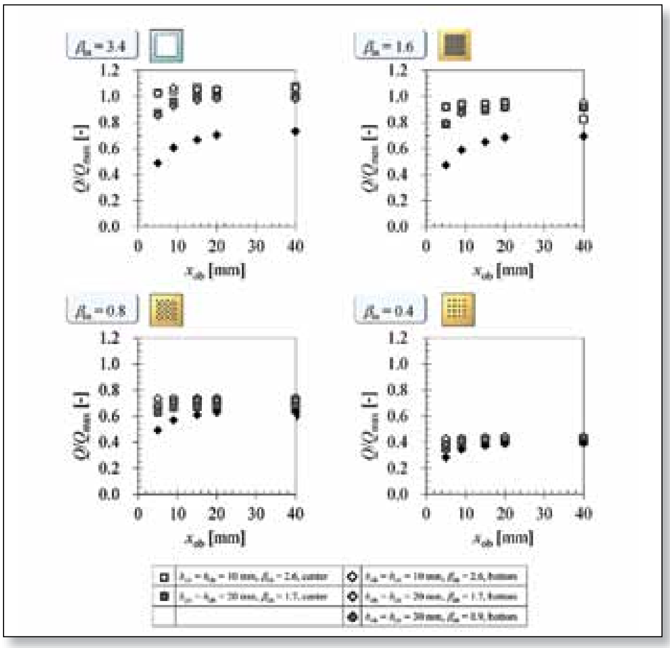

FIGURE 6: Supply flow rate of fan (B) versus distance of obstruction from fan inlet (x_{ob}) for different values of obstacle dimensions.

via the test fan. The width and the height of the enclosure (w_{en}, h_{en}) were set at 41 mm and the length l_{en} was set at 130 mm. Figure 3 (b) shows the shapes of the enclosure inlet. Table 2 shows the list of the total inlet area. Five types of the inlet plate were used. The condition of the area of the inlet was evaluated by using β_{in}. This is the ratio of the total inlet area A_{in} divided by the fan flow area A_{tip}. A_{tip} is expressed using the following relationships. Here, A_s is the profile area of the struts between the casing and the hub.

$$A_{tip} = \frac{\pi}{4}(d_{tip}^2 - d_{hub}^2) - A_s \text{ [mm}^2\text{]} \quad \textbf{(1)}$$

β_{in} is defined as the following formula.

$$\beta_{in} = \frac{A_{in}}{A_{tip}} \text{ [-]} \quad \textbf{(2)}$$

In actual electronic equipment, the inlet area is varied according to the air inlet structure such as the existence of perforated plates and filters for a dust control. Therefore the value of β_{in} was set at between 0.4 and 3.4.

Figure 4 and Table 3 show the details of the obstruction mounted in the enclosure. To simulate the actual electrical components in electronic equipment, a rectangular obstruction was mounted in front of the fan while changing the dimensions of the obstruction and the mounting position. Here, the ratio of flow passage area A_{cl} divided by the fan flow area A_{tip} is defined as the flow area ratio β_{ob}. Here, A_{cl} is defined as:

$$A_{cl} = h_{en}w_{en} - h_{ob}w_{ob} \text{ [mm}^2\text{]} \quad \textbf{(3)}$$

β_{ob} is expressed using the following formula:

$$\beta_{ob} = \frac{A_{cl}}{A_{tip}} \text{ [-]} \quad \textbf{(4)}$$

The value of β_{ob} was set at between 0.9 and 2.6. The distance between the fan and the obstruction was changed from 5 mm to 40 mm.

EXPERIMENTAL RESULTS

Figures 5 and 6 show the change of the operating flow rate of each fan when the enclosure is mounted in front of the fan. Here, we evaluated the supply flow rate by using the non-dimensional flow rate (Q / Q_{max}). Q_{max} is the flow rate when there is no enclosure and obstruction.

The supply flow rate of the fan decreases when β_{in} becomes smaller or the dimensions of the obstruction becomes bigger (β_{ob} becomes smaller). The deterioration of the flow rate is caused by the increase of the pressure drop at the inlet and the obstruction. When β_{in} or β_{ob} becomes smaller, the flow pass becomes narrow. This causes the significant pressure drop. This tendency can be observed regardless of the type of the test fans.

We investigate the relationship between the supply flow rate and each opening area ratio. The deterioration of the flow rate becomes significant when β_{in} becomes smaller than 1.0. Even if β_{in} is larger than 1.0, the supply flow rate decreases when β_{ob} = 0.9. Here, Fig. 7 shows the relationship among the supply flow rate, β_{ob} and β_{in}. The supply flow rate approaches the maximum flow rate in the case that both β_{ob} and β_{in} becomes larger than 1.0. When either β_{ob} or β_{in} becomes smaller than 1.0, the deterioration of the supply flow rate is caused.

From these results, we can conclude that the supply flow rate of the fan is decreased according to the flow pass area. Of course, the fan's supply flow rate deteriorates when the number of the mounted components increases. The components increase the pressure drop in the enclosure regardless of their dimensions. However, when the flow pass area in electronic equipment becomes smaller than the fan's flow area, the deterioration of the supply flow rate becomes significant. On the other hand, when the flow pass area in the enclosure is larger than 1.0, the deterioration of the flow rate can be inhibited.

Here, when the dimensions of the obstruction become larger, the distance between the fan and the obstruction x_{ob} also affects the supply flow rate; the supply flow rate decreases when the position of the obstruction is near the fan. We previously reported that the fan performance itself deteriorates when the large obstruction is mounted in front of the fan [6]. In this case, the large obstruction affects the inlet flow to the fan and the fan performance itself may be deteriorated. In order to predict the correct supply flow rate regardless of the deterioration of the fan performance, the further investigation about the relationship between the obstruction near the fan and the fan performance should be additionally investigated.

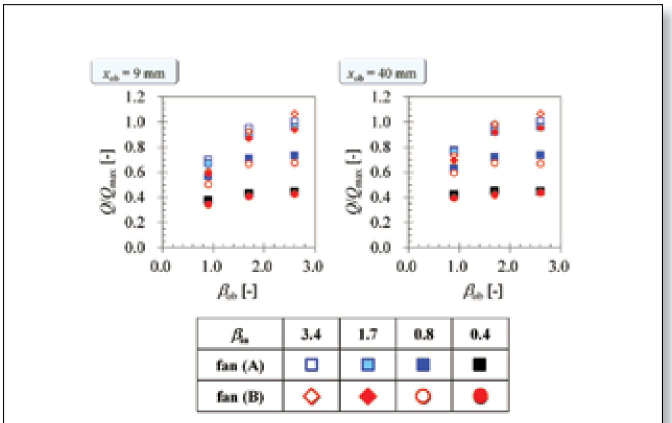

FIGURE 7: Relationship between opening area ratio and supply flow rate of each fan.

SUMMARY

In this article, the relationship between the supply flow rate of the axial fan in high-density packaging electronic equipment and the flow passage area is investigated experimentally by using the test enclosure. When the flow passage area in the enclosure becomes smaller than the fan's flow area, the supply flow rate of the fan significantly decreases. In order to avoid the deterioration of the supply flow rate, flow passage area should be larger than the fan's flow area. The obtained results may be used for estimating the supply flow rate of the fan easily in a design early stage.

For future study, an additional investigation of the pressure drop characteristic and the fan performance characteristic in high-density packaging electronic equipment may be meaningful in order to confirm the reproducibility of our results. Now, we are trying a development of detailed database of the pressure drop characteristic in high-density packaging electronic equipment. We will discuss whether our results can be applied regardless of the structure of electronic equipment. There is still room for developing methodology to apply our investigation to thermal design methods such as CFD analysis and flow and thermal resistance network analysis [9] in order to predict the supply flow rate of the fan in the enclosure rapidly and to shorten the thermal design period.

Note: *To view the nomenclature and subscripts for this article, see page 48.*

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Ultra-Thin Titanium Based Thermal Solution for Electronic Applications

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INTRODUCTION

AS ELECTRONIC system technology advances with continual increases in requirements leading to greater demand for higher power consumption, there have been growing challenges related to the design of thermal engineering and heat rejection technologies. The need for performance inevitably leads to operation of most electronic systems at the limits of the available thermal management technology. Today, one widely used method of thermal management in microprocessor and semiconductor chips is the heat pipe, due to its simplicity, reliability, practicality, and low-cost. However, conventional heat pipes have thermal transport and geometric limitations.

A thermal ground plane (TGP) is basically a flat heat pipe or vapor chamber type heat pipe. The TGP will expand upon the 2-phase cooling approach utilized in heat pipes and minimize issues relating to temperature gradients, increased weight, or added complexity. An important feature of the intended TGP technology is compatibility with existing chips and electronic devices without redesign of those systems; insertion of TGPs into these systems can provide new engineering margins yielding increased power use for the system, reduced operating temperatures, or reduced size of other components in the thermal management system.

PREVIOUS APPROACHES:

Early attempts to use TGPs for cooling electronics can be traced back to the 1970s [1]. In retrospect, the path forward has indeed been elusive. At first, simple cylindrical heat pipes were embedded in copper or aluminum plates. The heat pipes were bonded into holes drilled into the plate material. These devices were on the order of 10 mm thick. They were heavy, and thermal conductance was poor (~0.1 W/cm^2-°C) due to the bondline thermal resistance between the plate and the heat pipes. In an attempt to provide a thinner TGP, thin-wall cylindrical heat pipes were flattened, and bonded between two aluminum facesheets. Although these TGPs were thinner (~4 mm overall thickness), thermal conductance remained poor, because of the bondline between the heat pipes and facesheets. Moreover, these TGPs were not tolerant to internal temporal working fluid pressure variations caused by temperature. The thin-wall flattened heat pipes tended toward their naturally rounded configuration at high operating temperatures associated with qualification tests (>100°C) or high altitude aircraft and spacecraft applications (>80°C). This resulted in flexing the circuit boards and associated solder joints.

Subsequently, vapor chambers [2] were developed. The vapor chambers were basically flat heat pipes that eliminated the individually embedded heat pipes of the previous designs, thereby eliminating the

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George Fleischman worked nearly 7 years for TRW (now Northrop Grumman) on heat pipe technology. He worked at Hughes Aircraft (now Boeing) 24 years on heat pipes for satellite thermal control. While at Hughes George was the principal investigator or co-investigator for a total of four 0-g experiments flown on the space shuttle. He is the principal author or co-author of nineteen technical papers on heat pipe technology, and co-inventor of five patents. George retired in 2010 after working 10 years for Raytheon in El Segundo. He received his B.S. and M.S. degrees from Cornell University.

TABLE 1: PROPERTIES OF ALUMINUM, COPPER AND TITANIUM						
	Strength / Weight (kN-m/kg)	Yield Stress (MPa)	Density (kg/m^3)	CTE (ppm/°C)	Thermal Conductivity (W/m-°C)	Electrical Resistivity (Ω-m)
Titanium (99%)	288	830	4510	9.5	19	47.8E-08
Copper (OFHC)	24.7	70	8930	16.7	395	1.67E-08
Aluminum (606-T6)	214	400	2700	22.2	154	2.65E-08

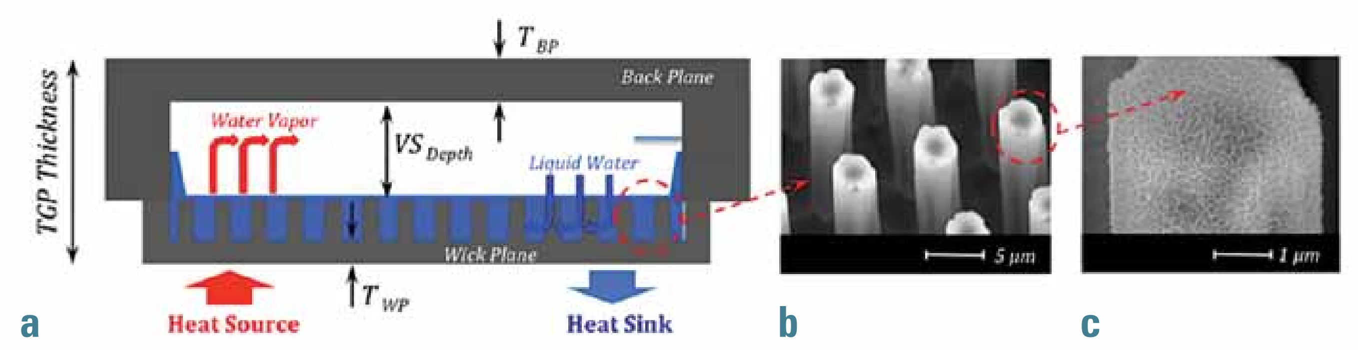

FIGURE 1: (a) Ti-TGP operation **(b)** Micro-scale wicks **(c)** Coated nanostructure titania (NST).

bondline between these heat pipes and facesheets. Vapor chamber TGPs typically used fine mesh wire screens or sintered powdered wicks leading to high thermal resistance to conduct heat into the wick material, at high heat flux levels, and excessive blockage of vapor space. For manufacturing reasons these vapor chambers were constructed of copper. However, copper has relatively poor structural properties, and this approach resulted in thick (~5 mm), heavy units. Moreover, copper has a higher coefficient of linear thermal expansion (CTE) relative to silicon (namely, 16.7 ppm/°C versus 2.6 ppm/°C, respectively) resulting in delamination of components and cracking in solder joints.

THE TITANIUM BASED APPROACH

The titanium based thermal ground plane (Ti-TGP) [3] was developed in response to advanced portable semiconductor and aerospace applications that are searching for ultra-thin, flat, lightweight and reliable thermal solutions.

Titanium has superior mechanical and electrical properties compared to copper or other conventional materials that have been used in heat pipes, Table 1. Titanium has: i) higher strength to weight ratio, ii) CTE closer to silicon which provides an improved thermal match between silicon based chips and the thermal solution, iii) higher corrosion resistance and, iv) compatibility with water.

Although the thermal conductivity of titanium is relatively lower than copper, the vapor chamber facesheets can be made 3 to 4 times thinner than a copper TGP. Therefore, the temperature drop for conducting heat into or out of the panel is not significant. For example, for a given budget thickness of a 4 mm TGP, the facesheet of titanium can be as thin as 500 μm, while the copper facesheet is required to be 1.5 mm thick in order to withstand the vapor pressure. That provides a 3 mm vapor space for the titanium TGP, while a copper TGP can only have a 1 mm vapor space. The temperature drop across a titanium facesheet would be ~2.5°C for a heat flux of 10 W/cm^2 compared with ~0.5°C for a copper TGP. This difference of ~2°C is a small penalty for the advantages of using titanium.

Generally, TGPs (flat vapor chambers) consist of two main structures; wick and back planes that are brought together, charged with working fluid, and sealed. The TGP cross-section and internal wick details are given in Figure 1. The overall thickness is calculated by adding the vapor space depth (VS_{Depth}) to the thickness of the wick and the back planes (T_{WP} and T_{BP}) as shown in Figure 1a. For a given TGP thickness budget, the vapor space depth is determined based on the required thermal metrics regardless of the material used. However, the thickness of the wick plane (excluding wick depth) and back plane are dependent on the material. These are the only two parameters that can be used to reduce the overall thickness. The high fracture toughness and yield stress of titanium compared to copper or aluminum allows both T_{WP}

and T_{BP} to be as thin as 150 μm without suffering mechanical failure, resulting in an ultra-thin TGP (600 to 900 μm) that can withstand the internal pressure of the working fluid.

The multi-scale fabrication capability of titanium is another attractive feature. It can be either macro-machined using traditional machining processes or, micro-fabricated using micro-patterned masks and wet or dry etching to fabricate features having dimensions of 5 to 100 μm, Figure 1(b). Titanium can also be coated with nanostructure on the micro-scale wicks to generate a super hydrophilic surface (~0° wetting angle). Wettability of the titanium-water interface is an important factor in wicking velocity, which drives heat flow rate. The wick surfaces are enhanced by a chemical process to generate a highly porous surface called Nano-Structured-Titania (NST) [6], with pore features on the order of 100nm, Figure 1(c). The Ti-TGP is then hermetically sealed by micro-laser welding. [3,5]

The Ti-TGP has been customized for heat load capacities from 1W up to 1KW [3] with thermal conductance of 45 W/°C and 27 W/°C, based on average evaporator and condenser temperatures, for thickness of 5 and 3 mm, respectively. Figure 2 shows an ultra-thin and portless Ti-TGP, weighing 1 gram with thickness of 900 μm and overall dimensions of 50 mm X 8 mm. Figure 2a is a photograph of the plan view, whereas Figure 2b shows the edge view of the actual TGP.

Another attractive feature of titanium is scalability and conformability that allows the Ti-TGP to be designed and fabricated into predefined 2D and 3D shapes (Figure 3).

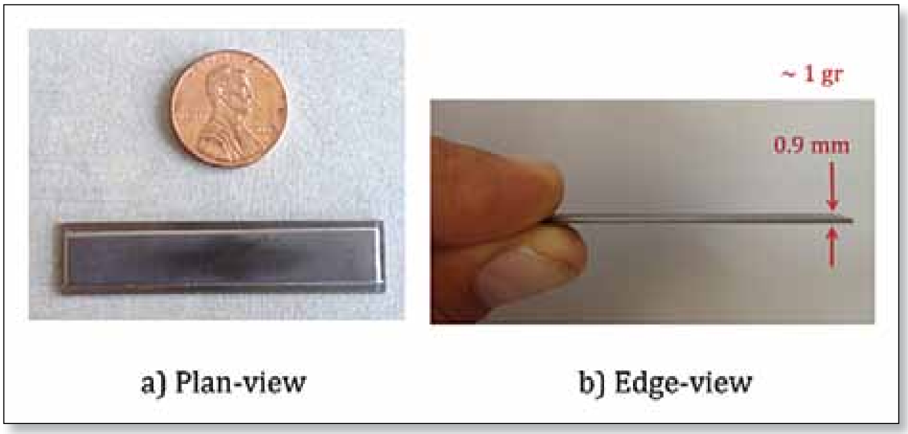

FIGURE 2: The ultra-thin and portless Ti-TGP (50 mm X 8 mm X 0.9 mm).

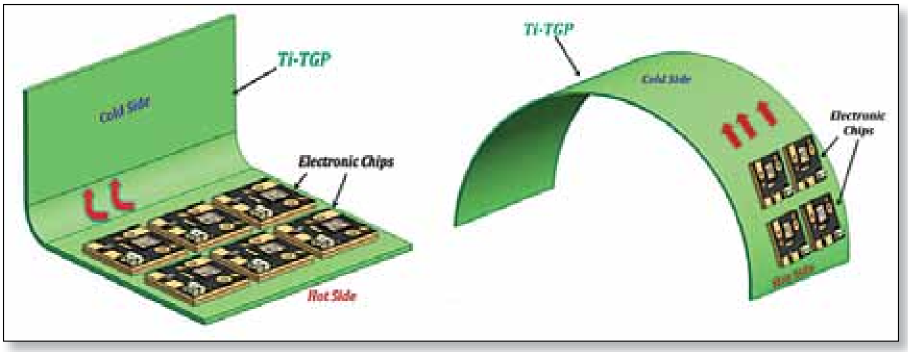

FIGURE 3: Conformal Ti-TGP.

FUTURE DIRECTIONS

A new generation of semiconductor and micro-electronics devices are operating at higher power densities and consequently generating higher heat flux (≥ 100 W/cm^2) capability. These applications are beyond the heat load capacity of current passive flat thermal ground plane solutions.

The future of advanced thermal management is moving toward active solutions to push the heat flux limit beyond passive solutions. Adaptive ultra-thin titanium-based active piezoelectric driven solutions that are able to extend the heat flux limit up to 150 W/cm^2 are currently being developed. Thermal solutions for SiC GaN MMIC are also currently being pursued with the aim of rejecting 1.2 kW/cm^2 heat flux from the GaN MMIC.

In summary, a range of thermal solutions will be available to accommodate a wide range of power and heat flux requirements.

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sales@elma.com; www.elma.com

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North Bend, WA 98045-2660 US
425-888-1880; www.enerdynesolutions.com

Enertron, Inc.
5005 S Ash Ave., Ste 5, Tempe, AZ 85282, US
480-649-5400; Fax: 480-649-5434; enertron-inc.com

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603-533-9011; epac-inc.com; tom@epac-inc.com

ERG Aerospace Corporation
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www.ergaerospace.com
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608-833-1155; Fax: 608-827-6171
www.xes-inc.com

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732-969-0100; Fax: 732-969-3311
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877-249-0874; Fax: 408-436-7705
www.futurefacilities.com; www.6sigmaet.info

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www.selcoproducts.com; sales@selcoproducts.com

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2014 BUYERS' GUIDE
PRODUCTS & SERVICES INDEX

The Products & Services Index contains more than 50 categories to help find the products and services you need. Details of all the suppliers listed within each category can be found in the company directory, starting on page 40. To learn how to be included in this directory, e-mail editor@electronics-cooling.com.

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Delta Electronics
EAO Ltd.
ebm-papst Inc.
JARO Thermal
JMC Products
Nidec America Corporation
Nuventix
OLC Inc.
Rosenberg USA Incorporated
Sanyo Denki America Inc.
SEPA EUROPE GmbH
SUNON Inc.
Waypoint Thermal Management, Inc.

Bonding

Dymax Corporation
Ellsworth Adhesives
Rogers Corporation
Scheugenpflug, Inc.

Chillers

Aavid
AMS Technologies
Aqua Product Company
Capovani Brothers
Lytron
Pfannenberg
Rittal Corporation
Thermonics Corp.,

Circuit Assembly Materials

Indium Corporation
Nexlogic Technologies Inc.
SinkPAD Corporation

Cold Plates

Aavid
Advanced Cooling Technologies Inc.
Advanced Thermal & Environmental Concepts (ATEC)
AMS Technologies
Amulaire Thermal Technology, Inc.
Aspen Systems Inc.
Baknor
Celsia Inc.
Delta Engineers
EPAC
inTEST Thermal Solutions
Lytron
Malico Inc.
MaxQ Technology LLC
Minteq International, Inc.
Niagara Thermal Products
Parker Hannifin - Precision Cooling Systems Division
Sapa Extrusions - North America
Smart Heatsinks
SNS Cooling Technology Inc.
Summit Thermal System Co., Ltd.
TECA ThermoElectric Cooling America Corp.
Thermshield LLC - Division of Niagara Thermal Products
Vette Corp.
Wakefield-Vette
Wolverine Tube Inc. - MicroCool Division

Composites

Jones Tech PLC
Material Innovations Inc. (MII)
Spectra-Mat Inc.

Connectors

Advanced Interconnections Corp.
Indium Corporation
Ironwood Electronics
LCR Electronics
Parker Hannifin Corporation

Connectors, Cable

Amphenol Industrial Operations
Aries Electronics
Staubli Corporation

Coolers

Alpha Novatech Inc.
APACK Inc.
Caliente, LLC
CoolJag
Delta Engineers
Dynatron Corporation
EXAIR Corporation
MovinCool
Nextreme Thermal Solutions
Noctua.at
Parker Hannifin - Precision Cooling Systems Division
TECA ThermoElectric Cooling America Corp.
TE Technology Inc.
Vette Corp.
Vortec, an ITW Company
Zalman Tech Co., Ltd.

Couplings

Staubli Corporation

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Cradle
Future Facilities Inc.
Package Science Services LLC

Arlon Inc.

Brady Corporation
Dow Corning Corporation
Dymax Corporation
Ellsworth Adhesives
Enerdyne Solutions
Fujipoly America Corp.
Graftech International
Henkel
Indium Corporation
Intermark USA Inc
Jones Tech PLC
Kunze Folien GmbH
MH&W International Corp.
Minteq International, Inc.
Plansee SE
ResinLab
Schlegel Electronic Materials
sp3 Diamond Technologies, Inc.
Stockwell Elastomerics Inc.
The Bergquist Company
Timtronics

Laboratories, Test & Research

AERO NAV Laboratories
Anter Corporation
Iceotope Research and Development Limited
Material Innovations Inc. (MII)
Package Science Services LLC

Liquid Cooling

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Baknor
Chilldyne, Inc.
CoolIT Systems Inc.
Curtiss-Wright Controls Electronic Systems
Delta Engineers
Elma Electronic, Inc.
Iceotope Research and Development Limited
Kunze Folien GmbH
Malico Inc.
MaxQ Technology LLC
Mersen
Niagara Thermal Products
Parker Hannifin - Precision Cooling Systems Division
Rittal Corporation
SNS Cooling Technology Inc.
Staubli Corporation
Summit Thermal System Co., Ltd.
Thermonics Corp.,
Vette Corp.
Wolverine Tube Inc. - MicroCool Division

Passive Air Cooling

Baknor
Beijing Deepcool Industries Co. Ltd
Celsia Inc.
Chatsworth Products, Inc.
Elma Electronic, Inc.
Delta Engineers
Indium Corporation
Radian Thermal Products, Inc.
Singapore Institute of Manufacturing Technology
STEGO, Inc.
SUNON Inc.
Thermonics Corp.,

Phase Change Materials

AIM Specialty Materials
Alfatec GmbH & Co.
Brady Corporation
Caliente, LLC
Henkel
Indium Corporation
Kunze Folien GmbH
Laird Technologies
MH&W International Corp.
Polymer Science Inc.
The Bergquist Company
TTM Co., Ltd.

Sensors, Test & Measurements

Caliente, LLC
DegreeC, Degree Controls Inc.
FLIR Commercial Systems, Inc.
Microsanj LLC
Nextreme Thermal Solutions
OptoTherm Inc.
Palmer Wahl Temperature Instruments
Selco Products Company
Sensor Products Inc.
Spectrum Sensors
Spirig Advanced Technologies Inc., (SAT)
Temperature@lert
Wavelength Electronics Inc.

Services

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CapeSym, Inc.
Cradle
Daat Research Corp.
Flometrics, Inc.
Mechanical Solutions Inc.
Microsanj LLC
Nexlogic Technologies Inc.
Scheugenpflug, Inc.
sp3 Diamond Technologies Inc.
TDMG Inc
Temperature@lert
Ten Tech LLC
TES International LLC

Software (EMC)

Hyphen

Software (Simulation)

A.J. Wishart
CapeSym Inc.
Cradle
Daat Research Corp.
EPAC
Future Facilities Inc.
Harley Thermal LLC
INTEGRATED Engineering Software
Mechanical Solutions Inc.
Mentor Graphics Corporation - Mechanical Analysis Division
Ten Tech LLC
TES International LLC
Thermal Solutions Inc.

Software (Thermal)

Harley Thermal LLC

Substrates

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SinkPAD Corporation
Spectra-Mat Inc.
The Bergquist Company

Temperature Controllers

Caliente LLC
Concept Group Inc.
CoolIT Systems Inc.
DegreeC, Degree Controls Inc.
EIC Solutions, Inc.
EXAIR Corporation
Selco Products Company
STEGO, Inc.
Temperature@lert
Verotec Inc.
Wavelength Electronics Inc.

Test Equipment

Anter Corporation
Capovani Brothers Inc.
Degree Controls, Inc.
inTEST Thermal Solutions
Ironwood Electronics
Microsanj LLC
Palmer Wahl Temperature Instruments
Sensor Products Inc.
Teseq
Thermal Engineering Associates Inc.

Thermal Compounds

AOS Thermal Compounds
Arlon Inc.
Dow Corning Corporation
Ellsworth Adhesives
Indium Corporation
Jones Tech PLC
Kaneka Americas
NAMICS Technologies, Inc.
ResinLab
Surmet Corporation
Timtronics
TTM Co., Ltd.
Zalman Tech Co., Ltd.

Thermal Design Services

Aavid
Advanced Thermal & Environmental Concepts (ATEC)
Alpha Novatech Inc.
AMS Technologies
Baknor
CapeSym Inc.
Celsia Inc.
Chatsworth Products, Inc.
Cofan USA
Concept Group Inc.
CoolIT Systems Inc.
Daat Research Corp
Degree Controls, Inc.
Enerdyne Solutions
Future Facilities Inc.
Harley Thermal LLC
Heatron, Inc.
Ironwood Electronics
Mechanical Solutions Inc.
Mentor Graphics Corporation - Mechanical Analysis Division
Mersen
Mintres BV
Package Science Services LLC
Radian Thermal Products Inc
SinkPAD LLC
Smart Heatsinks
TDMG Inc.
Ten Tech LLC
TES International LLC
Thermal Engineering Associates Inc.
Thermal Solution Resources, LLC

Continued from the articles on page 34.

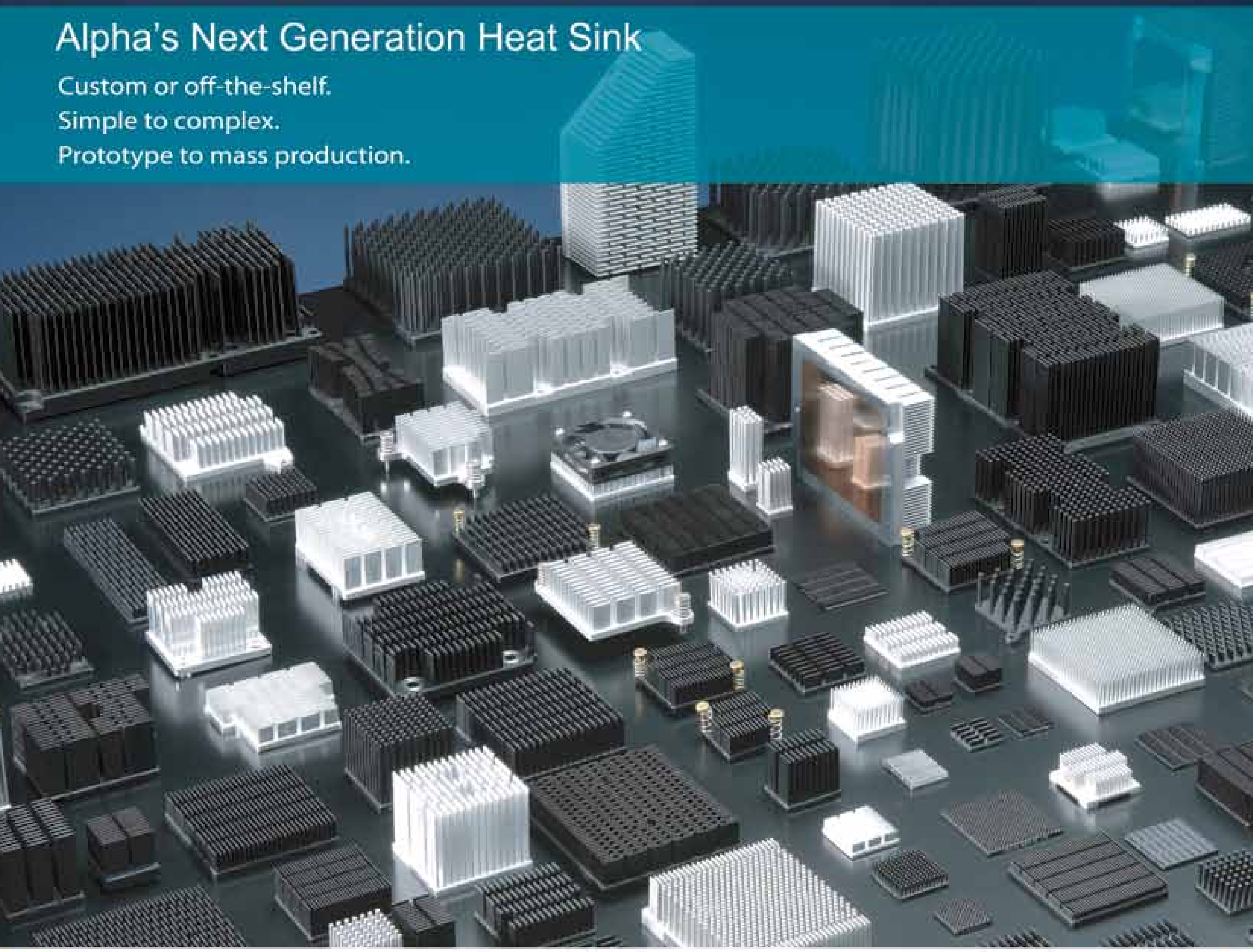
NOMENCLATURE

A	area	[mm^2]
b	depth	[mm]
d	diameter	[mm]
h	height	[mm]
l	length	[mm]
Q	volume flow rate	[m^3/s]
w	width	[mm]
x	distance	[mm]
β	opening area ratio	
ΔP	pressure difference	[Pa]
π	circular constant	

SUBSCRIPTS

ch	chamber vs. surrounding
cl	clearance around obstruction
en	enclosure
hub	fan hub
in	enclosure inlet
ob	obstruction
s	strut
tip	fan trip

Index of Advertisers



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Feature and design change for thermal & mechanical improvement.

Counterbore features added to fin side of the heat sink
Allows for push pin and spring attachment in height constrained applications.

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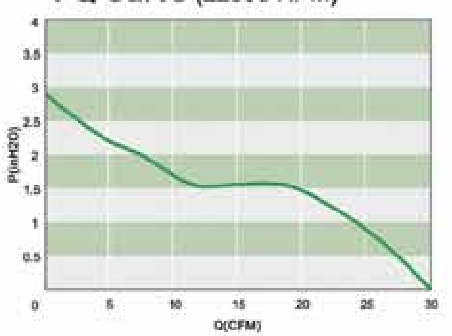
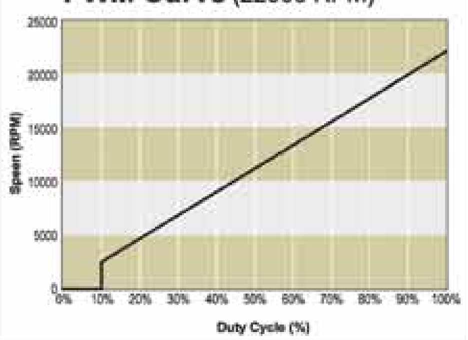
SUNON®

PF 40x40x28mm

PQ Curve (22000 RPM)



PWM Curve (22000 RPM)



High Air Flow

PF series

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- 33% Low Vibration Reduced
- PWM Control Function
  40% Energy saving (100% duty)
  50% Energy saving (under 50% duty)

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