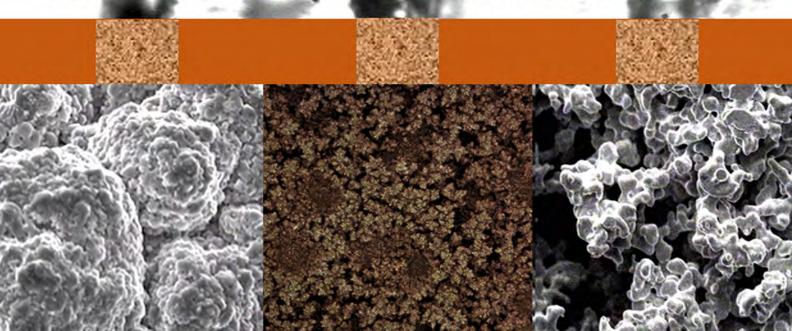


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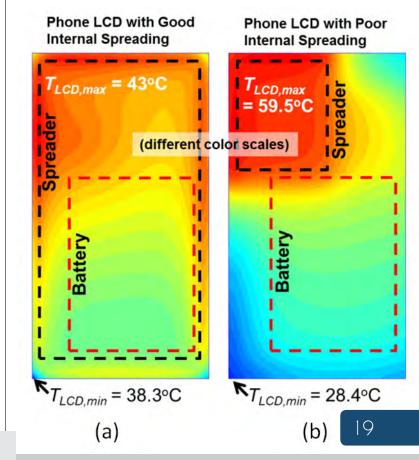
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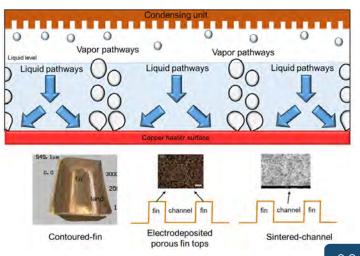


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Editorial

Reflections on 2015 and Beyond

Peter Rodgers, Editor-in-Chief, December 2015



he planned March 2016 Edition of Electronics Cooling will be dedicated to both reviewing the achievements of this magazine since its release in 1995 and considering the thermal management challenges that will be faced over the coming decade. However, as 2015 draws to a close it is now evident that electronics thermal management, as a discipline, has evolved over the past twenty years to now form an integral role of the product design process in most organizations. As older practitioners will note, this has not always been the case, with thermal management often

initiated in many organizations as a "band aid" after the characterization of an initial product prototype. Such practices and their limitations were highlighted in early editions of Electronic Cooling [1, 2]. Similarly over the past two decades, Electronics Cooling has facilitated discussions on the link between operational temperature and reliability. For example, the limitations of broad sweeping design for reliability guidelines, i.e. "for every 10°C increase in temperature the useful life decreases by a factor of two" have been outlined. This led to advocating more comprehensive product performance assessment methodologies [3]. Given the reflective tone of this editorial, it would be amiss not to highlight to younger practitioners that thermal design based computational fluid dynamics analysis has not always been one computer mouse click away! Over the last two decades the application of numerical thermofluid modeling has evolved from resolving initial computer aided design file incompatibility issues, limitations in pre-processing tools, and severe computational power limitations, to becoming an effective and indispensable part of the product development process. However, as previously noted [2], that does not mean all aspects of thermal analysis should be numerical based. The Calculation Corner article included in this edition of *Electronics Cooling* illustrates the importance of first order calculations, in this instance for estimating parallel plate-fin heat sink thermal resistance. Originally published in 2003, this calculation column is still of value to younger practitioners.

As we conclude 2015, considering the field of energy on a broad level, which electronics thermal management is part of, this year was a significant assessment milestone. The reason being that numerous energy demand and production roadmaps drawn up for Year 2030 were initiated in the early 2000's, with 2015 being a pivotal midpoint. The electronics thermal management community can contribute a key role in helping to achieve 2030 targets by enhancing the sustainability of electronics systems throughout their life cycle; from materials selection, manufacturing/assembly, operation, to product disposal.

Finally, on behalf of the Editorial Team, I wish you a prosperous and cool 2016!

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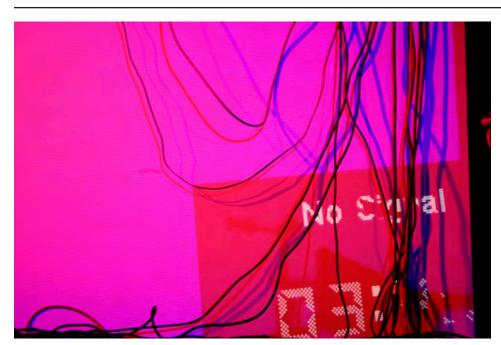


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Electronics Cooling Communication for dumMEs and dumEEs

Jim Wilson Raytheon



LECTRONICS COOLING DESIGN AND ANALYSIS

problems inherently bring together engineers from different backgrounds, especially mechanical and electrical engineers. Engineers with a heat transfer or fluid mechanics background usually studied these subjects in the mechanical engineering department. Understanding of semiconductors and related circuits usually involves engineers that have electrical backgrounds. My personal background is mechanical but I have worked with digital and analog electrical engineers for many years and the fairy tale for this column is that we all immediately understand each other. The related fact is that there is much to be learned by realizing that while there is much in common, communication is easier when we recognize that our backgrounds influence our terminology and perspective. A risk in writing a column about this topic is that it most certainly will not be comprehensive, but will only reflect some of the perspectives I have noticed that potentially create communication barriers.

Some terminology is immediately relatable between disciplines. Starting with the electrical-thermal analogy, the electronics cooling community has a long history solving conduction heat transfer problems by relating voltage and temperature, current and heat flow, thermal and electrical resistance, and capacitance for transient effects. Prior to the ease of performing computational simulations, circuit analysis was found to be an effective method of temperature prediction [1,2]. However, even a relatively simple concept like resistance can have a different perspective between thermal and electrical disciplines. From the electrical point of view, the scale range of electrical resistivity is very large. Not counting superconductors, electrical resistivity in ohm-m ranges from about 10-8 for

metals to 10^{16} for insulators. This means that an electrical insulator as part of an electrical circuit can truly be treated as not having any current flow. From a thermal point of view, resistance to heat conduction is a function of material thermal conductivity and the comparable scale range of thermal conductivity is much smaller, from about 10^{-3} to about 10^3 in W/m-K. This smaller scale range means that thermal engineers do not have true insulating materials and typically must consider more of the physical domain for simulations. For example, an electrical voltage analysis of a circuit card would typically only consider the conducting traces and ignore the dielectric, while a comparable thermal simulation would most likely need to include both the metal and dielectric layers.

Electrical engineers that deal with power levels or signal strength, like Radio Frequency (RF) engineers, deal with the large scale range by using a log scale, most often using decibels. Expressing gain of a system in this manner is convenient, es-

pecially for systems that have a very large range of power levels. For example, an antenna system may transmit 1000s of Watts but only receive a few mW. Power levels are often expressed in units of dBm, or dBW, where the m refers to 1 milliwatt and the W refers to 1 W (for example 0 dBm is 1 milliwatt of power). Thermal engineers who interact with RF engineers should learn to communicate in dBs but the RF engineers should learn that thermal engineers have a preference for Watts. Sometimes power levels are measured to tolerances of dB and this can be challenging for thermal engineers. If a signal is measured to a tolerance of +/- 0.5 dB the percentage tolerance is about +/- 12%. Depending on the magnitude of the signal, this can cause grief to the thermal engineer trying to perform an energy balance. The RF engineer might be happy the measurement is within 0.5 dB of expectations but the thermal engineer would like a smaller uncertainty.

Aside from the thermal engineer who remembers solving 2D potential flow problems in graduate school, electrical engineers are usually more comfortable with using complex numbers. The use of the term impedance has transient implications, as in the impedance of an alternating current circuit expressed as the

complex ratio of voltage to current. Some thermal engineers correctly use the term impedance in a thermal sense when describing the transient behavior of devices, especially power devices. However, sometimes thermal contact resistance is described using the term thermal impedance and this is incorrect. Thermal engineers would be better served to use terms like contact conductance or contact resistance for describing thermal interfaces to avoid confusion.

In keeping with the thermal facts and fairy tales theme, regardless of our backgrounds, communication with our coworkers is always easier when we take the time to understand the perspectives of others.

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Estimating Parallel Plate-fin Heat Sink Thermal Resistance

Robert E. Simons IBM Corporation

Editor's note: In recognition of the 20th year of ElectronicsCooling, we are republishing articles from past issues that we believe to be of particular value to our readership. The following article was published in the February 2003 issue as a Calculation Corner authored by Bob Simons. Bob served as an Associate Technical Editor of this publication from January, 2001, to December, 2011.

For those readers who find this sort of tutorial useful, please refer to the list, compiled by Bob, of many other Calculation Corner columns authored by him as well as by others: http://www.electronics-cooling.com/2011/09/a-useful-catalog-of-calculation-corner-articles/.

S NOTED PREVIOUSLY IN THIS COLUMN, the trend of increasing electronic module power is making it more and more difficult to cool electronic packages with air. As a result there are an increasing number of applications that require the use of forced convection air-cooled heat sinks to control module temperature. An example of a widely used type of heat sink is the parallel plate configuration shown in Figure 1.

In order to select the appropriate heat sink, the thermal designer must first determine the maximum allowable heat sink thermal resistance. To do this it is necessary to know the maximum allowable module case temperature, $T_{\rm case}$, the module power dissipation, $P_{\rm mod}$, and the thermal resistance at the module-to-heat sink interface, $R_{\rm int}$. The maximum allowable temperature at the heat sink attachment surface, $T_{\rm base}$, is given by:

$$T_{\text{base}} = T_{\text{case}} - P_{\text{mod}} \cdot R_{\text{int}} \tag{1}$$

The maximum allowable heat sink resistance, $\boldsymbol{R}_{\text{max}}$, is then given by:

$$R_{\text{max}} = \frac{T_{\text{base}} - T_{\text{air-in}}}{P_{\text{mod}}} \tag{2}$$

where $T_{\rm air\cdot in}$ is the temperature of the cooling air at the inlet to the heat sink passages. At this point many thermal engineers will start looking at heat sink vendor catalogs (or more likely today start searching vendors on the internet) to find a heat sink that will fit in the allowable space and provide a heat sink thermal resistance, $R_{\rm hs}$, less than $R_{\rm max}$ at some specified flow

rate. In some cases, it may be useful to do a sizing to estimate $R_{\rm hs}$ for various plate-fin heat sink designs to determine if a feasible design configuration is possible. The remainder of this article will provide the basic equations to do this.

The thermal resistance of the heat sink is given by:

$$R_{hs} = \frac{1}{h \cdot \left(A_{base} + N_{fin} \eta_{fin} A_{fin}\right)}$$
(3)

where h is the convective heat transfer coefficient, A_{base} is the exposed base surface area between fins, N_{fin} is the number of fins, η_{fin} is the fin efficiency, and A_{fin} is the surface area per fin taking into account both sides of the fin.

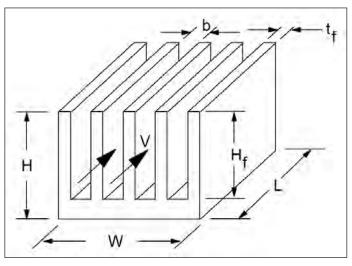


Figure 1: Parallel plate fin heat sink configuration.



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To proceed further it is necessary to establish the maximum allowable heat sink volume in terms of width, W, height, H, and length in the flow direction, L. It is also necessary to specify a fin thickness, \mathbf{t}_{fin} . Using these parameters the gap, b, between the fins may be determined from:

$$b = \frac{W - N_{fin} \cdot t_{fin}}{N_{fin} - 1} \tag{4}$$

The exposed base surface area may then be determined from:

$$A_{\text{base}} = (N_{\text{fin}} - 1) \cdot b \cdot L \tag{5}$$

and the heat transfer area per fin from:

$$A_{fin} = 2 \cdot H_f \cdot L \tag{6}$$

At this point it is necessary to specify the air flow rate either in terms of the average velocity, V, between the fins or a volumetric flow rate, G. If a volumetric flow rate is used, the corresponding air velocity between the fins is:

$$V = \frac{G}{N_{fin} \cdot b \cdot H_f} \tag{7}$$

To determine the heat transfer coefficient acting upon the fins, an equation developed by Teertstra *et al.* [1] relating Nusselt number, Nu, to Reynolds number, Re, and Pr number, Pr, may be employed. This equation is:

$$Nu_{b} = \left[\frac{1}{\left[\frac{\text{Re} \cdot \text{Pr}}{2}\right]^{3}} + \frac{1}{\left[0.664\sqrt{\text{Re}} \ \text{Pr}^{0.33}\sqrt{1 + \frac{3.65}{\sqrt{\text{Re}}}}\right]^{3}}\right]^{-0.33}$$
(8)

The Prandtl number is:

$$Pr = \frac{\mu \cdot C_p}{k} \tag{9}$$

where μ is the dynamic viscosity of air, c_p the specific heat of air at constant pressure, and k is the thermal conductivity of air. The

Reynolds number used in (8) is a modified channel Reynolds number defined as:

$$Re = \frac{\rho \cdot V \cdot b}{\mu} \cdot \frac{b}{L} \tag{10}$$

where ρ is the density of air. Equation (8) is based upon a composite model spanning the developing to fully developed laminar flow regimes and was validated by the authors [1] by comparing with numerical simulations over a broad range of the modified channel Reynolds number (0.26 < Re < 175) and with some experimental data as well. Using the Nusselt number obtained in (8) the heat transfer coefficient is given by:

$$h = Nu_b \cdot \frac{k_{fin}}{b} \tag{11}$$

where k_{fluid} is the thermal conductivity of the cooling fluid (i.e. air). The efficiency of the fins may be calculated using:

$$\eta_{fin} = \frac{\tanh(m \cdot H_f)}{m \cdot H_f}$$
(12)

where m is given by:

$$m = \sqrt{\frac{2 \cdot h}{k_{fin} \cdot t_{fin}}}$$
 (13)

and $k_{\mbox{\tiny fin}}$ is the thermal conductivity of the fins.

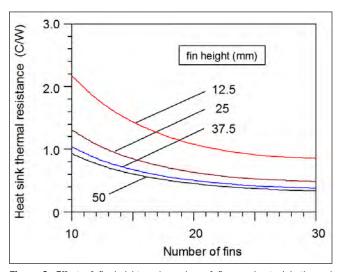


Figure 2: Effect of fin height and number of fins on heat sink thermal resistance at an air velocity of 2.5 m/s (492 fpm).

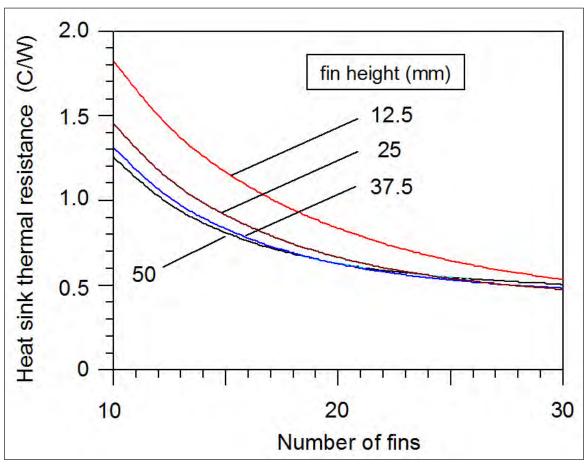


Figure 3: Effect of fin height and number of fins on heat sink thermal resistance at a volumetric air flow rate of 0.0024 m³/s (5 CFM).

Using these equations it is possible to estimate heat sink thermal performance in terms of the thermal resistance from the temperature at the base of the fins to the temperature of the air entering the fin passages. It may be noted that the relationship for Nusselt number (8) includes the effect of the temperature rise in the air as it flows through the fin passages. To obtain the total thermal resistance, $R_{\rm tot}$, to the base of the heat sink it is necessary to add in the thermal conduction resistance across the base of the heat sink. For uniform heat flow into the base $R_{\rm tor}$, is given by:

$$R_{\text{tot}} = R_{\text{hs}} + \frac{\text{H-H}_{\text{f}}}{k_{\text{base}} \cdot W \cdot L}$$
 (14)

and k_{base} is the thermal conductivity of the heat sink base.

For purposes of illustration these equations were used to estimate heat sink thermal resistance for a 50 x 50 mm alumi-

num heat sink. The effect of increasing the fin height and the number of fins is shown in Figure 2 for a constant air velocity and in Figure 3 for a constant volumetric flow rate. In both cases it may be seen that there are limits to how much heat sink thermal resistance may be reduced by either increasing fin length or adding more fins. Of course to determine how a heat sink will actually perform in a specific application it is necessary to determine the air velocity or volumetric flow rate that can be delivered through the heat sink. To do this it is necessary to estimate the heat sink pressure drop characteristics and match them to the fan or blower to be used. This is a topic for consideration in a future article.

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Low Electrical Conductivity Liquid Coolants for Electronics Cooling

Bojanna Shantheyanda, Sreya Dutta, Kevin Coscia and David Schiemer Dynalene, Inc.

1.0 Introduction

IQUID COOLING, WHICH CAN BE achieved using indirect or direct means, is utilized in electronics applications having thermal power densities that may exceed safe dissipation through air cooling. Indirect liquid cooling is where heat dissipating electronic components are physically separated from the liquid coolant, whereas in case of direct cooling, the components are in direct contact with the coolant [1]. Most desired liquid coolants' for electronics cooling applications have good themophysical properties, high flash point and auto ignition

Bojanna Shantheyanda graduated with a MS in Technology Entrepreneurship from University of Maryland in 2015. He received his MS in Electrical Engineering from University of Central Florida in 2010. Working as a research engineer at Dynalene he is involved in developing filtration, desiccation, ion exchange and carbon based products. Previously, he worked as a research and process development engineer of specialty and commodity activated carbon materials for Y-Carbon, Inc.



Dr. Sreya Dutta received her Ph.D in Materials Science and Engineering from Lehigh University in 2009. She has several years of experience in advanced electron microscopy, sol-gel synthesis, coatings, corrosion and compatibility study of heat transfer fluids with various materials. She works as a Materials Scientist at Dynalene. She was actively involved in the Phase III DOE SBIR project on "Large Scale Testing, Demonstration and Commercialization of Fuel Cell Coolants". She also helps Dynalene with Quality Control and Lab Services testing.



Kevin Coscia worked in research and development for Dynalene since June, 2010. He graduated with a B.S. in Chemical Engineering from Lehigh University in May, 2010. Kevin's initial work with Dynalene was researching and developing molten salts for high-temperature applications, synthesizing functionalized nanoparticles for ion-exchange resins as well as developing new corrosion inhibitor packages for heat transfer fluids. He was extensively involved in projects with the Department of Energy and Department of Defense to develop high-performance nanocoolants for electronics cooling.



David Schiemer attended Lehigh University and received a degree in Mechanical Engineering in 2013. During his senior year, David worked at Dynalene as a R&D intern studying nanoparticle coolants and their effects on PEMs (Polymer Exchange Membranes). Currently, David works for Phoenix Electric Corporation in Boston, MA and specializes in designing, assembling, and installing switchgear for utility and industrial power applications.



temperature, compatible with materials of construction, good chemical and thermal stability, inexpensive, nontoxic and long shelf life. Good thermophysical properties for the liquid coolants are required in order to obtain both higher convective heat transfer coefficients and lower pumping power [2]. Deionized water is a good example of a widely used electronic coolant for indirect cooling applications. Other popular non-dielectric coolant chemistries used in indirect cooling applications are propylene glycol, ethylene glycol, ethanol/water, calcium chloride solution, potassium formate/acetate solution and liquid metals such as alloy of gallium, indium and tin (Ga-In-Sn) [2].

The electrical conductivity of the liquid coolant becomes important in a direct cooling application because of the contact between the coolant and the electronics [3]. However, in indirect cooling applications the electrical conductivity can be important if there are leaks and/or spillage of the fluids onto the electronics. In the indirect cooling applications where water based fluids with corrosion inhibitors are generally used, the electrical conductivity of the liquid coolant mainly depends on the ion concentration in the fluid stream. Higher the ionic concentration, larger is the electrical conductivity of the fluid. The increase in the ion concentration in a closed loop fluid stream may occur due to ion leaching from metals and nonmetal components that the coolant fluid is in contact with. During operation,



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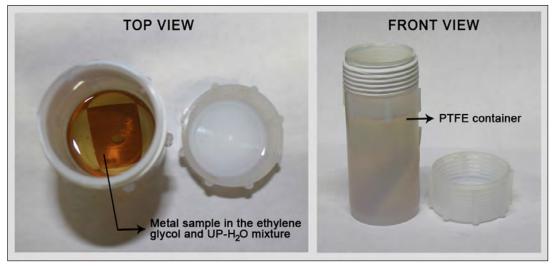


Figure 1: Long-term ion leaching experimental setup.

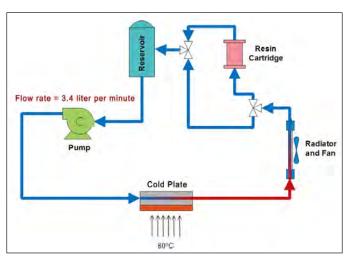


Figure 2: Schematic of the indirect closed loop cooling experiment set-up.

the electrical conductivity of the fluid may increase to a level which could be harmful for the cooling system.

Ion exchange resin can be used to remove the ionic substances that raise the electrical conductivity of the coolant in an electronics cooling application. They are bead like polymers that are capable of exchanging ions with ions in a solution that it is in contact with.

In the present work, ion leaching tests were performed with various metals and polymers in both ultrapure deionized (DI) water, i.e. water which is treated to the highest levels of purity, and low electrical conductive ethylene glycol/water mixture, with the measured change in conductivity reported over time. Additionally, changes in the electrical conductivity of ultrapure DI water in an indirect, single phase, active cooling loop, with and without ion exchange resin are characterized with the findings reported. Finally, recommendation for design and estimation of the longevity of the ion exchange resin cartridge in an electronics cooling loop is discussed.

2.0 EXPERIMENTATION

In this section the experimental setup for measuring coolant electrical conductivity in both the ion leaching and closed loop indirect cooling experiments are described.

2.1 LONG-TERM ION LEACHING EXPERIMENT

The experimental setup used for the long-term ion leaching analysis is shown in Figure 1. The experiment was performed using aluminum (AL3003),

brass (B5665), stainless steel (304L), high-density polyethylene (HDPE), polypropylene, nylon, polyvinyl chloride (PVC), nitrile rubber (Buna-N), polyurethane and silicone samples separately immersed in:

- 1) Ultra-pure distilled water (UP- H_2O) with the electrical conductivity 0.5 μ S/cm, and
- 2) Premade mixture of 50:50 ethylene glycol and UP- H_2O , and nonionic inhibitors (EG-LC).

All fluid and test samples were placed in polytetrafluoroethylene (PTFE) containers which were cleaned with distilled water, alcohol, UP-H₂O and dried in ambient atmosphere. PTFE containers were chosen over borosilicate glass because they contain strong, compact bonds which are excellent at maintaining their original crystallinity, therefore, exhibiting lesser ion leaching capacity to the base fluid. The containers were charged with either UP-H₂O or EG-LC. Metal and polymer coupons were rinsed with distilled water, alcohol, UP-H2O and polished to remove excess surface debris. The materials were placed in the containers and sealed with PTFE thread tape and PTFE lids. The samples were allowed to equilibrate at room temperature for two days before recording the initial electrical conductivity. In all tests reported in this study fluid electrical conductivity was measured to an accuracy of ±1% using an Oakton CON 510/CON 6 series meter which was calibrated prior to each measurement. A furnace was preheated to 80°C in ambient atmosphere and verified for heating uniformity to ±1°C at different locations, i.e. from the wall heating coils to the center of the furnace. The PTFE sample containers were placed in the furnace when steady state temperatures were reached. The test setup was removed from the furnace every 168 hours (seven days), cooled to room temperature with the electrical conductivity of the fluid measured. The time taken for the samples to cool, measure electrical conductivity, and place back in the oven was generally less than four hours. The electrical conductivity of the fluid sample was monitored for a total of 5000 hours (~208 days).

Components	Construction Material		
Reservoir	Acrylic and chrome plated aluminum		
Tubing	Silicone		
Cooling block	Copper		
Tube connectors	Nylon and PVC		
Radiator	Aluminum		
Swiftech MCP655-B Pump	Polypropylene		
Sealant tape	PTFE		
Ion exchange resin cartridge	Acrylic		

Table 1: Components used in the indirect closed loop cooling experiment that are in contact with liquid coolant.

2.2 CLOSED LOOP, INDIRECT COOLING EXPERIMENTAL SET-UP

A schematic of the experimental setup is shown in Figure 2. Table 1 lists the components used for which the liquid coolant made direct contact with. Before commencing each experiment, the test setup was rinsed with UP-H $_2$ O several times to remove any contaminants. The system was loaded with 230 ml of UP-H $_2$ O and was allowed to equilibrate at room temperature for an hour before recording the initial electrical conductivity, which was 1.72 μ S/cm. Fluid electrical conductivity was measured to an accuracy of $\pm 1\%$. After the initial measurements, the copper cooling block was placed on a hot plate operated at 80°C. During operation the fluid reservoir temperature was maintained at 34°C. The change in fluid electrical conductivity was monitored for 136 hours. The fluid from the system was collected and stored.

Similarly, closed loop test with ion exchange resin was carried out with the same cleaning procedures employed. The initial electrical conductivity of the 230ml UP-H $_2$ O in the system measured 1.84 μ S/cm. An ion exchange resin cartridge (diameter = 38.1mm, height = 50.8 mm) containing 20g of Dowex mixed bed resin was installed in the fluid loop. Table 2 shows the test matrix that was used for both ion leaching and closed loop indirect cooling experiments.

Parameter	Long-term ion leaching	Closed loop indirect cooling UP-H2O • Acrylic • Chrome plated aluminum • Silicone • Copper • Nylon • PVC • Aluminum • Polypropylene • PTFE	
Test fluid	(1)UP-H2O* (2)EG-LC**		
Test samples	3003 Aluminum B5665 brass 304 stainless steel High-density polyethylene (HDPE) Polypropylene Nylon Polyvinyl chloride (PVC), Nitrile rubber (Buna-N), Polyurethane Silicone		
Temperature	80°C	Hot plate = 80°C, fluid reservoir =34°C	
Flow rate	Stationary	3.4 liter per minute	
Duration of the experiment	5000 hours	136 hours	
Ion exchange resin	None	Both with and without ion exchange resin	

**Premade mixture of 50:50 ethylene glycol and UP-H2O, and and nonionic inhibitors (EG-LC)

Table 2: Test matrix for both ion leaching and indirect closed loop cooling experiments.

The change in electrical conductivity of the fluid samples when stirred with Dowex mixed bed ion exchange resin was measured. Two fluid samples were used for testing:

- 1) Water from the closed loop, indirect cooling experiment that did not use resin cartridge and
- 2) NaCl solution with the electrical conductivity of 11.82 $\mu\text{S}/$ cm.

0.1g of Dowex resin was added to 100g of fluid samples that was taken in a separate container. The mixture was stirred and change in the electrical conductivity at room temperature was measured every hour.

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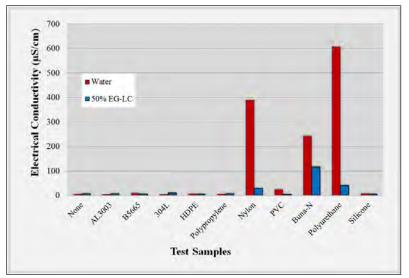


Figure 3: Ion leaching experiment: Measured change in electrical conductivity of water and EG-LC coolants containing either polymer or metal samples when immersed for 5,000 hours at 80°C

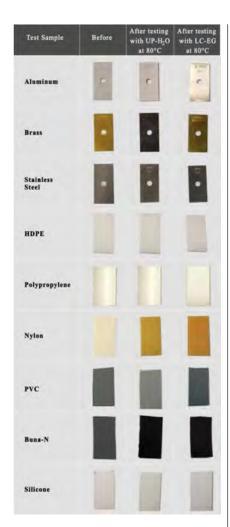


Figure 4: Before and after images of metal and polymer samples immersed for 5,000 hours at 80°C in the ion leaching experiment.

2.0 RESULTS AND DISCUSSION 2.1 LONG-TERM ION LEACHING EXPERIMENT

The measured change in the electrical conductivity of the UP-H₂O and EG-LC test fluids containing polymer or metal when immersed for 5,000 hours at 80°C is shown Figure 3. To place in context the measurement results. the electrical conductivity of drinking water is typically less than 500μS/cm, river water between 50 to 1500uS/ cm, industrial water less than 10,000µS/cm with seawater typically less than 50,000µS/ cm [4].

The results indicate that metals contributed fewer ions into the fluids than plastics in both UP-H₂O and EG-LC based coolants. This could be due to a thin metal oxide layer

which may act as a barrier to ion leaching and cationic diffusion. Both UP-H₂O and EG-LC fluid containing polypropylene and HDPE test samples exhibited the lowest electrical conductivity changes. Fluids containing polypropylene and HDPE exhibited the lowest electrical conductivity changes. This could be due to the short, rigid, linear chains which are less likely to contribute ions than longer branched chains with weaker intermolecular forces. Silicone also performed well in both test fluids, as polysiloxanes are generally chemically inert due to the high bond energy of the silicon-oxygen bond which would prevent degradation of the material into the fluid. It was observed that materials containing nitrogen groups, such as Buna-N rubber, polyurethane, and nylon had the largest electrical conductivity increases. It would be expected that PVC would produce similar results to those of PTFE and HDPE based on the similar chemical structures of the materials, however there may be other impurities present in the PVC, such as plasticizers, that may affect the electrical conductivity of the fluid. Additionally, chloride groups in PVC can also leach into the test fluid

and can cause an increase in electrical conductivity.

Figure 4 shows the before and after sample images of 5,000 hour testing of the metals and polymer samples, which was used in the ion leaching experiment. Buna-N rubber and polyurethane showed signs of degradation and thermal decomposition which suggests that their possible utility as a gasket or adhesive material at higher temperatures could lead to application issues. Polyurethane completely disintegrated into the test fluid by the end of 5000 hour test.

2.2 CLOSED LOOP, INDIRECT COOLING EXPERIMENT

The measured change in electrical conductivity of the UP- H_2O for 136 hours with and without ion exchange resin in the loop is shown in Figure 5. The electrical conductivity of the UP- H_2O without resin cartridge increased by a factor of seven from $1.72\mu S/cm$ to $11.77\mu S/cm$ by the end of 136 hours of testing, an increase of approximately $1.77\mu S/cm$ per day. This indicates, during the course of the experiment, a constant ion leaching from the components when the fluid is in contact. The electrical conductivity of the UP- H_2O in the loop containing the ion exchange resin cartridge consistently remained below $0.5\mu S/cm$, indicating that the ion exchange resin was able to remove the ions that leached to the fluid stream, maintaining low electrical conductivity of the fluid during the duration of the experiment.

Figure 6 shows the change in the measured electrical conductivity of the fluid samples when stirred with the resin sample. The conductivity of the water sample from the closed loop experiment reduced by approximately 70% from 11.77µS/cm to 3.32µS/cm in six hours. Whereas, the electrical conductivity of the NaCl solution reduced by approximately 85% from 11.82µS/cm to 1.8µS/cm in six hours.

These results indicated that the capacity of the resin de-

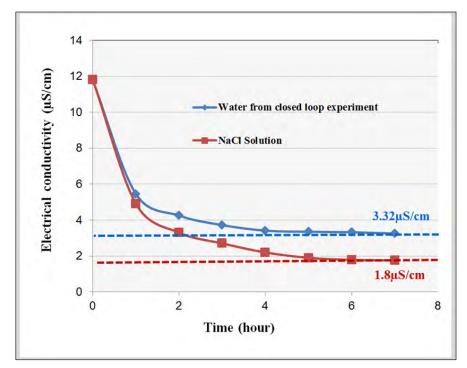


Figure 6: Measured change in electrical conductivity of fluid samples as a function of time when stirred with the resin sample in the closed indirect cooling loop experiment.

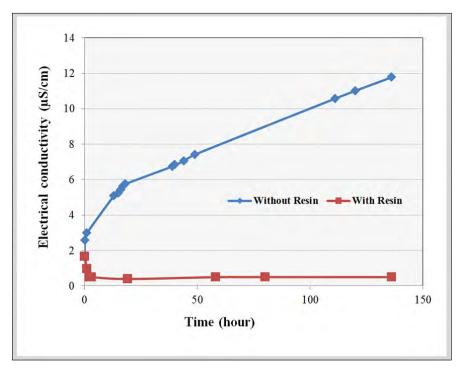


Figure 5: Measured change in the electrical conductivity of UP-H₂O coolant as a function of time with and without resin cartridge in the closed indirect cooling loop experiment.

pends on the test fluid used for the experiment. This shows that different ions present in the fluid will result in different ion exchange capacity of the fluid. Therefore, calculating the ion exchange resin capacity with the fluid sample from the actual cooling loop is important. In order to calculate the accurate longevity of the resin

cartridge that was used in the cooling loop experiment, the resin capacity with the water sample from the closed loop experiment was taken into consideration. Therefore, an ion exchange resin cartridge containing 20g of Dowex mixed bed resin may take on order 938 days to saturate. In other words, to maintain a low electrical conductivity, a resin cartridge with the dimension and weight specification as that of the resin cartridge used in the experiment, need to be changed every 30 months for the cooling system that was used in the experiment.

CONCLUSIONS

The long term ion leaching experiment showed that an increase in the electrical conductivity of the coolant fluid is contributed by ion leaching of both metals and polymers that were used in the closed loop cooling system. By determining both the rate of increase in the electrical conductivity and the ion exchange capacity of the resin with the ions in the fluid used in the cooling system, the estimation of the longevity of the resin cartridge in an electronics liquid cooling loop can be calculated.

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A Figure of Merit for Smart Phone Thermal Management

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INTRODUCTION

ITH SMART PHONES AND OTHER mobile devices available in a variety of sizes and shapes, it is challenging to think in a consistent and comparative manner about the effectiveness of the thermal management solutions that they employ. This is growing more important as the mobile and wireless industries and associated research communities explore novel mobile cooling approaches. Here we define a universal thermal figure of merit - a dimensionless Coefficient of Thermal Spreading (CTS) - that can be calculated using either numerical simulations or Infrared (IR) surface temperature imaging and can be used to compare the thermal design effectiveness of many mobile devices and power levels. The proposed CTS Figure of Merit quantifies the effectiveness of heat spreading within the device by means of the uniformity of the surface temperature, and addresses a long-time need to quantify the thermal design effectiveness of various mobile devices which are skin temperature limited.

There has been past work on thermal performance metrics of electronics, particularly those for which central processing unit (CPU) overheating limits power generation. Some metrics are defined at the package level for single or multi-chip designs, and are useful for junction temperature prediction and

as performance figures of merit [1, 2]. Other authors discuss the importance of the skin cooling and other thermal challenges in handheld mobile devices [3, 4]. However, when it comes to the system level thermal performance, the industry lacks a metric to quantify the "goodness" of the thermal design. A key benefit of such a metric would be to track the impact of design changes on the thermal performance considering the device skin limits.

One major thermal challenge of portable electronic devices is the strong spatial and temporal variability of the thermal boundary conditions at the case. A phone with outstanding *internal* thermal management will likely aim for a reasonably consistent temperature on its *exterior* surfaces. In fact, in the limit of perfect internal thermal management, all of the heat generated by the chips and other components inside the phone will be spread to the various phone surfaces and provide a nearly uniform temperature distribution when viewed from the outside. Figure 1 shows that selecting a good thermal management strategy inside the phone improves the temperature uniformity and lowers the peak surface temperature.

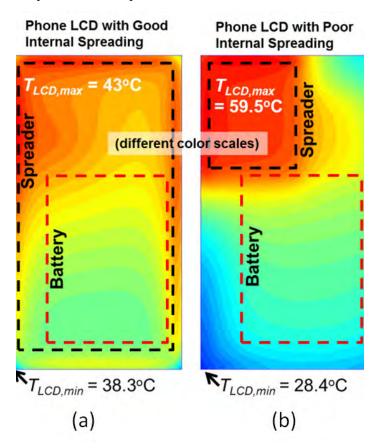


Figure 1: Simulated temperature distributions on the surface of a generic phone LCD (138 mm x 70 mm) for two different thermal management schemes. (a) Large heat spreader (128 mm x 62 mm), which couples the battery with the heat generating chips and yields a more uniform temperature. (b) Smaller heat spreader (35 mm x 33 mm) yielding highly non-uniform LCD temperature.

Figure 1 illustrates that phone thermal design must meet certain skin limit temperatures and avoid the potential hot spots. The poor heat spreading on the device surface leads to a peak temperature of 59.5°C (Figure 1(b)), violating the 45°C skin

temperature limit specifications set for the current design. By improving the thermal spreading, the peak temperature drops below the critical limit (Figure 1(a)).

The new proposed spreading metric is important both for thermal and electrical design/performance. At present, to meet the various performance specifications (skin/junction limit temperatures), the processors are throttled to reduce the power that leads to exceeding the limits. It is in the interest of the chip/device manufacturers to come up with a system level solution that will increase the overall electrical and thermal performance. This prompted the need for a heat spreading metric.

DEFINING THE COEFFICIENT OF THERMAL SPREADING (CTS)

We define the specific figure of merit associated with the heat spreading efficiency, a metric which we will call the "Coefficient of Thermal Spreading" (CTS). This metric indicates that by designing towards improvements in the CTS, we can improve the heat spreading and enhance the power handling capacity of a given phone/mobile device, achieving higher performance.

Figure 1 suggests that the variation of the surface temperature is decreased as the thermal design quality improves. One strategy for defining the CTS would be to evaluate the standard deviation of the temperature about its average value, $T_{\rm ave}$. The maximum temperatures depicted for the two phone designs in Figure 1 suggest the following:

$$CTS = \frac{\theta_{ave}}{\theta_{max}} = \left(T_{ave} - T_{ambient}\right) / \left(T_{max} - T_{ambient}\right) \tag{1}$$

Equation (1) is simply the ratio of the average temperature rise on the phone surface to the peak temperature rise. This ratio is dimensionless and increases to unity as the phone approaches a "perfect" thermal design, with uniform case temperature, for which \mathbf{T}_{ave} and \mathbf{T}_{max} are the same. In contrast to a metric based on the standard deviation, Equation (1) is directly related to power and maximum surface temperature, the key inputs/deliverables of the design process. Improving the CTS translates directly into a reduction of the maximum surface temperature for a given power.

To develop a quantitative metric, it is a useful to assume a constant value of the convective heat transfer coefficient, h, over the entire surface, in part because the local heat transfer rate varies due to a variety of external parameters. Equation (2) shows that for a given power and surface area, the *average* surface temperature is independent of the phone design. A poorly designed phone has hot/cold regions, but the average surface temperature is the same as of a well designed phone, assuming equal power generation and surface area for both devices.

$$P_{phone} = h A \theta_{ave} \tag{2}$$

where $P_{phone}[W]$ is the total heat generated in the phone; A is the total surface area, and $\theta_{ave} = T_{ave} - T_{ambient}$ is the average phone surface temperature rise relative to the ambient air.

There is another way to calculate the CTS, which may be more straightforward depending on what information is available. Making use of Equation (2), we calculate the CTS using:

$$CTS = \frac{P_{phone}}{hA\theta_{max}} = \frac{P_{phone}}{P_{perfect}}$$
(3)

where $P_{\it phone}$ is the power generated without rising above the case temperature limit and $P_{\it perfect/ideal}$ is the power removed from a phone with perfect internal spreading.

Equation (3) is useful for extracting the CTS from infrared imaging data, which can provide a solid estimate of the maximum temperature rise.

MEASURING THE CTS

IR imaging was performed to gain understanding of the CTS metric. The benchmark use case is Quad-Dhrystone and the device is in vertical orientation (Figure 2(a)). Test details/equipment: a) K-type thermocouple measures the ambient temperature; b) data logger records the thermocouples temperatures; c) IR camera measures the LCD/Back Cover peak/average temperatures; d) Wait 40 mins until surface temperatures reach steady-state, start CTS measurement.

Since the surface emissivity of LCD/back cover is unknown, three K-type thermocouples (designated as 1 through 6, three on

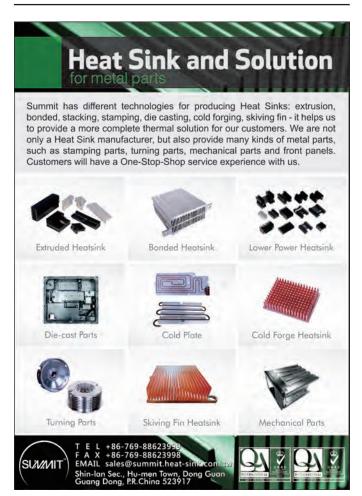
each LCD/Back cover surface) were mounted at low/medium/high-temperature zones at LCD/Back cover (Figure 2(b)). The thermocouple readings were used as the reference temperature to calibrate the emissivity of the LCD/Back cover surfaces. The surface emissivity setting of the IR camera is adjusted until the temperature difference between the thermocouple and IR camera reading is less than 1°C. The determined surface emissivity is the emissivity of the LCD/Back cover surface.

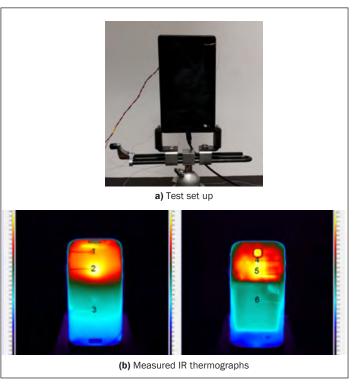
There is potential for further reduction in the tests variability (due to the open air environment) by using JEDEC closed box [5], with modified port for IR camera access. This deserves further evaluation, in case the industry is moving towards the CTS concept adoption.

To capture the temperature profiles: a) Run power intensive use case; b) Capture the surface temperature using IR camera; c) Port the IR temperature data into .csv file; d) Do an area weighted average of the surface temperatures for the display/case surfaces; e) Extract the overall device skin maximum temperature; f) Calculate CTS = $(T_{ave, skin} - T_{ambient})/(T_{max, skin} - T_{ambient})$. Figure 3 summarizes the CTS measurement over 30 minute: CTS peaks at 0.62 for this specific device.

EXAMPLE APPLICATIONS OF THE COEFFICIENT OF THERMAL SPREADING (CTS)

We expect the CTS to guide the design improvements and interactions with the phone/mobile manufacturers/companies. We completed several simulation/CFD studies of phone





Note Thermocouple locations 1 to 6 defined in (b). **Figure 2:** IR imaging of commercial phone.

design incorporating differing spreader geometries, at various powers. Figure 4 plots the simulated maximum surface temperatures as a function of heat spreader geometry and power.

For a phone that is cooled sufficiently well, increasing the CTS guides to higher power capacity without overheating the case. In Figure 4, the green arrow draws attention to three successive simulations for increasing spreader size that allow the power to be increased from 2.2 to 3.5 W without overheating the skin. Larger spreaders allow the CTS to increase from 0.5 to 0.8. By increasing the CTS of a device from 0.5 to 0.8, there is over 1.2W Power benefit and the skin limit stays at 45°C.

For problem phone designs (device skin is too hot), increasing the CTS should guide to a working design, or to the conclusion that the power is unmanageable. The blue arrow in Figure 4 draws attention to three successive simulations at 3.5W constant power, for which increasing the spreader size (thus increasing the CTS) drops the maximum skin temperature from $\sim 60^{\circ}\mathrm{C}$ to the required 45°C limit.

For the case of 6.7W and the big spreader, the red arrow suggests that the CTS needs to be increased above unity to function properly. This is impossible, as the CTS reaches a maximum of one for a perfect/isothermal case, meaning that power reductions will be essential. For that specific device platform, the maximum power using an ideal CTS is limited to 3.8W.

Finally, the CTS is a figure of merit for the design geometries/materials, and should be independent of the power level for the given use case/s. The dashed blue lines in Figure 4 show that, for a given spreader dimension, the CTS is essentially independent of the phone power. The dashed lines are not perfectly vertical because of the slight temperature dependence of the thermal properties.

Although the CTS is power independent for specific use case/s, the CTS *does* vary with time. If Equation (1) is evaluated as a function of time, while the device is heating up, the CTS evolves with time and approaches higher degree of uniformity in steady state. The CTS remains largely independent of power levels, although this can become more complicated if the power is time varying as well.

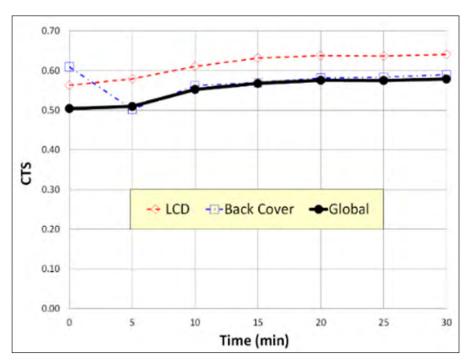


Figure 3: Calculated Coefficient of Thermal Spreading extracted experimentally for commercial phone

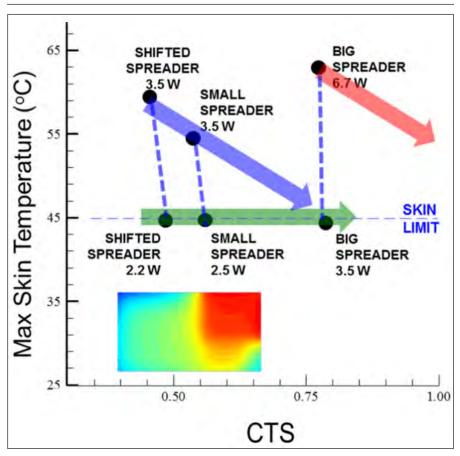


Figure 4: Maximum skin temperature versus CTS. Note: (i) The phone designs along the **green arrow** are limited by skin temperature, with power chosen specifically to meet that limit. (ii) The designs along the **blue arrow** show what happens to the skin temperature, for a constant given power, through improved thermal design. (iii) The **red arrow** suggests that it is impossible to improve a design sufficiently to cool very large power loads.

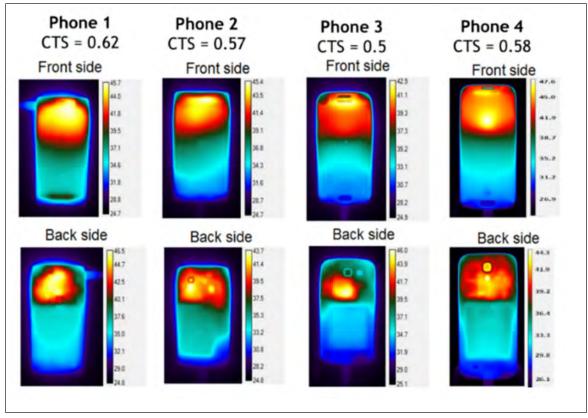


Figure 5: Measured IR temperature surface thermographs and CTS values for several commercial phones. CTS calculated using Equation (3) and the infrared imaging data. The temperature scale is different for each phone.

QUANTITATIVE DESIGN TARGETS USING THE CTS

The CTS is a powerful tool as it enables the best performing mobile/portable electronic devices. Chip manufacturers can define a minimally acceptable CTS level to ensure that their chips are cooled appropriately and deliver a level of performance that customers will find compelling/favorable. While all companies should strive for a CTS approaching unity (the perfectly cooled phone/mobile), eventually the costs associated with internal thermal management may become excessive. With improvements in thermal technologies, the higher CTS/performance devices should increase.

Our internal thermometry work has evaluated CTS values from 0.5 to 0.62 for various commercial phones (Figure 5): these numbers are critical because they translate directly into allowable internal power generation levels. By encouraging the phone manufacturers to increase the CTS to higher levels — our simulations suggest 0.8 — it is possible to achieve better balance between performance and cost.

WHY IS THE CTS IMPORTANT?

The increased CTS leads to better heat transfer and reduced peak temperature at the phone surface. As the internal spreading improves (CTS from 0.43 to 0.84), the device skin temperatures drop below the critical values (no hot spot) and a smaller temperature gradient occurs across the device surface/s (Figure 6). The high CTS device dissipates an extra 1.2W before it violates

the skin limits compared to the design with low spreading efficiency (CTS = 0.43).

For the specific device tested/simulated: every 1° C skin temperature difference leads to 0.16 W change in power, and is achieved by reducing CTS by 0.03.

HOW CAN WE IMPROVE THE CTS?

To enhance the mobile device heat spreading (CTS): a) Optimize the PCB ground plane; b) Use larger copper content for solid ground plane layer; c) Connect all ground pins of key ICs directly to this layer; d) Separate hottest ICs; d) No high Power ICs overlap on opposite PCB sides; e) Place connectors on opposite sides of key ICs where possible.

ALTERNATIVE CTS FORMULATIONS?

The authors evaluated alternative CTS formulations: a) Tavg/ T_max; b) Tmax/T_ideal; c) T_ideal/Tmax; d) T_ideal_system/T_real_system. Due to the lack of a physical meaning or independence on ambient Temperatures, it was decided to select the most appropriate version, as defined by Equation (1).

CONCLUDING REMARKS

This article proposes a new, dimensionless thermal spreading effectiveness metric for mobile devices, named CTS (Coefficient of Thermal Spreading). The CTS value quantifies the internal thermal spreading of mobile devices, and is a

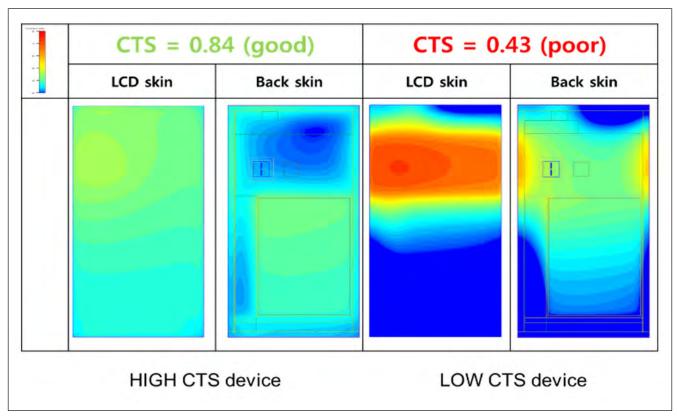


Figure 6: Comparison of calculated CTS values for poorly designed (CTS = 0.43) versus well designed (CTS = 0.84) devices: hot spot evident on poorly designed vs well spread heat on well designed phone skins. Note: CTS calculated using Equation (1) with average/peak skin temperatures from simulations. The temperature scale is the same.

specific metric to improve the thermal design. It indicates how much a given mobile device can be improved for the given shape/ size/form factor. As shown by simulations, optimally designed phones could reach CTS values between 0.8 and 0.9, while poorly balanced phones have CTS values below 0.5. Different mobile devices have different CTS values depending on overall size and internal design. CTS metric is used to help improve the thermal spreading over the device surface and reduce the skin maximum temperature. If adopted by the industry, the CTS Figure of Merit will lead to more thermally balanced phones/mobile devices.

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Saving Energy with Every Byte:

A Concerted Effort for Efficient Thermal Management of Data Centers

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ITH THE ADVANCEMENT OF TECHNOLOGY, the access to information has become rapid as well as ubiquitous. These mammoth resources which can be accessed through one click are stored and processed in data centers. These data centers are one of the largest and fastest growing energy consumption systems, and are expected to consume more than 140 billion kilowatt-hours of energy by the end of this decade [1]. Increasingly compact processors have shrunk the server volumes and increased the heat management issues faced by the data centers. Hence sufficient number of investigations over the last decade has focused on improving the thermal performance of data centers. Researchers have used numerical, experimental and computational fluid dynamic (CFD) analyses to study data centers from macro to micro level [2] with an aim to minimize the energy requirement for cooling. However there are still many challenges to be overcome in order to achieve efficient operation of data center due to its dynamic behaviour. Such challenges can be categorised in terms of: (i) the raised floor plenum data center models, (ii) rack layout with thermal analysis, (iii) energy efficiency with performance metrics, (iv) data center dynamics (control & life cycle analysis), (v) data center model validation and (vi) programming based optimization [3]. Coupling CFD models with

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Dr. Atul Bhargav is the Assistant Professor in Mechanical Engineering at Indian Institute of Technology Gandhinagar. He has completed his undergraduate studies from IIT Madras and PhD from University of Maryland. His research interests include energy systems design and optimization; experiments and numerical modeling of fuel processing for fuel cell applications; Fuel cell, HVAC, Co-gen and Tri-gen system modeling to study trade-offs and to develop control strategies and Multi-disciplinary system optimization. He is also looking into the regimes of nano-scale heat and mass transfer as well as thermal managements of commercial spaces. He has also developed the Energy Systems Research Laboratory at IIT Gandhinagar.



real time control and job placement algorithms can provide valuable insights and solutions to the above mentioned concerns. Although air cooling in data centres in some instances may reach its limits due to high thermal loading, it can still be managed effectively through close examination of flow and thermal dynamics of the system. Data center systems can be parameterised through standard metrics such as Power Usage Effectiveness (PUE) and Energy Reuse Effectiveness (ERE) through the server inlet-outlet temperatures, cold air flow rates, and power consumption. Hence there is a need for standardisation of these variables using the knowledge of system thermal behaviour through real-time measurements. Thermal behaviour of the system can be efficiently captured through predictive modelling on real-time basis and can be integrated with the control strategies.

The focus of this article is to consider how further improvements in efficiency of data centers can be obtained. In this context, a multi-disciplinary approach is proposed to data center cooling system design, data center layout design and data center operation. In previous work [4] the authors developed CFD models to understand the dynamics of the data center system which are the first building block for further model development. These CFD models leads to conclusion that the data center subsystems such

as plenum obstructions, perforation of tiles, server fans, structural arrangement of server racks and cooling systems all affects data center system performance. A summary of key challenges faced by data center personnel in the field of thermal management can be given as follows:

- 1. Are these steady state and transient CFD models sufficient to model data center thermal issues? Is steady state CFD analysis sufficient? What is about the computational time?
- 2. If the answer to the previous question is yes, then what is the accuracy of these models? If no, then what are the tools apart from CFD will help to address the heat management issue?
- 3. Data centers are highly dynamic in nature, is it possible to develop the models that can capture these dynamism?
- 4. Is there standardization to tackle the heat management through ASHRAE? Are those helpful for data center operators?

While addressing solutions to the above questions it's intuitive that the structural arrangement of the data center system may affect the system performance. To cool the servers efficiently, data centers have special arrangements such as raised floor plenum (RFP) with different supply and return structure though overhead block arrangement. These arrangements can substantially alter the data center thermal profile.

To understand the thermal performance of the data center system, detailed tile perforation of data center system was studied from the previous work [5]. At the same time perforation of the tiles and obstruction in the plenum chamber affects thermal profile of the data center system. Hence, using the analysis of perforation tile details the flow distribution and thermal performance of the system was studied and validated for various test cases on conventional raised floor data center. Thus there are two prominent cases reviewed in this article, 1) Verification of detailed perforated tile geometry and quantification of tile air flow-rate and 2) Flow distribution analysis in

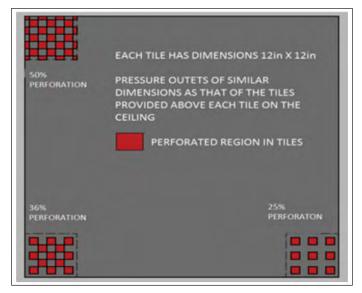
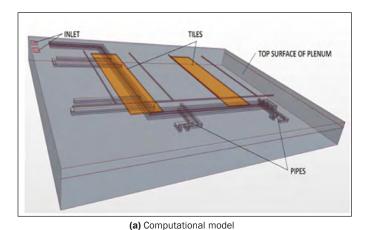


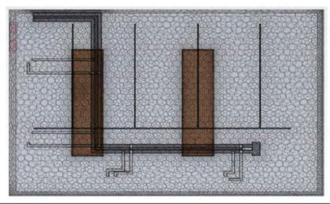
Figure 1: Top view of computational domain for detailed geometrical study of perforated tiles.

the raised floor plenum chamber with seven test models.

To quantify the effect on cold air flow rates by different perforation of tiles a rectangular computational domain was prepared for CFD study. Each tile of 2m × 2m at three corners of the domain modelled with 25%, 36% and 50% perforation. The grey area is flow domain while the red area indicates the perforation in figure 1. The geometry of the tiles was analysed in terms of flow rates and thermal profiles at different perforations. While comparing the perforated tile modelling with the available actual system data it was found that to model 25% and 56% tiles, the CFD model must incorporate 56% and 100% open area, respectively. The reason behind it can be explained in terms of momentum loss of air. Cold air from Computer Room Air-Conditioning (CRAC) units while passing through perforated tiles forms a single large jet through combinations of small jets of air formed due to perforation. During

Table 1: Porous inertial resistance (P) and number of mesh cells for each CFD model assessed.			
Model	Geometry	P (kg.m-4)	Number of Mesh cells in 100,000
А	Plenum chamber	29	1.49
В	Plenum chamber with pipes	29	63.4
С	Plenum chamber (with modified pressure loss coefficient)	630	0.9
D	Plenum chamber with pipes (with modified pressure loss coefficient)	630	6.34
E	Plenum chamber having pipes above a data center room	630	0.57
F	Plenum chamber without pipes above a data center room containing server racks	630	0.94
G	Plenum chamber with pipes above a data center room containing server racks	630	1.04





(b) Computational mesh (plan view)

Figure 2: Details of plenum obstructions incorporated in all seven computational domains, Table 1.

this phenomenon cold air loses significant momentum.

Furthermore seven computational models were built with various combinations of plenum chamber with and without obstructions, data center room and server racks (Table 1). All the computational models were incorporated in a commercial CFD software [6] for steady state analysis. The operating characteristics of the system are detailed in Table 2.

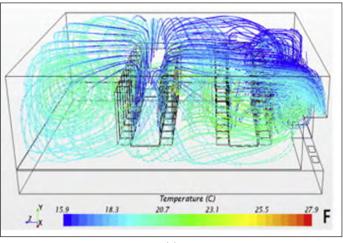
Table 2: Data center operating conditions.		
Cold air temperature	15 °C	
Ambient temperature	25 °C	
Cold air flow rate	6 kg/s (per CRAC)	
Server rack heat source	10 kW (per rack)	

To overcome meshing challenges while introducing obstructions in plenum chamber all the pipes were modelled with rectangular cross section for ease in polyhedral mesh generation. Figure 2 shows the structure of the obstruction incorporated inside the plenum chamber with meshing details.

The details of Navier-Stokes mathematical formulation with turbulence models can be referred from [4]. The air flow inside the system was assumed to be steady state and isothermal. Porous resistances across the tiles plays an important role in modelling perforated tiles in computational domain. The momentum equations with segregated solvers includes the porous media body force where the inertial and viscous resistances across the tiles can be provided. These resistances

are sensitive with pressure loss coefficients. Hence first four models (A to D, Table 1) were useful for fixing the pressure loss coefficient to account the momentum loss for its further use in next complex models.

Tile cold air flow-rates with modified pressure loss coefficients were matched with the experimental data from the literature [7]. Hence, it is suggested that the modified pressure loss coefficient values should be used while modelling the perforation tiles. The flow field and thermal profiles was observed on the models (F & G, Table 1) that contains all details of the data center system (Figure 3). It was found that the obstruction can lead to an increase in temperature by 2.5 °C as well as decrease the air flow rate up to 80% [4]. The performance of the data center can be enhanced by routing the under floor blockages, ducts and pipes. Therefore there is need to develop standardised codes that would guide the placement of obstruction for efficient construction of the system.



(a)

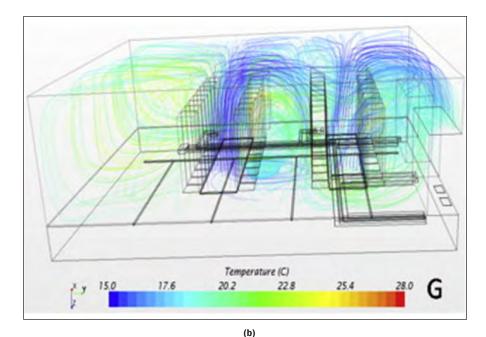


Figure 3: Temperature tracking through streamlines in a CFD model of data center room with (a) plenum and servers without obstructions (Model F) and (b) with obstructions (Model G), Table 1.

There are many such arrangements of the racks that may lead to efficient thermal management of the data center. Such different structural arrangements can be assessed using CFD analysis but will be difficult to validate. Still the question of CFD analysis remains questionable in terms of computational time and experimental validation. The steady state CFD modelling may be sufficient to understand the physics of the actual data center. As a possible improvement, transient analysis has been reported in recent studies but are expensive in terms of computational time [8], [9]. Also there are many difficulties while actual modelling of the server systems, cooling units and perforation tiles which is the focus for most researchers including ASHRAE standards. However the real time data center system data of various variables will be a key for CFD model validation as well as formulation of the mathematical models of the system. Data center itself is very complex and dynamic in nature and hence difficult to have the data with all possible input changes of the system. Hence there is a need for a scaled down testing facility which can mimic the actual data center facility. However, the implementation of such scaled down testing is difficult with flow and thermal dynamics matching between actual and scaled down system needing to be captured through dimensionless analysis.

The successful implementation of prototype testing will be breakthrough research for data center operators. Apart from that, all the CFD analysis and system testing will provide real-time data of server temperature, air flow rates, etc. Controlling the air flow rate as per the demand in specific server rack locations is the main objective for all type of data centers to save the power consumption. This objective forms the basis to develop the control strategies that includes the thermal model from the available testing data.

ACKNOWLEDGEMENT

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Vendor Workshops
Tear-down Sessions
Evening Tutorial

WEDNESDAY

MARCH 16, 2016 Technical Sessions Luncheon Speaker Exhibition Vendor Workshops How-To Courses Networking Reception

THURSDAY

MARCH 17, 2016 Technical Sessions-AM and PM

FRIDAY

MARCH 18, 2016 JEDEC JC 15 Meeting

EXHIBITION

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Exhibit space is still available. semi-therm.org

NEW SESSIONS FOR 2016

Industry Hot Issues in Thermal Management Thursday, March 17- 2:00-pm -5:00 pm

This is a Thursday afternoon session focused on pressing thermal concerns
• Future of Mobile Computing

- Power, performance and thermal challenges in the client market segment
 - Energy storage/transient topics and multifunctional material topics
 - · Future trends in data center challenges

EVENING TUTORIAL Tuesday March 15, 7:30 PM Panel Discussion: Open Compute Project

What began as Facebook's design efforts to scale its computing infrastructure in the most efficient and economical way possible has resulted into Open Compute project, which has sparked a collaborative dialogue amongst peers in industry. The effort has lead the "open sourcing" of hardware design and data center infrastructure with participation and contributions from multiple members. The panel comprising of some of these members will discuss the philosophy and workings of the open compute project focusing on mutual benefits arising from such collaborative efforts.

Inaugural Thermal Hall of Fame Awarded to Robert E. Simons Presented by SEMI-THERM Educational Foundation

The Hall of Fame recognizes persons in the electronics thermal management field who have made significant contributions to the development and commercialization of thermal management technologies during the course of their careers. Hall of Fame members are entrepreneurial in their own right, pushing the boundaries to develop and commercialize technologies while mentoring those around them. They are respected in the field for sharing of their knowledge in a multitude of ways – technical papers and presentations, course teaching, lectures, participation in conferences and symposia.

Robert E. Simons received a B.S. degree in Mechanical Engineering from Widener University, Chester, PA, and an M.S. degree in Operations Research and Applied Statistics from Union College, Schenectady, NY. In 1962 he designed heat shields for re-entry vehicles at GE and then joined IBM in 1966 working in thermal engineering. He was a key participant in the design and development of cooling technologies for the IBM 3033, 3081, and 3090 computer systems, as well as the development of direct liquid



BOB SIMONS

immersion cooling techniques. As a co-inventor of the cooling scheme for the IBM Thermal Conduction Module (TCM), he received an IBM Outstanding Innovation Award, and has received numerous IBM invention achievement awards. He is an inventor on over 80 issued U.S. patents and has published over 60 papers and book chapters. He has been active in the Semi-Therm conference since its inception, serving in the capacities of session, program and general chairman. Prior to retiring from IBM in 1995, he was a Senior Technical Staff Member and manager in the Advanced Thermal Laboratory at the IBM Development Laboratory in Poughkeepsie, NY.

SHORT COURSES

For the first time in 2016, full technical conference passes now include free short courses on Monday March 14, 2016

These outstanding technical courses are focused on the thermal sciences and are presented by leaders in the thermal field.

SHORT COURSE 1 Monday March 14, 8:00 AM Heat Sink Theory, Fundamentals, and Advanced Applications Instructors: Herman Chu and Martin Vogel, Juniper Networks

In this Course, the instructors will provide fundamentals on designing and assessing key heat sink attributes- thermal performance, airflow characteristics, and spreading resistance with various materials and geometries. For advanced topics, the latest developments in heat sink technologies, such as high findensity, high-fin-aspect ratio hybrid heat sinks and high heat spreading heat sink base technologies, along with derivations of compact heat sink models will be covered. As part of the advanced topics, the instructors will include overview on evaluating heat pipe and vapor chamber heat sinks and provide guidance on when these technologies are appropriate since they are significant cost addition to the overall heat sink. If time permits, the instructors may touch on advances in mini-cold plate developments.

About the Instructors:



Marlin Vogel



Herman Chu

Marlin Vogel is presently a Distinguished Engineer at Juniper Networks where he has led cooling technology roadmap development since 2010. Previously, Marlin was at Sun Microsystems for 18 years where he conducted research, development, and productizing of thermal technologies for CPU. He led the CPU module and system thermal development efforts for the high end Sparc servers. Prior to joining Sun Microsystems, Marlin was a member of the General Dynamics Thermodynamics Analysis group for 7 years serving as co-leader of the thermal design effort for a Navy stealth jet aircraft engine exhaust.

Herman Chu is a Senior Staff Engineer at Juniper Networks. His primary responsibilities are product developments for thermal, power conservation and acoustics disciplines. His current passion is to educate and drive reduced power/efficient designs for electronics in order to continue the growth of the IT infrastructure globally that is sustainable.

SHORT COURSES

SHORT COURSE 2 Monday March 14, 8:00 AM
JEDEC JESD 51: Thermal Standards with Hands-on Demonstrations
Instructor: Eduardo De Los Heros, Amkor Technology

JEDEC thermal resistance standards are used routinely by both packaging engineers and system designers. This JEDEC Thermal Testing Standards short course provides an overview of experimental testing hardware including details such the design of a thermal test vehicle, cold plates, still air chamber and installation of thermocouples. A hands-on experience is provided allowing students to run actual thermal testing apparatus including a Theta ja still air box, Theta ja moving air wind tunnel, Theta jb and Theta jc cold plates. Several different package styles will be tested including a small PBGA, large FCBBGA and a QFN package. Lastly, students will gain an appreciation for the correct method for using JEDEC thermal standards and how to apply them to make general thermal analyses.

About the Instructor:



Eduardo De Los Heros

Eduardo De Los Heros is a Senior Thermal Engineer at Amkor Technology with over 4 years of experience as a testing engineer. He has extensive experience in designing thermal test vehicles, design testing systems, data acquisition and supporting large scale testing programs. Eduardo obtained his Bachelor's degree in Mechanical Engineering from Arizona State University in Tempe in December of 2011.

TEAR-DOWN SESSIONS TUESDAY MARCH 15

Tear down sessions are open to anyone attending the symposium and/or the exhibition at no charge.

Thermal Design in Mobile Application Space Presenter: Phillip Fosnot, Amkor Technology.

New Generation, Lower Cost LED Lightbulbs
Presenter: Patrick Bournes, Gambit, Inc.

SHORT COURSES

SHORT COURSE 3 Monday March 14, 8:00 AM Thermal Modeling Using Excel Resistance Networks Instructors: Bruce Guenin, Oracle; Cathy Biber, Intel

This course will introduce attendees to efficient use of spreadsheets as a complementary tool to commercial numerical software. There are many situations in which a spreadsheet analysis can help you to

- plan the simulation strategy,
- include non-thermal aspects of the problem like weight or cost,
- attain a general understanding of expected model behavior,
- uncover trends and fundamental limits, and
- expose sensitivities that will affect model results.

By analyzing the problem using first principles, we force ourselves to think about the problem more thoroughly and broadly. This saves time by eliminating infeasible alternatives, identifying major sensitivities, and more.

We'll start with demystifying spreadsheet setup and introducing some relevant examples. The second half of the course will be students actively working on their own spreadsheet in a guided hands-on example.

About the Instructors:



Bruce Guenin



Cathy Biber

Bruce Guenin is a Principal Hardware Engineer at Oracle. He specializes in the development of advanced packaging technologies and in thermal and mechanical simulation and testing. He is an Associate Technical Editor of Electronics Cooling Magazine and a past chairman of the JEDEC JC-15 Thermal Standards Committee and the SEMI-THERM Conference. His contributions to the thermal sciences have been recognized by receiving the Harvey Rosten Award in 2004 and the Thermi Award in 2010. He received the B.S. degree in Physics from Loyola University, New Orleans, and the Ph.D. in Physics from the University of Virginia.

Cathy Biber currently works on thermal design and temperature management of slim mobile devices at Intel. She often gets to use both spreadsheet analysis and CFD skills honed over her career as a consultant and thermal engineer in electronics, solar and lighting equipment, and thermal processing.

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SHORT COURSES

SHORT COURSE 4 Monday March 14, 1:30 PM

Transient Measurements to Extract Resistances and Material Properties
Instructor: Andras Poppe, Mentor Graphics

This course covers advanced topics selected from the field of thermal measurement of packaged semiconductor devices with the transient method. The transient method is based on capturing the real-time thermal transients completed with mathematical algorithms to turn the measured Zth(t) curves into structure functions. The test results evaluation procedure discussed in detail is the NID method (network identification by deconvolution). The tutorial will "de-mystify" the famous structure functions; through practical examples it will be shown how they are used in real applications. The course will include but not be limited to, the following topics:

- 1. Thermal transient testing: measurement methods and available tools (transient extension of the JEDEC JESD51-1 "static" electrical test method; comparison of the JESD51-1 "static" and "dynamic" test methods)
- 2. Post processing of the measured Zth(t) curves by the NID method: time-constant spectra, structure functions, compact thermal RC models derived from Zth(t) curves
- 3. Structure functions as models of the physical structure. Using structure functions for heat-flow path reconstruction and for modeling purposes including validation/calibration of detailed CFD models and test based compact thermal modeling of power semiconductor device packages
- 4. Principles of structure function based thermal property measurements and application examples such as TIM testing or the transient method of measuring RthJC (JEDEC JESD51-14) standard
- 5. Overview of the LED thermal testing standards (JEDEC JESD51-5x series)
- 6. Non-destructive structure analysis: advanced case studies such as continuous, on-line monitoring of failure development during power cycling reliability tests

The theoretical part of the tutorial will be completed with practical examples and hands-on demonstration using Mentor Graphics' thermal testing hardware and software tools.

About the Instructor



András Poppe

András Poppe, PhD, was one of the co-founders of MicReD, now part of Mentor Graphics Mechanical Analysis Division. Currently at Mentor Graphics, he supports business development of the MicReD products. András obtained his PhD and MSc degree in electrical engineering from the Budapest University of Technology (BME), Faculty of Electrical Engineering. From 1986 to 1989 he was a researcher at BME Department of Electron Devices. His research field was circuit simulation and semiconductor device modeling. Since 1996 he has been working at BME as an associate professor. He is actively involved in the JEDEC JC15 and CIE TC2-63 and TC2-64 standardization committees. His fields of interest include thermal transient testing of packaged semiconductor devices, characterization of LEDs and OLEDs, electro-thermal simulation.

SHORT COURSES

SHORT COURSE 5 Monday March 14, 1:30 PM
Thermal Measurement Errors and Common Mistakes
Instructors: Dr. Alfonso Ortega, Villanova; Dr. Robert Moffat, Stanford Emeritus

The measurement of temperature in electronic equipment is one of the most common needs in the evaluation of thermal performance and reliability. Because of the apparent simplicity of building and using thermocouple sensors, the errors that commonly occur in the measurement of both air and solid component temperatures are not well appreciated. If ignored, these errors will propagate throughout the measurement chain and lead to high uncertainty in the measurements to be interpreted. Because experimental verification has become an essential part of computational simulation using CFD tools, lack of certainty in the "real" data will also lead to an inability to validate the computational simulations.

In this course, we will discuss and perform hands on demonstrations of practical temperature measurements that are common in the characterization of electronic equipment. We will point out difficulties in the use of point-sensors such as thermocouples in the measurement and interpretation of temperature of flowing fluids in air and liquid cooled systems, and in the measurement of the temperature of solid materials. We will discuss the errors that commonly occur in alternative methods such as Infrared measurements. With understanding of the source of errors, we will discuss the use of uncertainty analysis in order to understand and control the propagation of error in the measurement chain.

About the Instructors:



Dr. Alfonso Ortega



Dr. Robert J. Moffatt

Dr. Alfonso Ortega is the James R. Birle Professor of Energy Technology and Associate Vice President for Research and Graduate Programs at Villanova University. He is the Director of the Laboratory for Advanced Thermal and Fluid Systems which he founded in 2005. He is the Site Director for the NSF Center for Energy Smart Electronic Systems (ES2) founded in 2011 with Binghamton University, University of Texas-Arlington, and Georgia Tech. Dr. Ortega is an internationally recognized researcher in the areas of thermal management of data centers and electronic systems, convective and conjugate heat transfer in complex flows, experimental measurements in the thermal sciences, and thermal management in energy systems. He is the author of over 300 journal and symposia papers, book chapters, and monographs.

Dr. Robert J. Moffatt has ten years of experience with the General Motors Research Labs and thirty-one years at Stanford University working on heat transfer and experimental methods. He pioneered the use of uncertainty analysis in experimental planning. Dr. Moffat worked with Dr. Alvin Hackel, a pediatric anesthesiologist, to develop the Stanford Transport Incubator for inter-hospital transport of critically ill premature infants for which he was rewarded the ASME Melville Medal. He has more than 240 publications. Dr. Moffatt retired from teaching and remains active in research and consulting.

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SEMI-THERM HOW-TO COURSES WEDNESDAY, MARCH 16

How to courses are a series of free courses developed to introduce practical knowledge of thermal issues to marketing or technical personnel who are new to the thermal management field. The courses will be presented from 6PM to 8PM in two parallel sessions on Wednesday, March 16 2016, at SEMI-THERM 32.

Attendees will benefit from the exposure to terminology and will learn about alternatives to address certain thermal issues, and practical techniques and tips. Each course will last about 50 minutes. The courses are open to anyone attending the symposium and/or the exhibition at no charge. Seating will be limited so attendees should plan on coming early.

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Enhanced Pool Boiling using Separate Liquid-Vapor Pathways for Cooling High Heat Flux Electronics Devices

Satish G. Kandlikar^{1,2} and Arvind Jaikumar²

¹Mechanical Engineering Department, Rochester Institute of Technology ²Microsystems Engineering Department, Rochester Institute of Technology

INTRODUCTION

HE ADVANCEMENTS IN MICROELECTRONICS AND micro-electro-mechanical systems (MEMS) devices to meet the miniaturization trend has placed an increasing demand on thermal management. Single-phase cooling techniques utilize sensible heat transfer mode which is reliable, but is incapable of sustaining the increasing thermal trends as the design is generally pressure drop limited. Furthermore these cooling techniques present large temperature increase in the working fluid that is undesirable. Two-phase cooling offers attractive cooling possibilities by using the latent heat in which the liquid contacting the heated surface changes its state to vapor and removes large amounts of heat. The heat removal process is governed by two performance parameters (i) Critical Heat Flux (CHF) and (ii) Heat Transfer Coefficient (HTC). At CHF, a vapor layer encapsulates the surface preventing the liquid from contacting the surface and significantly hampering the heat transfer. In other words, the CHF is the upper governing limit of the efficient heat dissipating regime in the boiling mode. On the other hand, the temperature difference needs to be maintained at a minimum which dictates the efficiency of the heat removal process. Equation (1) gives the relationship between HTC, heat flux and the temperature difference between the surface (junction) temperature and the saturation temperature of the liquid employed.

Satish G. Kandlikar is at RIT since 1980 and is currently the Gleason Professor of Mechanical Engineering. He received his Ph.D. degree from the IIT Bombay in 1975. He has worked extensively in the area of flow boiling and CHF phenomena at microscale, single-phase flow in microchannels, electronics cooling, and water management in PEM fuel cells. He has published over 400 journal and conference papers. He is the recipient of the 2012 ASME Heat Transfer Memorial Award. His recent work on pool and flow boiling has produced exceptionally high heat fluxes along with very high heat transfer coefficients.



Arvind Jaikumar is currently pursuing his Ph.D. in Microsystems Engineering at the Thermal Analysis Microfluidics and Fuel Cell Laboratory at Rochester Institute of Technology (RIT). He obtained his bachelors in mechanical engineering from Visvesvaraya Technological University (VTU), Karnataka, India and his Master of Science in mechanical engineering from RIT, Rochester, USA. He is engaged in creating micro/nano structures and coatings for enhancement in pool boiling heat transfer.



$$HTC = \frac{q''}{\Delta T_{sat}} \tag{1}$$

where HTC = heat transfer coefficient (W/m²°C), q'' = heat flux (W/m²), ΔT_{sat} = wall superheat (°C) = $T_{surface}$ - $T_{saturation}$.

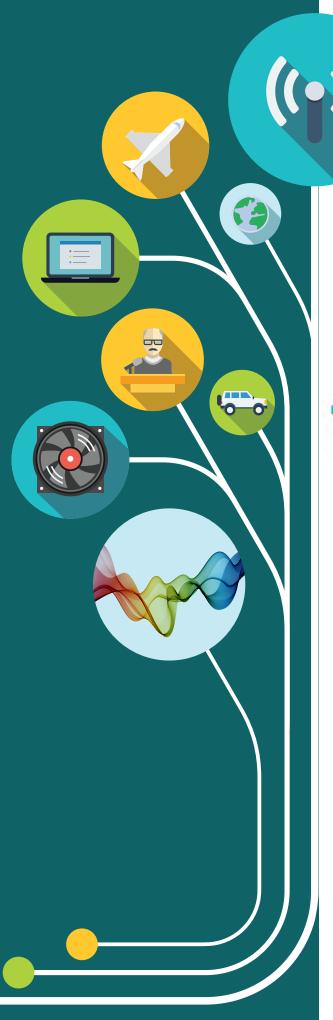
The HTC is inversely related to the temperature difference so a high value is desirable to keep the surface temperatures low. Moreover the convective thermal insulance (R_{th}) at the interface of the heater surface and the boiling fluid is the inverse of HTC as shown in equation (2):

$$R_{th} = \frac{1}{HTC} \tag{2}$$

where R_{th} = thermal insulance (m²°C/W).

In the last decade researchers have employed a wide variety of surface enhancements including microgrooves [1], pin fins [2], porous coatings [3] and graphene coatings [4] to reach a CHF of 150 - 200 W/cm2 with water. Area enhancement, availability of additional nucleation sites and liquid wettability changes were identified as the chief contributing enhancement mechanisms. A plain copper surface without any enhancement feature results in a CHF of 128 W/cm² with distilled water and 11 W/cm2 with FC-87 which is a dielectric fluid. These values are used here to serve as a baseline for enhancement comparisons.

A new class of enhancement technique has been proposed recently [5-7]. Fundamental pool boiling mechanisms



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suggest that liquid rewetting i.e. liquid supply to the nucleation site after the bubble has departed from the nucleation site is critical in extending the CHF. Kandlikar [5] developed a contoured fin surface in which the bubble motion was governed by evaporation momentum force. In this surface, the nucleation site was formed at the intersection of fin and land. The resulting bubble trajectory was such that it travelled along the contour of the land with subsequent liquid addition through the fin as shown in Figure 1 (lower left image). This technique resulted in a CHF of 300 W/cm2 at a temperature difference of 4.9 °C with an extremely high HTC of 62.9 W/cm2°C. This formed the foundation for the development of surfaces with separate liquid-vapor pathways.

In another configuration which comprised of open microchannels and porous coatings, Patil & Kandlikar [6] used a two-step electro-deposition process to coat the fin tops of open microchannels with copper. The resulting surface had a cauliflower like morphology with the pore size ranging between 5-20 µm as shown in Figure 1

(lower middle image). This influenced the nucleation to occur on the fin tops with subsequent liquid addition through the channels regions similar to a jet impingement like mechanism. This resulted in a CHF of 325 W/cm² at a temperature difference of 7.3 °C. Jaikumar & Kandlikar [7] investigated three surfaces by using screen printing and sintering on open microchannels and were identified as (i) sintered-throughout (porous coatings completely covering the microchannel geometry), (ii) sintered-channel (porous coatings inside the channel) and (iii) sintered-fin tops (porous coatings on fin tops) respectively. The porous coatings yielded a pore size similar to that of Patil & Kandlikar [6]. While the performance of sintered-throughout surface was enhanced by increased nucleation activity, the sintered-fin-tops and sintered-channels generated separate liquid-vapor pathways. The sintered-channel was capable of sustaining the separate

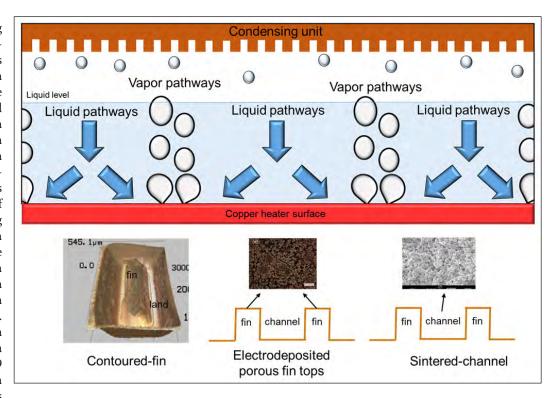


Figure 1: Schematic showing separate liquid-vapor pathways with nucleation regions on the heater surface and liquid supply pathways surrounding the nucleation sites (top). Enhanced microstructures and coated surfaces with separate liquid-vapor pathways developed by the authors (bottom)

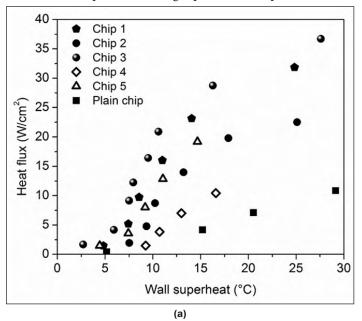
Chip no:	Channel width (µm)	Channel depth (µm)	Fin width (µm)	CHF (W/cm²)	HTC (W/cm²°C)
Plain chip				11	0.4
1	300	400	200	31	1.6
2	400	200	200	22	1.1
3	400	400	200	37	2
4	762	400	200	10	0.6
5	762	200	200	19	1.3

Table 1: Dimensions of open microchannel geometry used in the study with FC-87 as the boiling liquid.

liquid-vapor pathways at higher heat fluxes which resulted in a CHF of 303 W/cm² and a HTC of 31.5 W/cm²°C with water.

Although water is a popular fluid with good thermal properties it cannot be easily extended to electronics cooling applications due to its conducting nature and high saturation temperature. With a typical temperature limit of 85 °C imposed by the electronics industry, it is important to obtain an experimental database with dielectric fluids (i.e. FC-87, FC-72, HFE, *etc.*) which are more suited for electronics cooling application. Jaikumar & Kandlikar [8] extended the work conducted by Patil & Kandlikar [6] to FC-87. Figure 2(a) shows the pool boiling curves obtained with the enhanced surfaces. The heat flux is represented in units of W/cm² which is the desirable units for electronics cooling applications. Chips 1 to 5 have different dimensions which are listed in Table 1. A CHF of 37

W/cm² was obtained with this surface with a highest HTC of 2 W/cm²°C. Similar liquid-vapor pathways to that observed with water was found. Generation of separate liquid-vapor pathways simultaneously increases the CHF and HTC, and offer a wide operating range by effectively removing heat at small temperature differences compared to its single-phase counterparts.



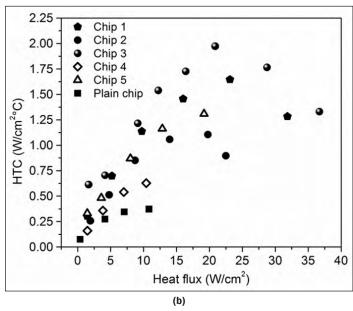
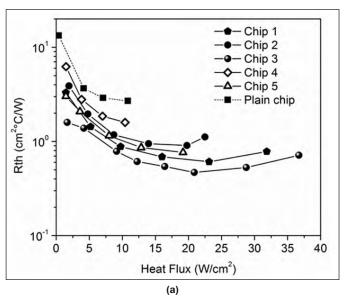


Figure 2: Boiling characteristics for FC-87 at atmospheric pressure for chips 1-5 listed in Table 1. (a) Pool boiling (b) heat transfer coefficient [8].

Figure 2(b) is a plot of the variation of HTC with heat flux where the HTC is deduced by dividing the heat flux and the temperature difference (wall superheat) value. Maximum HTC is obtained between heat fluxes of 15-20 W/cm². The maximum HTC obtained for a plain chip is 0.4 W/cm²°C whereas these values for the enhanced surface are between 0.6-2 W/cm²°C. The five chips defined in Table 1 were studied to understand the effect of channel width and depth. Channel width is the distance between

two fins and serves as the liquid pathway. This region is where the liquid impinges on to the surface before turning towards the fin tops similar to a jet impingement like mechanism. The channel depth is the depth of the channel from the fin tops to the bottom of the channel. The channel width and depth investigated in this study were between 300 µm and 762 µm. The nucleation sites which are porous copper coatings were strategically placed on the fin tops which serves as the preferential vapor removal pathway. Figure 3 (a) and (b) shows the variation of thermal insulance with heat flux using FC-87 and water, respectively. The general trend indicates that the thermal insulance reduces at higher heat fluxes. Furthermore, the figure shows that the thermal insulance for the enhanced surface with separate liquid-vapor pathways (with both FC-87 and water) is significantly lower than that of a plain chip showing that the liquid is efficiently contacting the surface and enhancing the heat transfer.



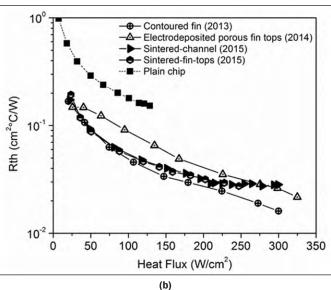


Figure 3: Measured variation of thermal insulance with heat flux for test chips investigated in Table 1 with (a) FC-87 and (b) Water.

The performance values indicate that the cohesive effect of channel width and depth dictates the degree of enhancement. The channel width and depth govern the quantity of liquid turning towards the fin tops and the flow resistance the liquid has to overcome to reach the fin tops, respectively. A closer examination revealed that a channel width to depth ratio of unity enhanced the performance significantly which is in complete agreement with the results obtained with water. When this ratio is smaller than unity then the channel depth is more and the liquid will be unable to reach the channel bottoms and turn towards the fin tops; the flow resistance dominates such surfaces and deteriorates the performance. When the ratio exceeds unity the liquid impingement suffers and the reduction in area hampers the performance.

There is a need to further investigate the performance of aforementioned enhancements [5,7] with dielectric fluids. Some of the thermal considerations that make two-phase cooling attractive for high energy density components are: (i) better and efficient cooling performance (ii) a high factor of safety (for reaching CHF) as the vapor chamber offers a wider operating range. As an example, for a 20 W/cm² thermal load, the vapor chamber performance shown in Figure 2 provides a CHF value of up to 37 W/cm² thereby giving an extra 30-40 % operation range. (iii) The componential cost is also significantly reduced as there is no inclusion of pumps and other flow regulating devices.

CONCLUSIONS

The development of enhanced surfaces with separate liquid-vapor pathways has shown immense potential to increase both CHF and HTC simultaneously. Furthermore a distinct advantage of these heat exchangers is that they can be manufactured using conventional milling, computer numerical control (CNC) milling, embossing technique, *etc.* The porous coatings can be deposited using screen printing, electrodeposition, spray coating, *etc.* which make it feasible for cooling high heat flux devices. The research presented shows that the separate liquid-vapor pathways can be effectively utilized with water as well as dielectric fluids in enhancing pool boiling heat transfer.

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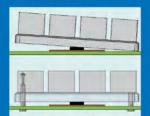
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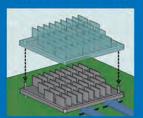
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