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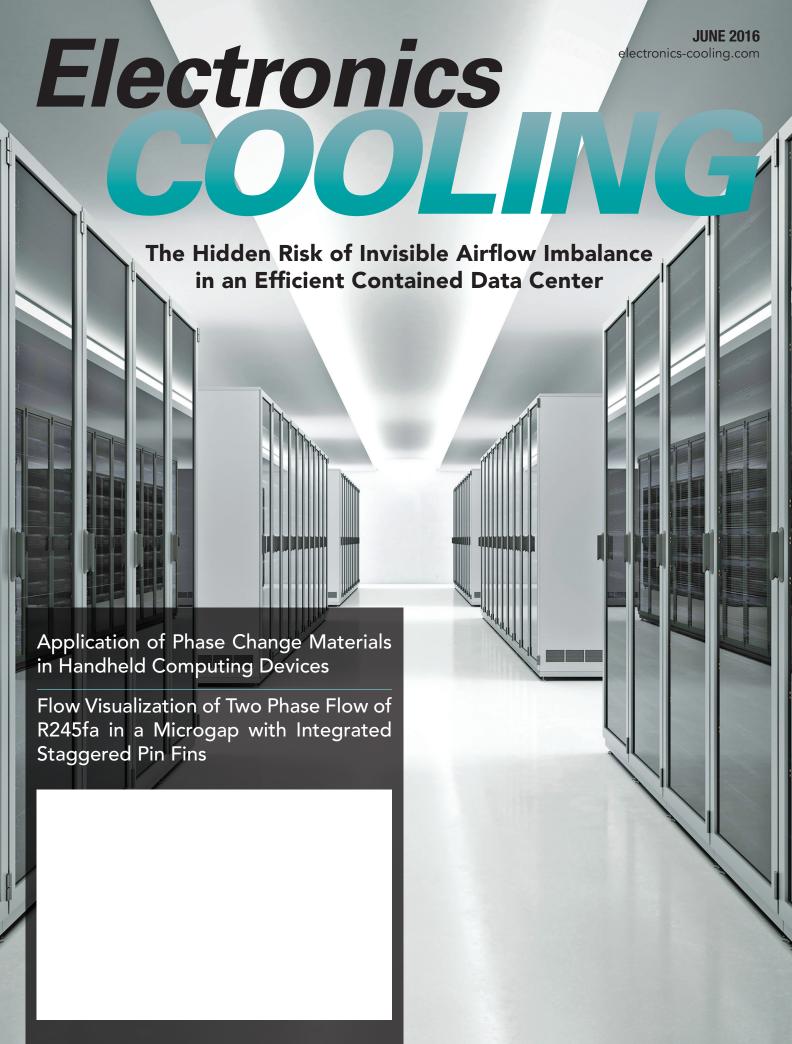
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## **Editorial 2016**

#### It Takes a Village – To Raise an Engineer

**Bruce Guenin, Acting Editor-in-Chief, June 2016** 



**ur modern world is infused** with technology. Wherever we turn, we find constant improvements in our cars, appliances, our phones and other gadgets. The improvements extend beyond the devices themselves to the very means of producing them. Equally compelling are the advances in software that operate more and more within the rich fabric of internet connectivity.

The workings of all this technology are largely a mystery to non-engineers. Nonetheless, products representing all of these advances grow in popularity to the point that they are seen as necessities by a large segment of our population.

Behind all of these developments that have transformed our lives are a myriad of engineers. To most people, engineers seem so different from the general population. To begin with, they are not intimidated by technology.

In contrast they actually enjoy the complexity of it. When they see a technical problem, engineers instinctively go toward it, intent on dividing and conquering it. That is to say, implementing a process of breaking down a complex problem into a series of manageable portions that can be individually understood and made right.

It's interesting to consider the process of transformation that starts with a kid who might have been curious about how things worked and enjoyed tinkering with objects to repurpose them, and ends with a professional engineer.

Along the way, there were educational experiences in which teachers and other mentors not only provided instruction to these young people but also served as role models as they shared their own fascination with science, math, and technology and their own strategies for problem solving in the context of the classroom, lab, or science projects.

The process continues through their more formal training at the college level and even after they enter the working world. It extends far beyond the mere transmission of technical knowledge to these emerging professionals.

Social scientists refer to these organizations that help our formation not only as professionals, but also as responsible adults and citizens as institutions. Their purpose includes the education and nurturing of their participants. They also serve to transfer values from one generation to another. Their agenda contains an explicit commitment to investing in and developing the "human capital" of their members.

To succeed as an engineer into today's complex, interconnected, and rapidly changing world requires more than just technical knowledge. Because of the magnitude and complexity of today's technical challenges, engineering, by its very nature, is collaborative. It requires that engineers work well in groups and communicate effectively with one another.

There are, invariably, in the course of any major project these days, technical challenges that were not anticipated, as well as the omnipresent schedule and cost pressures. As they mature in their profession, it's important that engineers develop a process for making sound decisions, even when there are no good options and when schedule pressures are immense.

The role of mentors is very important in this process of maturation. In the course of our careers, we are mentored by teachers, bosses, and colleagues, who populate the various organizations we participate in. They share their know-how and demonstrate patience in pursuit of their own project goals. They encourage us to persevere, even as we are in the depths of despair as we face challenges that seem overwhelming at the time. They provide the glue that binds these mini-societies together.

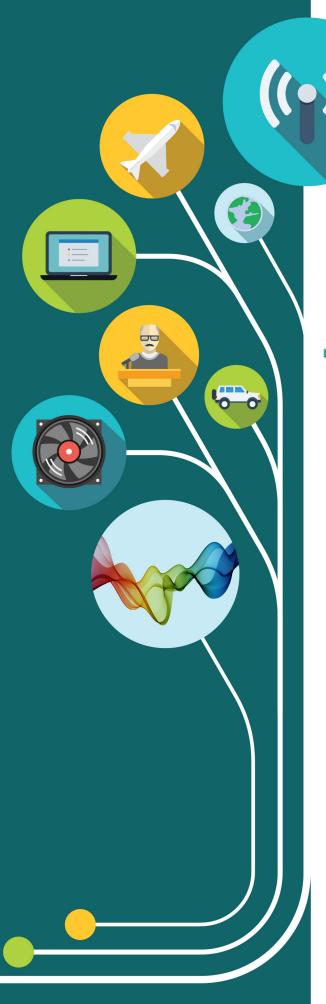
In the engineering profession, there are institutions beyond the corporations and universities that provide the same sort of benefits to their members. These include professional societies, conferences, and industry standards organizations. In these economically-turbulent times, they offer an advantage in that participation in them and the resulting personal relationships can be maintained even after one's corporate address has changed.

Now that ElectronicsCooling is in its 21st year of existence, perhaps it also could be considered an institution in our field.

#### **Milestones**

In his editorial in the March issue, my fellow editor, Jim Wilson, stated that it would his last one as a lead editor. I'd like to acknowledge the significant contributions Jim has made to this publication over the 12 years he has been associated with it. With his profound knowledge of thermal science and engineering and his consummate professionalism, he has been a major asset to our editorial team. I wish him the best. Meanwhile, Jim has graciously offered to provide continuing editorial support as we seek his replacement.

Also, I'd like to offer my warm congratulations to one of our former editors, Bob Simons, who has received the inaugural Semi-Therm Hall of Fame Award. It was great to see his many contributions to our field honored in this way.



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# **Cooling Matters**

### News of thermal management technologies

## LAPTOPS MAY START PRODUCING FAR LESS HEAT

(May 10, 2016) Massachusetts Institute of Technology's postdoc Cui-Zu Chang and his colleagues have been "working to create devices with components which have little [to no] resistance to the flow of electricity" in laptops, according to TechRadar.com.

Topological insulators, or, "exceptionally thin materials with special properties, which let electrons flow freely across the surface, but not through the bulk of the material", are the solution, reported TechRadar.com.

"Scientist Chang has been working in this field for some time, and achieved a major breakthrough last year when switching to use vanadium to produce atomically thin layers of magnetic topological insulators," said TechRadar, "[And] now, with further refinement, the researchers have managed to achieve zero resistance to a current flowing lengthwise along the edge of their circuit."

"These devices would produce far less heat, which could lead to all manner of breakthroughs in terms of less cooling, thinner notebooks, more powerful portables and generally more efficient computing," TechRadar.com reported.

#### LIQUID COOLING USED IN NEW OFF-GRID POWER GENERATOR AND WATER PURIFIER

(April 7, 2016) Watly has recently launched an Indiegogo campaign to raise the final needed funds for the release of its water sanitizing and electricity generating computer powered entirely by solar energy.

The Watly 3.0 "combines photovoltaic and thermal solar technology to sanitize 5,000 liters of water a day," while also "generating off-grid electricity that powers its internal electronics and can recharge external devices" and provide internet connection with its built-in router, reported PV Magazine.

According to PV Magazine, "The solar heat is used for vapor compression distillation, which can sanitize any water, no matter how dirty, while the PV panels on the roof of the machine generate the power needed for the internal electrics."

"The water is used to cool the solar PV panels so that it can function at optimum efficiency, and they then warm up the water to help the thermal solar system," said Marco A. Attisani, Watly Founder and CEO.

Attisani divulged his ultimate goal "is that enough Watly 3.0 machines are built to create their own network, and then from that their own grid."

## GRAPHENE NANOFLAKES BETTER DISSIPATES ELECTRONICS' HEAT

(April 29, 2016) Recently, a team of researchers from Chalmers University of Technology in Sweden have developed a more efficient approach to cooling electronics using graphene nanoflake-based film.

According to E&T, the team performed "experiments in which they managed to increase the efficiency of heat transfer by 76 per cent" – the kind of results that suggest "potential thermal management solutions for electronic devices."

"The graphene-based film was further enhanced by adding functionalised amino-based and azide-based silane molecules," E&T reported, "In simulations, the researchers observed how the functional layer constrained the cross-plane scattering of low-frequency phonons, which in turn enhances in-plane heat-conduction of the bonded film."

"In the research, scientists studied a number of molecules that were immobilised at the interfaces and at the edge of graphene nanoflake-based sheets forming covalent bonds. They also probed interface thermal resistance by using a photo-thermal reflectance measurement technique to demonstrate an improved thermal coupling due to functionalisation," according to E&T.

The research was published in the journal Nature Communications.

### Datebook.

#### **May 31 - June 3**

Electronic Components and Technology Conference – ECTC 2016

Las Vegas, Nevada, USA www.ectc.net

#### **May 31 - June 3**

ITherm 2016: Fifteenth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems

Las Vegas, Nevada, USA http://www.ieee-itherm.org/docs/ itherm2016cfp.pdf

#### June 2

## Thermal Engineering Show

United Kingdom
http://www.
thethermalengineeringshow.
co.uk/

#### **June 9 - 12**

### 21st Guangzhou International Lighting Exhibition

**Guangzhou, China** http://guangzhou-internationallighting-exhibition. hk.messefrankfurt.com/ guangzhou/en/for-visitors/ welcome.html

#### **NEW MATERIAL COOLS SOLAR CELLS YET ABSORBS SUNLIGHT**

Recently, researchers from Stanford University have achieved a combination of cooling and maintaining sunlight absorption with a wafer made of silica to better cool solar cells, according to BusinessWire.com.

BusinessWire.com explained, "The researchers etched tapered holes, about 6 micrometers across and 10 micrometers deep, in the wafer. The holes are designed to smooth the path the thermal radiation takes to escape." The team then "tested the silica layer by placing it on top of a solar cell mimic — a polished silicon wafer with an antireflection surface and aluminum back that has similar absorption characteristics to standard solar cells, but wasn't actually wired to produce electricity."

According to BusinessWire, "the testing verified that because the silica layer is transparent, approximately the same amount of sunlight still reaches the

solar cell mimic." They even said they found a "slight increase in absorption because of anti-reflection and light trapping effects of the etched silica," and the temperature was "lowered 13° C compared to the bare solar cell mimic."

Linxiao Zhu, a graduate student in the research group of electrical engineering professor Shanhui Fan, said, "What's unique about our work is that we demonstrate radiative cooling while preserving the amount of solar absorption." Zhu also said that radiative cooling is a "mostly untapped resource" that "relies on the coldness of the universe."

Other applications that could benefit from this cooling approach, "especially since the new research shows it can work without significantly altering the sunlight absorption characteristics of an underlying material," could be "cooling cars, clothing, and outdoor equipment," Zhu also said.

## POTENTIAL ELECTRONICS COOLING APPLICATION OF CARBON NANOTUBES

(April 21st, 2016) A technique has been found that could allow carbon nanotubes to be used in electronic cooling and as devices in microchips, sensors and circuits in the future.

Phys.org reported that the technique "uses a laser and electrical current to precisely position and align carbon nanotubes" to make it a "potential new tool for creating electronic devices out of the tiny fibers."

The technique is called "rapid electrokinetic patterning (REP)" and "uses two parallel electrodes made of indium tin oxide, a transparent and electrically conductive material," said Phys.org, "The nanotubes are arranged randomly while suspended in deionized water. Applying an electric field causes them to orient vertically. Then an infrared laser heats the fluid, producing a doughnut-shaped vortex of circulating liquid between the two electrodes. This vortex enables the researchers to move the nanotubes and reposition them."

Phys.org explained that, "the technique overcomes limitations of other methods for manipulating particles measured on the scale of nanometers, or billionths of a meter. In this study, the procedure was used for multiwalled carbon nanotubes, which are rolled-up ultrathin sheets of carbon called graphene. However, according to the researchers, using this technique other nanoparticles such as nanowires and nanorods can be similarly positioned and fixed in vertical orientation."

These findings were published by the Nature Publishing Group in a paper led by Purdue doctoral student Avanish Mishra in the online journal Microsystems and Nanoengineering on March 24, according to Phys.org.

#### SELF-HEALABLE ELECTRONIC MATERIAL THAT CAN HELP PREVENT OVERHEATING

(May 16, 2016) A new, more durable electronic material has recently been created to repair itself and heal all its functionality even after breaking several times.

after breaking several times.
Phys.org detailed, "Self-healable materials are those that, after withstanding physical deformation such as being cut in half, naturally repair themselves with little to no external influence."

"Researchers have been able to create self-healable materials that can restore one function after breaking, but restoring a suite of functions is critical for creating effective wearable electronics," claimed Phys.org. That is to say, "if a dielectric material retains its electrical resistivity after self-healing but not its thermal conductivity, that could put electronics at risk of overheating."

Phys.org reported that the material the team created, "restores all properties needed for use as a dielectric in wearable electronics—mechanical strength, breakdown strength to protect against surges, electrical resistivity, thermal conductivity and dielectric, or insulating, properties." They added "boron nitride nanosheets to a base material of plastic polymer" which is much like graphene, except two dimensional and resists and insulates against electricity, rather than conducts it.

"The material is able to self-heal because boron nitride nanosheets connect to one another with hydrogen bonding groups functionalized onto their surface. When two pieces are placed in close proximity, the electrostatic attraction naturally occurring between both bonding elements draws them close together. When the hydrogen bond is restored, the two pieces are "healed"." according to Phys.org.

pieces are "healed"," according to Phys.org. The findings have been published online in Advanced Functional Materials.

#### INNOVATIVE WATER BOILING APPROACH COULD COOL ADVANCED ELECTRONICS

Oregon State University engineers have recently discovered a new way to make advanced electronics more efficient by inducing and controlling boiling bubble formations.

According to ScienceDaily.com, "The new approach is based on the use of piezoelectric inkjet printing to create hydrophobic polymer "dots" on a substrate, and then deposit a hydrophilic zinc oxide nanostructure on top of that. The zinc oxide nanostructure only grows in the area without dots. By controlling both the hydrophobic and hydrophilic structure of the material, bubble formation can be precisely controlled and manipulated for the desired goal."

With this technology, researchers say they will be able to "control both boiling and condensation processes, as well as spatial bubble nucleation sites, bubble onset and departure frequency, heat transfer coefficient and critical heat flux for the first time," which means it can be beneficial to either "boil water and create steam more readily, like in a boiler or a clothing iron; or with a product such as an electronics device to release heat more readily while working at a cooler temperature."

Chih-hung Chang, a professor of electrical engineering in the OSU College of Engineering, said, "One of the key limitations for electronic devices is the heat they generate, and something that helps dissipate that heat will help them operate at faster speeds and prevent failure. [...] The more bubbles you can generate, the more cooling you can achieve."

"Advances in this technology have been published in Scientific Reports and a patent application filed," reported ScienceDaily.com.

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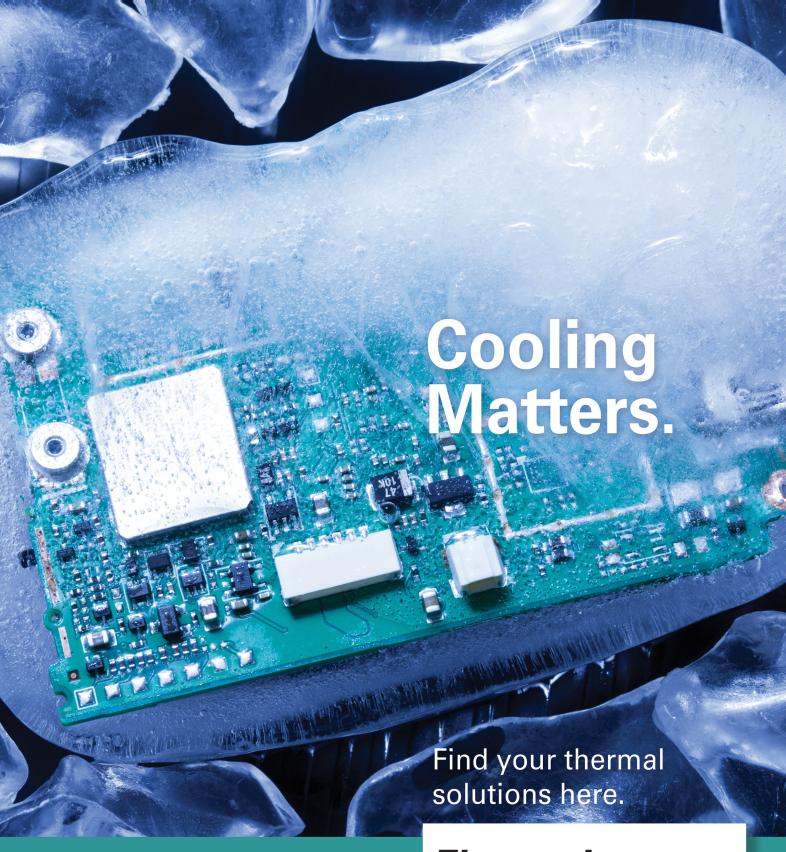
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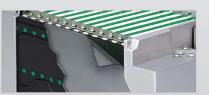
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## **Estimating the Effect of Flow Bypass on Parallel Plate-Fin Heat Sink Performance**

*Editor's note:* This is another in a series of reprints of Bob Simons' timeless Calculation Corner columns. Bob served as an Associate Technical Editor of this publication from January, 2001, to December, 2011.

For those readers who find this sort of tutorial useful, please refer to the list, compiled by Bob, of other Calculation Corner columns authored by him as well as by others: http://www.electronics-cooling.com/2011/09/a-useful-catalog-of-calculation-corner-articles/.

Bob Simons Reprinted from ElectronicsCooling, Feb., 2004

NPASTISSUES OF ELECTRONICS COOLING, methodologies were presented for estimating parallel plate-fin heat sink thermal resistance<sup>[1]</sup> and pressure drop<sup>[2]</sup>. The underlying assumption for both articles was that all the flow delivered by the fan is forced to go through the channels formed between the fins. As noted in the second article, this is often not the case and much of the flow delivered by the fan may take the path of least resistance by flowing around the heat sink.

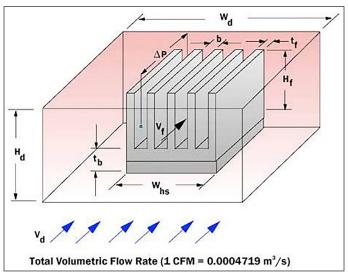


Figure 1. Parallel plate fin heat sink configuration in H<sub>d</sub> x W<sub>d</sub> flow duct.

This article will illustrate the use of simple flow equations (see Table 1) to estimate the air flow that actually passes through the fin passages of the heat sink in the presence of flow bypass. The heat sink geometry (see Figure 1) considered is the same as that in the earlier articles, but the heat sink is assumed to be in a duct of width  $W_{\rm d}$  and height  $H_{\rm d}$ . The flow delivered by the fan is assumed to approach the heat sink and surrounding free flow area with velocity  $V_{\rm d}$ . The total duct flow  $G_{\rm d}$ , is given by

$$G_d = V_d \times A_d \tag{1}$$

If the average air velocity through the heat sink fin passages is defined as  $V_{\rho}$  the flow through the heat sink,  $G_{h,r}$ , is given by

$$G_{hs} = V_f \times A_{hs} \tag{2}$$

It is assumed that the volumetric flow ratio of the air through the fin passages is constant throughout. The pressure drop,  $\Delta P$ , across the heat sink at the flow rate  $G_{\rm hs}$  through the heat sink is estimated using the method given in reference  $^{[2]}$ . The corresponding velocity,  $V_{\rm d}$ , in the duct approaching the heat sink is given by

$$V_d = \frac{-b + \sqrt{b^2 - 4 \bullet a \bullet c}}{2 \bullet a} \tag{3}$$

with the coefficients a, b, and c as given in Table 1. The derivation of Equation (3) is given in reference<sup>[3]</sup>. This velocity may then be used in Equation (2) to calculate the corresponding volumetric flow rate in the duct. If desired the amount of flow bypass may be calculated by subtracting the heat sink flow rate (Equation 2) from the total duct flow rate (Equation 1).

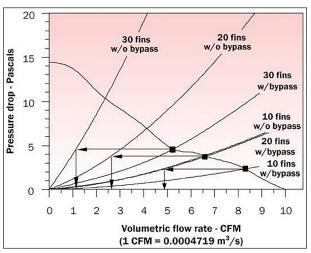
To illustrate the application of these equations, the same heat sink dimensions used in the preceding articles were used. An aluminum heat sink 50 mm wide x 50 mm long with 0.5 mm thick 25 mm tall fins was assumed. Calculations were performed for configurations of 10, 20 and 30 fins, with and without bypass.

For the case with flow bypass, duct dimensions 70 mm wide and 32 mm high were assumed, resulting in 10 mm clearance on either side of the heat sink.

Assuming several air velocities  $(V_f)$  through the heat sink, pressure drops  $(\Delta P)$  and corresponding volumetric flow rates  $(G_{hs})$  through the heat sink were calculated for the case without bypass as in reference<sup>[2]</sup>. These results were plotted to obtain the pressure drop curves (w/o bypass) in Figure 2. Equations (1) and (3) were then used to obtain the total duct flow rate  $(G_d)$  with bypass (i.e. flow through heat sink + bypass flow) corresponding to each of the assumed air velocities  $(V_f)$  through the heat sink. The pressure drops across the heat sink at each of the

Table 1. Summary of Bypass Flow Equations.

assumed air velocities through the fins was plotted versus the corresponding total duct flow rate with bypass to obtain the pressure drop curves with flow bypass.



**Figure 2.** Heat sink pressure drop curves (with and without flow bypass) and fan curve with flow operating points.

As in reference<sup>[2]</sup> the intersections of the fan curve and the pressure drop curves without bypass determine the volumetric flow rates through the heat sink. In a similar manner, the intersections of the fan curve with the pressure drop curves with bypass determines the total volumetric flow rate entering

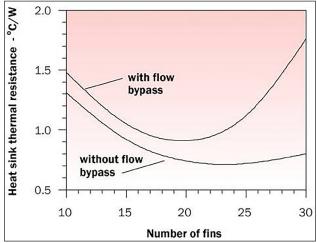
the heat duct. As shown in Figure 2, the pressure drop across the heat sink and the duct at positions corresponding to the inlet and outlet of the heat sink is also determined by the intersection of the fan curve and the pressure drop curves with bypass. Projecting horizontally at constant pressure drop to the pressure drop curves for flow through the heat sink (without bypass) gives the amount of flow actually passing through the heat sink.

Having determined the actual flow through the heat sink, the equations outlined in reference<sup>[1]</sup> were used to calculate the thermal resistance for each heat sink configuration with and without flow bypass. These results are summarized in Table 2.

Number of	CFM <sup>1</sup>	R <sub>th</sub>	CFM <sup>1</sup>	$R_{th}$
Fins	(w/o bypass)	(°C/W)	(w/bypass)	(°C/W)
10	6.6	1.31	4.9	1.48
20	4.1	0.74	2.6	0.91
30	2.4	0.8	1.1	1.76
$^{1}$ 1 CFM = 0.0004719 m $^{3}$ /s				

**Table 2.** Summary of Volumetric Flow Rates Through Heat Sinks and Corresponding Heat Sink Thermal Resistances (Heat Sink-to-Air).

The effects of the presence or absence of flow bypass and the number of fins on heat sink thermal resistance, are also shown graphically in Figure 3. As can be seen, the effect of flow bypass on heat sink thermal resistance can significantly increase heat sink thermal resistance as the number of fins increases.

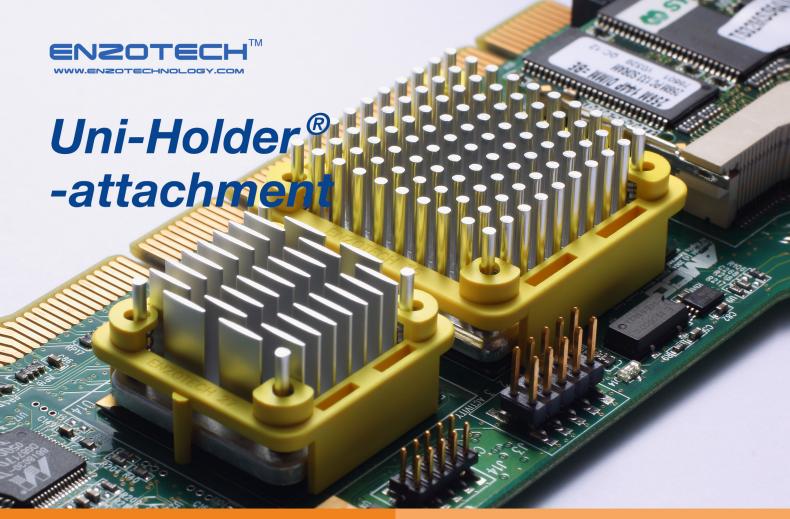


**Figure 3.** Effect of number of fins on heat sink thermal resistance with and without flow bypass.

Although the method presented here can be a useful tool for preliminary tradeoff estimates it should not be construed as a replacement for detailed computational fluid dynamic modeling or experimental verification.

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wire spring anchor — pedestal







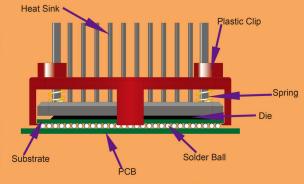




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## **Understanding and Defining Electronics Cooling Requirements**

Jim Wilson Associate Technical Editor

Y EXPERIENCE IN ELECTRONICS COOLING has taught me that it is often a fairy tale that thermal engineers fully understand requirements related to their designs and analyses, or that they fully understand the implications of subjecting thermal requirements on suppliers or coworkers. A rush to get a quick answer or to use the latest feature in an analysis software code often means jumping right into the analysis modeling tool and neglects the critical first steps related to refining the problem statement. The fact of this column is that taking the effort to comprehend thermal design and analysis requirements will minimize wasted effort and reduce the time required to optimize a design.

Near the start of thermal design or analysis task, it is important to understand why you are doing the work (often directly related to the phase of the product development cycle you are supporting) and what criteria will be used to assess when the task is complete. A few typical reasons for performing thermal analysis are:

- Assure that components will be within manufactures rated temperature limits
- Contractually obligated to perform the analysis
- Provide guidance to a design team for optimization considering thermal effects
- Develop performance metrics for electronics that are temperature sensitive
- Prevent thermally related failures in the products use
- Support reliability estimates for the product
- Develop thermal requirements for a supplier
- Provide thermal characterization information to a customer
- Develop the thermal architecture of a system<sup>[1]</sup>

In the case of design optimization, the completion criteria are often directly related to the available budget and schedule. For this type of work, the successful thermal engineers learn to tailor their effort to the available time and money. Experience is very beneficial, but even in its absence thermal engineers can perform analysis that is commensurate with the resolution of

the design data. Hand calculations may be all that is needed to properly refine requirements, assess sensitivities, and impact the product design in the initial stages. Making an informed decision on the appropriate level of detail for an analysis can be difficult. Determining the resolution of boundary conditions and other thermal parameters requires effort and some knowledge of the operating environment.

Once you have established why you are doing the work and when you will be done, it is appropriate to assess the design information available. A few common areas where uncertainty is often present are:

- Dissipated power estimates The values at an early stage may only represent a rough estimate and may contain excessive margin. A common thought process is to see if there are any thermal issues with a worst case estimate. If the subsequent analysis indicates acceptable performance then there is not a pressing need to revisit the thermal design, but the excessive margin is still present. In fairness to complex systems, actual thermal dissipation is sometimes not known with certainty until late in the design or testing phase.
- Material properties Just because a product data sheet lists a value does not mean this value is accurate. Items like thermal conductivity are difficult to measure<sup>[2]</sup>, and thermal interface material performance often depends on how it is used. Your design probably does not replicate the thermal characterization environment used to develop the advertised data.
- Accurate understanding of thermal margin in supplier delivered parts and requirements. It is often difficult to find supporting information that provides the basis for the cooling requirements (flowrates, mounting temperatures, etc) for some parts. For example, if a design goal is minimizing margin to enable a low mass design, using overly conservative vendor supplied parameters is not optimum.
- An understanding of how the parts are built and the associated tolerances. Parts are rarely built as

- perfectly as the design shows up in a solid model and the subsequent thermal model. Attachment layers may have voiding and the geometry is constrained by the manufacturing processes.
- Accuracy of the boundary conditions. In some cases the external boundary is reasonably well understood (a specified operating environment) but in some cases the thermal interface to another part of the system is described. Understanding and developing thermal requirements at this level usually takes time, especially if an understanding thermal margin is required. The reader is also cautioned against indiscriminate use of a fixed temperature boundary condition.<sup>[3]</sup>

After developing an understanding of what is needed to perform the thermal tasks and assessing the design information, the requirements for selecting appropriate software tools are usually evident. For example, the resolution of the modeling tool selected should be proportional to the accuracy of the design parameters and assumptions.

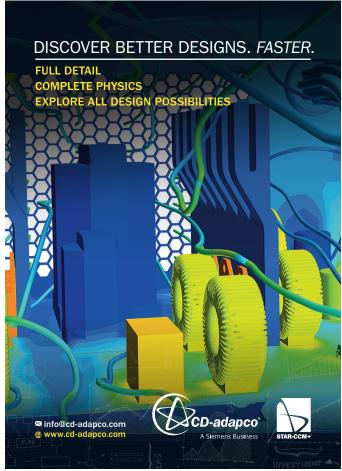
If the tasks include developing thermal requirements, giving consideration to the lists above at least allows a documentation of how they were developed and provides an initial set of information for sensitivity information.

While most thermal engineers are capable of solving a well posed problem, the fact that the problem is well posed should motivate one to make sure that the underlying assumptions required to define the problem in this manner are correct and applicable. Effective electronics cooling design work requires understanding how the system responds to its thermal environment and how the system changes as its thermal characteristics change. Additionally, relevant thermal requirements imposed on the system or derived from the system require attention at all phases of the design process. This helps avoid having a detailed design and analysis against requirements that are no longer completely relevant. A continuous collaborative exchange with other engineers is necessary for consistency between thermal requirements and the resulting design.

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## Visualization of Flow Boiling of R245fa in a Microgap with Integrated Staggered Pin Fins

Pouya Asrar, Xuchen Zhang, Craig E. Green, Peter A. Kottke, Thomas E. Sarvey, Andrei Fedorov, Muhannad S. Bakir, and Yogendra K. Joshi

#### INTRODUCTION

WO PHASE COOLING HAS BECOME a promising technique for managing high heat fluxes from electronic packages such as 3D stacked chips. Flow boiling in microchannel arrays has been employed in many applications<sup>[1-3]</sup>, and boiling regimes in different shapes of microchannels have been investigated<sup>[4,5]</sup>. In this article we have visualized the flow boiling of refrigerant R245fa in a different configuration of a pin fin enhanced microgap, which allows spanwise fluid movement for improved vapor management, as well as 3D electrical connectivity via the pins, to cool a footprint area of 1 cm x 1cm. The overall design of the pin fin test unit and the pin fin array dimensions are provided in Figure 2.

The working fluid used in this investigation, R245fa, has a much lower operational pressure compared to other refrigerants. Its charging pressure is 122 kPa at 20 °C, compared to 572 kPa for R134a at the same temperature. Also, the saturation temperature is within a reasonable range (15 °C to 85 °C) for thermal management of Si microelectronics.

Pouya Asrar received his Bachelor's degree in Mechanical Engineering from Sharif University of Technology. Prior to joining the Georgia Institute of Technology, he spent two years at Iowa State University to obtain his Master's degree in Mechanical Engineering. He then joined METTL lab in 2014 as a Ph.D. student. His current research is a micro cooling project with the focus on thermal analysis of two phase flow in 3D stacked ICs.



**Xuchen Zhang** received the B.S. degree in Electronic Engineering and the M.S. degree in Microelectronics from Shanghai Jiao Tong University, Shanghai, China in 2008 and 2011, respectively. He received the Dual-M.S. in electrical engineering with the Georgia Institute of Technology, Atlanta, GA, USA, in 2012, where he is currently pursuing the Ph.D. degree.



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### EXPERIMENTAL SYSTEM AND METHODS

Figure 1 demonstrates the schematic of the experimental setup. Before charging the system, the loop is evacuated using a vacuum pump<sup>[6]</sup>. As the next step, the source tank is warmed up to a temperature higher than room temperature to a typical value of 28 °C. A 1,000 ml reservoir is then charged with enough refrigerant before charging the rest of the system. In order to ensure that the syringes are fully charged, the reservoir is heated up to few °C higher than ambient temperature. Continuous flow becomes possible by having one of the pumps infusing, and the other one withdrawing simultaneously. After charging the pumps, the working fluid is pushed by one syringe pump towards the pre-cooler in the system in order to insure its liquid phase. The refrigerant passes through a microturbine flow meter<sup>[7]</sup>. R245fa is maintained contaminant-free by incorporating a 0.5 μm in-line filter<sup>[8]</sup>. It passes through a heat exchanger<sup>[9]</sup> before returning back to the 1000 ml reservoir.

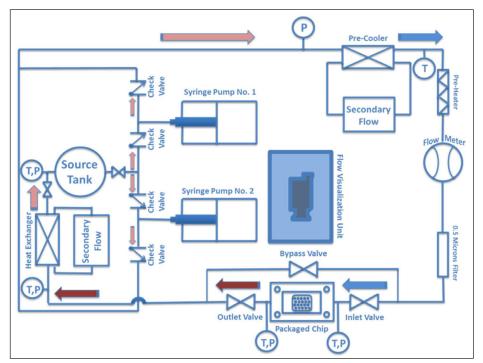


Figure 1. Flow Loop Schematic

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Steady state conditions are insured by running the system for a few hours, when variations are within 0.25% for pressure, and 0.5 °C for temperature in each pushing cycle. The heaters are then gradually powered at each heat flux, and all measurements are archived. Flow visualization is performed using a high speed camera<sup>[10]</sup> at 2,229 frames per second.

#### **FABRICATION PROCESS**

The 200 µm tall microgap consists of a 1 cm x 1 cm array of staggered cylindrical micropin-fins, as shown in figure 2i. The diameter and pitches of the micropin-fins are shown in Fig. 2i. Pressure ports are included on both sides of the micropin-fin array in order to accurately measure the pressure drop. Large mechanical support pins with diameter of 500 μm are added near the inlet and outlet to improve structural strength. Four serpentine platinum heaters/resistance temperature detectors (RTDs) with a thickness of 200 nm generate heat load and provide temperature measurements in four sections along the flow length (between inlet and outlet).

The fabrication process begins with the etching of the micropin-fins, followed by an anodic bonding of a glass lid to encapsulate the microgap. Next, the Platinum heaters are deposited on the silicon side. Finally, inlet, outlet and pressure ports are etched. The detailed fabrication process can be found in [11]. A cross-sectional schematic of the sample is shown in Fig. 2 ii.

#### **RESULTS AND DISCUSSION**

Starting from a small power (~ 1 W) applied to all four heaters; the power was increased gradually until two phase flow was observed in the microgap. The flow boiling first occurred near the exit of the microgap, and upon increasing the heat flux progressed towards the inlet. Figure 3 presents visualizations of the flow boiling for heat fluxes ranging from 11 W/cm² to 34 W/cm². Two phase flow started via nucleate boiling. Small bubbles were formed around pin-fins in the microgap, and

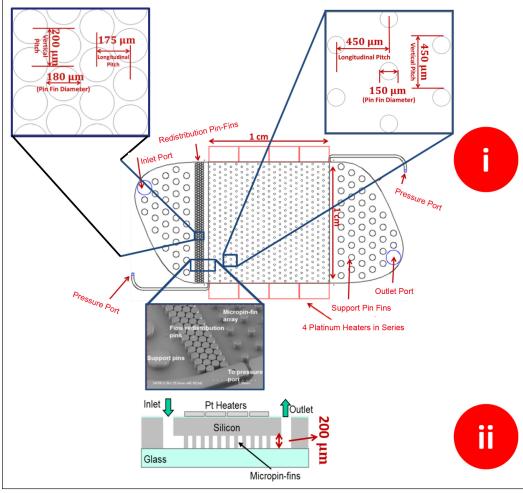


Figure 2. SEM Picture of the Device (i) and the Fabrication Steps (ii)

grew as they moved towards the outlet. As shown in figure 3, for heat fluxes of 25 W/cm<sup>2</sup> and above, the two phase region is evenly distributed over the microgap. This area progressed towards the inlet of the chip, as the heat flux increased. The red circles in Figure 3 identify the spots where the nucleation was observed around single pin fins. The nucleate boiling

Flow Rate: 15 mL/min

11
W/cm²
25
W/cm²
29
W/cm²
34
W/cm²

Figure 3. Flow Visualization Recorded with High Speed Camera at indicated values of heat flux

occurred at the first column of pin fins of the two phase area in the microgap.

A 1D heat conduction model was used to calculate the surface temperature at the interface with the refrigerant, corresponding to each heater temperature. Figure 4 illustrates the surface temperatures at all four heaters locations on the back of the chip. Heater 4 (closest to the outlet of the flow) showed the maximum surface temperature among all four heaters, whereas for heat fluxes above 25 W/cm<sup>2</sup>, heater 3 had the maximum temperature.

Figure 5 demonstrates the visualizations for heat flux of 11 W/cm² in more detail. Figure 5i clearly shows the triangular two phase wakes initiating at few locations along the pin fin array. This wake structure demonstrates the rapid spanwise spreading of bubbles generated around individual pin fins, as also observed by Isaacs et al.<sup>[8]</sup>. Figure 5ii illustrates the flow

boiling on a particular part of the gap at two different time frames. The first picture relates to the initiation of the bubbles around the pin fins, whereas the second clearly shows that a larger volume of vapor has covered the pin fins in the microgap, because of evolution of two phase region with respect to time.

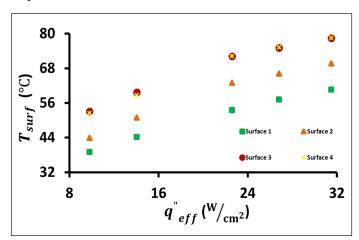


Figure 4. Surface Temperature Distribution

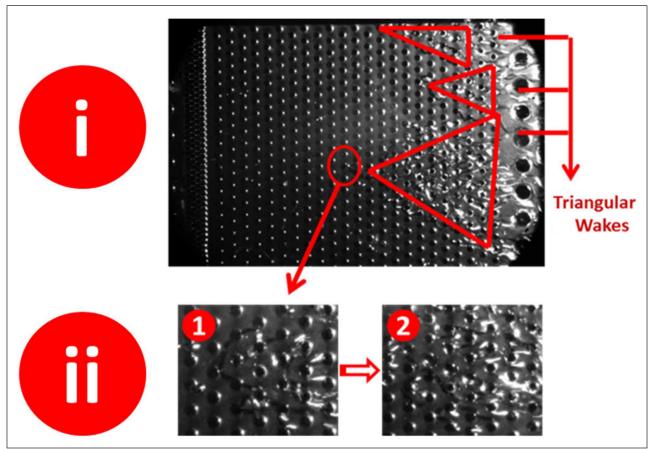


Figure 5. Triangle-Shaped Liquid/Vapor Wakes Happening at 11 W/cm² (i), Close-Up at the Nucleation Zone (ii) li-1: initial nucleation of bubbles

li-2: fully developed bubble production

#### **CONCLUSIONS**

A simultaneous visualization and thermal measurement study was performed on two phase flow of refrigerant R245fa in a test device having a microgap equipped with circular pin fins arranged in a relatively large footprint area of 1 cm x 1 cm. The heat flux ranged from 7 W/cm² to 34 W/cm². The nucleation zones around individual pin fins were visualized using a high speed camera. A maximum vapor quality of about 30% was calculated at the outlet of the test device. The enhanced microgap configuration offers a promising approach for two-phase thermal management of stacked chips.

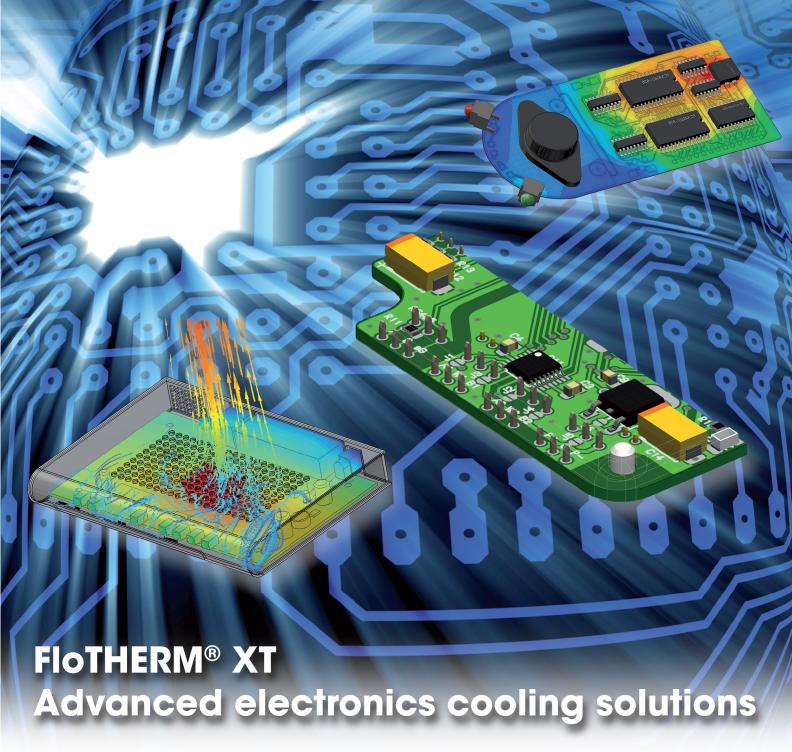
#### **ACKNOWLEDGMENTS**

The authors thank the DARPA IceCool Fundamentals Program for providing the financial support for this research.

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## The Hidden Risk of Invisible Airflow Imbalance in an Efficient Contained Data Center

Husam Alissa is a Ph.D. candidate at the State University of New York at Binghamton with a background in experimental and numerical transport analysis at the macro and micro scales. He is responsible for the experimental characterization of the ES2-Binghamton University new data center laboratory and CFD validations. He has worked on different experimental and numerical test setups from the facility level to the components level including IT air systems analysis, tiles performance, racks, aisles, containment and cooling units. His doctorate research work has resulted in more than 20 publications published or under review as well as multiple submitted invention disclosures. His current work is also focused on linking the effects of today's cooling solutions to the IT internal components' (CPUs, RAMs and HDDs) reliability, application delivery, and resiliency during failure events.



Kourosh Nemati is a Ph.D. candidate at the State University of New York at Binghamton, specialized in transport in data centers using both empirical and numerical approaches from server to room levels. He has characterized a fully-enclosed hybrid cooled server cabinet experimentally in Binghamton University data center. He has validated the enclosed cabinet numerical model in steady-state and transient mode with experimental data. In terms of airflow and heat capacity he has characterized different types of IT equipment experimentally and numerically. He has characterized a rear door heat exchanger experimentally and analyzed the thermal performance of rear door heat exchangers during different failure scenarios. His current study is focused on transient analysis of rack and heat exchanger of fully and partially enclosed systems for different kinds of failure scenarios.



Dr. Bahgat Sammakia is the vice president for research at Binghamton University and director of the NSF-IUCRC on Energy Smart Electronic Systems (ES2) and Binghamton University's Small Scale Systems Integration and Packaging Center (S³IP), a New York State Center of Excellence. He is a Distinguished SUNY Professor of mechanical engineering in the Thomas J. Watson School of Engineering and Applied Science. Dr. Sammakia has spent much of his research career working to improve thermal management strategies in electronic packaging systems at multiple scales ranging from devices to entire data centers. Dr. Sammakia joined the faculty of the Watson School in 1998 following a fourteen-year career at IBM where he worked in the area of research and development of organic electronic systems. He has contributed to several books on natural convection heat transfer and is also the principal investigator or co-principal investigator on several cross-disciplinary research projects. Dr. Sammakia is a Fellow of both the IEEE and the ASME.



#### **NEW SOLUTIONS, NEW CHALLENGES**

**ENERALLY, A LEGACY DATA CENTER** consists of an array of hot and cold aisles where the air intake to the IT equipment resides in the cold aisle and the air exhaust of the equipment rejects hot air into the hot aisle. In a raised floor environment, chilled air is supplied through the plenum to the cold aisle. The heated air in the hot aisle flow backs to the cooling unit return as shown in Fig. 1 (a). However, the recirculation of air from hot to cold aisles or vice versa is a common occurrence. This air recirculation endangers the well-being of servers and reduces data center cooling efficiency, resulting in an increased TCO. To resolve these issues cold or hot aisle containment (CAC or HAC) solutions were introduced to segregate the incoming cold air stream from the heated exhaust stream as shown in Fig. 1 (b & c). CAC or HAC cooling solutions allow higher chilled set point temperature and can enhance the performance of an air side economizer, which admits outside air to the cool air stream (when outside temperatures are low enough).

This segregation of the hot and cold air streams is referred to as containment. It is considered to be a key cooling solution in today's mission critical data centers. It promotes:

1. Greater energy efficiency: by allowing cooling at higher set points, increasing the annual economizer hours and reducing chiller costs.

- 2. Better use of the cold air and hence greater capacity: containment generates a higher temperature difference across the cooling unit making the most of the cooling coils capacity.
- 3. Less likelihood of recirculation so better resiliency (defined as the ability of a data center, to continue operating and recover quickly when experiencing a loss of cooling).

However, hot or cold aisle air containment (CAC or HAC) creates a new relationship between the IT air systems and the airflow supply source. In the legacy open air data center, each IT equipment is able to get its necessary airflow (i.e. free delivery airflow), independent of airflow through the other neighboring IT equipment, and also independent of airflow through the perforated tilesthrough the full range of air system fan speeds (i.e., varying RPM).

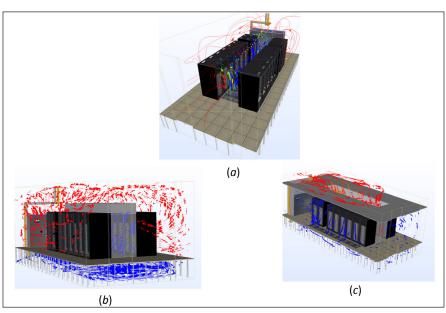


Figure 1. Schematic of (a) Legacy Open Hot Aisle-Cold Aisle (HA/CA) (b) Cold Aisle Containment (CAC) and (c) Hot Aisle Containment (HAC).[1]

To describe the potential issues with the containment, the design of a CAC system installed on a raised floor similar to Fig. 1 (b) is explained. Other containment solutions will have analogous exposures. The CAC solution is constructed such that the cold aisle is boxed to egregate the cold aisle from the rest of the data center. Airflow leakage paths through the CAC are minimized by the design. The result is that airflow for the IT equipment is delivered through the raised floor

Mark Seymour, a founder and CTO of Future Facilities delivering engineering simulation software and services to the data center industry to facilitate efficient and effective design, operational planning and capex/opex decision making particularly in relation to cooling. Mark started his career developing simulation software for the defense industry. In 1988 he started to apply his simulation knowledge to the built environment alongside full and part scale physical modeling and site investigations. As data center cooling became important in the 1990's his focus on the data centers increase and in 2003 he decided, with 2 colleagues to form Future Facilities providing modeling and associated services for design, assessment and operational planning of the IT halls. He is a corresponding member of ASHRAE TC9.9 and an Active member of the Green Grid and the NSF-ES2 project.



Ken Schneebeli has been an IBM Consultant in the areas of data center power, cooling, monitoring, availability, and energy efficiency for dozens of clients in US and internationally for 8 years. Prior to that, Ken was responsible for IBM storage product concept development, design, release, compliance, and support for 24 years. Ken currently has 11 patents issued, and is a BSME from University of Washington '82.



Dr. Demetriou is an Advisory Engineer at IBM Corporation in the IBM Systems' Advanced Thermal Energy Efficiency Lab focusing on advanced cooling technologies, cross brand thermal development and state-of-the-art data center designs. He received a Ph.D. in Mechanical and Aerospace Engineering from Syracuse University. He has authored or coauthored over 30 journal or peerreviewed publications and has several patents or patents pending. His work has been awarded numerous honors, including the ASHRAE Willis H. Carrier Award and the ASME Journal of Electronics Packaging Best Paper Award. He is a voting member of the ASHRAE TC 9.9 and an active member of ASME.



perforated tiles within the CAC. This causes a new airflow relationship between all the IT equipment enclosed by the CAC. There is no longer an unlimited supply of low impedance airflow from the open airroom for all the IT equipment with in the CAC. Instead, there is effectively a single source of constrained airflow through the perforated tiles. All of the IT equipment air systems are operating in parallel with each other and are all in series with the perforated tiles. As a result, the air systems for all the IT equipment will compete with each other when the airflow in the CAC through the perforated tiles is less than the summation of the IT equipment free delivery (FD) airflows. It can now be understood that different IT equipment will receive differing percentages of their design FD airflow, depending on the differing performance of each IT equipment air system when they are competing in parallel for a constrained airsupply.

Currently, there is a lack of IT equipment airflow data in the available literature. Such data is crucial to operate the data centers in which there is a perpetual deployment of containment solutions. Note that IT equipment thermal compliance is based on an implicit assumption of a guaranteed free delivery airflow intake. However, the airflow mismatches and imbalances

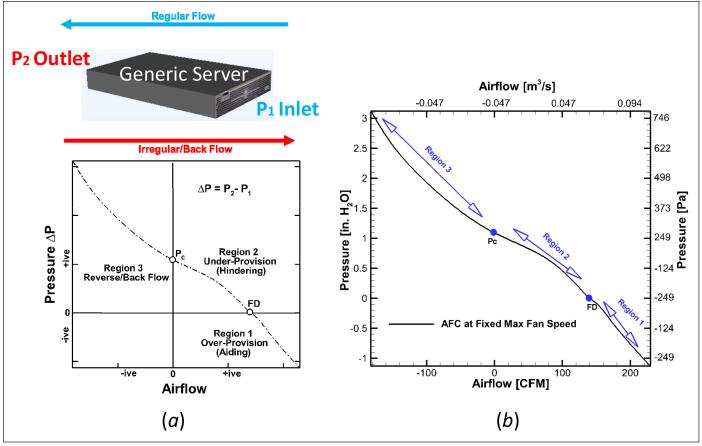


Figure 2. (a) Generic active flow curve (AFC) and (b) 2U New Generation server NG Active Flow Curve (AFC) at 100% fan speed.

can occur due to one or more of the following reasons: inherent variable utilization of the IT equipment; the practice of increasing set points to save energy; load balancing and virtualization; IT equipment with differing air flow capacity stacked in the same containment; redundant or total cooling failure; air filters derating with time; environmental changes during free cooling; maintenance of redundant power lines; initial airflow assumptions at the design stage; presence of physical obstruction at airflow vents; or rack/IT specific reasons (e.g. side intake vents in a narrow rack). For these reasons, understanding the IT airflow demand based on load and utilization becomes vital.

#### **GENERIC METHOD TO CHARACTERIZE IT AIR SYSTEMS**

For physical illustration, we will use a CAC scenario as an example. Fig. 2(a) shows the active flow curve (AFC) for a generic piece of IT equipment, where the pressure is measured at both the inlet and outlet<sup>[3]</sup>. Again, referring to a CAC scenario, the inlet or  $P_1$  is in the contained cold aisle. The outlet  $P_2$  is measured at the open hot aisle side. Obviously, the chassis is designed to pull cold air from the cold to the hot aisles (i.e. Regular Flow). From an aerodynamic point of view, the flow curve includes three regions of airflow that an operating server can experience.

Region 1 represents aided airflow. An example can be an over-provisioned CAC where  $P_2 < P_1$ . This will induce airflow rates that are higher than the free delivery or designed airflow through the IT equipment. Any operating point in this region

has a negative backpressure differential based on the definition of  $\Delta P$  and a flow rate that is always higher than point FD. The IT is said to be at free delivery (FD) or design airflow when the backpressure differential is equal to zero  $P_2$  -  $P_1$  = 0. This is analogous to an open aisle configuration, where the cold and hot aisle pressures are equal, or even a CAC scenario with neutral provisioning and an ideally uniform pressure distribution. Note that the FD point is implicitly assumed by IT vendors when addressing thermal specifications. However, the designed airflow may not be the actual operating condition in a containment environment. Therefore, both the inlet temperature and flow rate should be specified for IT, especially when installed with a containment solution. This becomes of great importance when the supply temperature is increased for efficiency, inducing variations in the server's fan speeds.

In region 2, the airflow of the IT is lower than the free delivery. This can be explained by an under-provisioned CAC situation where  $P_2 > P_1$ , hence, the positive backpressure differentials. As the differential increases, the airflow drops until reaching the critical pressure point at which  $P_2 - P_1 = P_C$ , after which the IT fans are incapable of pulling air through the system and into the hot aisle (airflow stagnation). Both points FD and  $P_C$  are unique properties of any IT equipment and are important to be identified by IT vendor specifications.

If the backpressure differential exceeds the critical pressure,  $P_2$  -  $P_1$  >  $P_C$ , then the system moves into region 3 in which the

airflow is reversed which means that the backpressure is high enough to overcome the fans and induce back airflow from hot to cold aisles through the IT chassis. This irregular flow behavior occurs when placing IT equipment with different air flow capabilities in the same containment [3, 4]. Generally speaking, IT equipment reliability and availability are exposed to increased risk in both regions 2 and 3. Fig. 2(b) shows the AFC for a 2U-New Generation (NG) server at maximum fan speed. In normal operation the server operates at 20% of the maximum speed. This means that the critical pressure is 12 Pa only during normal operation, following the affinity laws [7]. Similarly, the airflow demand during normal operation of this server is  $\sim 0.014$  m³/s (30 CFM). The point of emphasis here is that at certain events in the data center the IT equipment airflow demand might increase by 2-3 times.

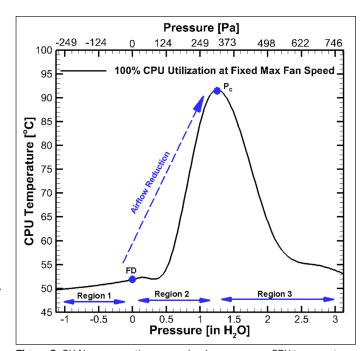
In short, the AFC testing process<sup>[3]</sup> is based on attaching operating servers at controlled fan speed to the flow bench and creating different imbalances that covers the three regions of airflow. The procedure was applied to five different IT chassis that cover the airflow spectrum in the data center. Note that the fans are operated at maximum RPM, but curves at lower RPM can be derived from affinity laws. Table 1 displays the main characteristic of each air system<sup>[3]</sup>. A 1U TOR (top of rack) switch represents the low end of the airflow spectrum (i.e. weak air system). The critical pressure is at 25 Pa (0.10 in. H<sub>2</sub>O) and the free delivery is 0.014 m<sup>3</sup>/s (31.17 CFM). A 9U BladeCenter has a free delivery airflow of 0.466m<sup>3</sup>/s (987.42 CFM) and the critical pressure is 1048 Pa (4.21 in. H<sup>2</sup>O). It is clear that the BladeCenter has the strongest air system when compared with all other IT equipment characterized. The importance of Table 1 is that it shows that during an airflow shortage event, the different pieces of IT equipment react differently, based on the relative strength of their air moving system. This indicates that some will fail or overheat before others do.

## TABLE 1 IT AIR SYSTEM CHARACTERISTICS

IT	FD (m <sup>3</sup> /s	) [CFM]	$P_{C}$ (Pa)	[in. H <sub>2</sub> O]
1U Switch	0.014	[31.17]	25	[0.10]
1U Server	0.034	[72.74]	326	[1.31]
2U Server	0.046	[98.97]	176	[0.71]
2U Server NG	0.066	[140.21]	271	[1.09]
9U BladeCenter	0.466	[987.42]	1048	[4.21]

#### **IMPACTS ON PROCESSING AND STORAGE COMPONENTS**

A. Impact on CPU: A 2U compute server was connected through a Linux interface where the CPU utilization and the fans' RPM were controlled while mounted on the flow bench. The AFC (Active Flow Curve) experimental procedure was implemented at maximum fan speed and 100% CPU utilization. As the backpressure was varied, steady state temperature readings were taken for the CPU, as shown in Fig. 3. The testing started at region 1 where

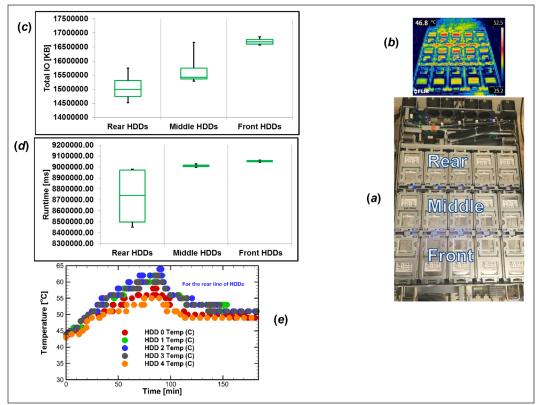


**Figure 3.** 2U New generation server backpressure vs. CPU temperature.

the server was over-provisioned with airflow higher than its design airflow rate. As aiding to air flow is reduced and the pressure values move from negative to zero at which the flow rate is at free delivery (FD). A very subtle increase in the CPU temperature is noted (50-52 °C). Increasing the backpressure further leads to flow region 2 in which CPU temperature starts to increase significantly since the airflow is lower than designed although inlet temperature is maintained at 20 °C, so concerns with IT reliability begin upon entering region 2. The backpressure is increased furthermore to reach  $P_C$ . At this point the CPU temperature reaches the maximum value since airflow is near zero through the server. Therefore, heat transfer via forced convection is minimized and the package is primarily relying on conduction, an inefficient heat removal mechanism. At that point the CPU has started to drop in voltage and frequency to reduce the heat flux, resulting in a loss of computational performance. Finally, as the flow curve moves into region 3, reverse airflow takes place. The system cools again due to forced convection. However, in a real-life case (not wind tunnel test) the rear of the server is in a hot aisle environment that is usually maintained at a high temperature to gain efficiency. This hot air will recirculate back into the contained aisle and cause issues for the surrounding IT equipment.

It is important to note that for acoustics and energy budget reasons, IT equipment usually operate at the low end of their air system's capacity. This implies that much lower external impedances are sufficient to cause problems.

B. Impact on Hard Disk Drives: To understand the effect of subtler airflow mismatches that can happen during



**Figure 4.** (a) Internal layout of a high density open compute storage server. (b) IR image of the HDD surfaces. (c) Distribution of the total IO for the rear, middle and front HDDs. (d) Distribution of the runtime for the rear, middle and front HDDs. (e) temperature profile of the rear five HDDs during test (SMART).

normal operation, a back pressure of ~30 Pa (equal to the critical pressure) is applied to an open compute high density storage unit<sup>[5]</sup>. This is a longer duration transient test during which the response of the storage system is observed under a read/write job condition. In this test, no fan speed constraints were applied. This allows for observing the actual response of the hardware fans' algorithm. The test starts while the chassis is operating at its free delivery airflow with zero external impedance. Then a back pressure perturbation is introduced for ~70 minutes after that the system is relived. During this period the HDDs (Hard Disk Drives) heat up as shown in the thermal image. The FCS (fan control system) responds to that by increasing the fans' speed. After that, the external impedance is removed, the unit is allowed to recover and the RPM gradually drops to initial value. The storage unit has three rows of HDDs—front, middle, and rear—as shown in Fig. 4(a). Fig. 4(b) shows an IR image of these components during operation. It can be seen that the rear HDDs can get thermally shadowed by the heat generated by the upstream components.

Bandwidth and IO are correlated to the thermal performance. The total IO is shown in Fig. 4(c) for the HDDs. It can be deduced that the rear HDDs, which are towards the back of the drawer, are generally observed

to have a lower total IO due to thermal preheating by the upstream HDDs and components. The total IO reduction will accumulate to yield bigger differences over longer time intervals. The runtime displays the time interval during which the HDDs are performing a read or write command/request. When the HDDs start to overheat they also start to throttle (processing speed slows down as temperature increases) requests to write or read which explains the reduction in the runtime of the rear thermally shadowed HDDs as shown in Fig. 4(d). The correlation between the data transfer and thermal performance can be further understood by looking at Fig. 4(e) where the temperatures are reported for the five HDDs at the rear during the test. This increase in temperature is a result of

the airflow imbalance that ultimately affects the IO and runtime.

### IMPLICATIONS ON MONITORING AND CONTROL

The cooling control scheme of the recent data center can be based on infrastructural temperature monitoring points at the IT inlets or, alternatively, at locations specified for the IT analytics Intelligent Platform Management Interface (IPMI) data. These locations include ones within the equipment but near the air inlet. Usually, the IPMI inlet sensor reads a couple of degrees higher than the infrastructural sensors due to preheating from components inside the chassis. However the inconsistency rapidly grows between both measuring systems during airflow imbalances such as those experienced in containment. Fig. 5 shows measurements taken for three servers in a mid-aisle rack during a blower failure experiment that starts at t=24 minutes in a CAC environment<sup>[6]</sup>. During such a scenario the IPMI data is significantly affected by the servers' internal heating. On the other hand, the infrastructural sensors are only reporting on the ambient air temperature. It would take ~ 35 minutes for the first server to hit 34 °C using Infrastructural sensors but only 9 minutes based on the IPMI reading. This happens because the IPMI sensors are closer to the hardware and are more affected by hardware temperature increase resulting from airflow reduction.

#### **CONCLUDING REMARKS**

This article discussed the interaction between the data center and the IT when air containment is deployed. It was shown that it is vital for the data center safe operation to be aware of the dynamic airflow response of the IT and their interaction with the data center. As we are steadily moving towards the cloud data center, a chip to facility thinking is important. Based on the discussions above, the following can be suggested to reduce risk of airflow imbalances:

- 1- Always utilize pressure controlled cooling units—not only inlet temperature-based—to control the contained data center cooling.
- 2- Utilize pressure relief mechanisms such as automatically opened doors during power outages in containment.
- 3- Design the cooling system (CRAH, CRAC, Fans wall...) to be able to deliver the maximum airflow demand of IT. This will be of even greater importance when the containment is used in a free cooling scheme.
- 4-Consider the impact of the air system differences between the IT stacked in containment.
- 5-Utilize the difference between IPMI and Infrastructural sensors as an early alarm of overheating.
- 6-Possible airflow mismatches in containment (due to failures, virtualization and varying loads...) require further availability and reliability guidelines to be incorporated with the current ASHRAE best practices (e.g. a server is specified for A2 temperature range within X range of back pressure/external impedance).

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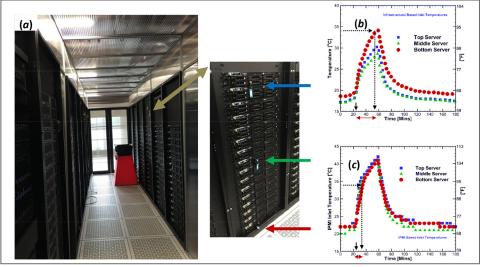


Figure 5. (a) Rack, external sensors and servers designation (b) Infrastructural inlet sensors (c) IPMI inlet sensors

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#### **NOMENCLATURE**

AFC	Active Flow Curve
CAC	Cold Aisle Containment
CPU	Central Processing Unit

 $CRAC \quad \ Computer\ Room\ Air\ Conditioner\ - Direct\ Expansion-.$ 

CRAH Computer Room Air Handler - Chiller-

FD Free Delivery (Design) airflow, [m<sup>3</sup>/s or CFM]

HAC Hot Aisle Containment

HDD Hard Disk Drive IO Input/output

IT Information Technology

IPMI Intelligent Platform Management Interface

NG New Generation server

P<sub>C</sub> Critical Backpressure, [Pa or in. H<sub>2</sub>O]

SMART Data from a hard drive or solid state drive's self-

monitoring capability

TOR Top of Rack

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### Pluggable Optics Modules - Thermal Specifications, Part 1

Bonnie Mack and Terence Graham Ciena Corporation

#### 1. INTRODUCTION

LUGGABLE OPTICS MODULES, (POMS), SUCH as SFP, QSFP, QSFP+, QSFP28, CFP, CFP2, and CFP4 transceivers, are optical interface devices that are connected to a PCB through ports in the faceplate. A brief description of these modules is given in Table 1. Initially conceived as low power devices, the module power density has increased along with demand for higher bandwidth. Consequently, it is progressively more difficult to cool these modules. The modules are hot-pluggable and the faceplate port utilizes a PCB-mounted cage. These cages are folded sheet metal enclosures that press fit into the PCB and provide connector alignment and electromagnetic compatibility (EMC) features as shown in Figure 1. The cages generally prevent heatsinking to the module bottom but provide an opening in the top surface where a spring-loaded riding heatsink can contact the lid. The challenge is to permit the required sliding while providing a low interface thermal resistance.

POMs are designed to support various communication standards. Multi-Source Agreements (MSAs) specify physical form factor and electrical interfaces. These agreements allow multiple manufacturers to make physically compatible products to promote competition, interoperability and multiple sources for systems vendors and end users. These MSAs become de facto standards. They also define power classes for POMs that are based on the supplied power and correspond to different

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internal processing levels and optical signal reach. POM data rates range from ~1 Gb/s to 100 Gb/s with a number of data rates available in each form factor. References [1] and [2] give physical dimensions of various form factors.

MSAs define the geometry of these optical modules, but parameters affecting the interface between a pluggable module and its heatsink have not been sufficiently well-defined or controlled. Some MSAs specify allowable contact forces, some do not. The surface finish and flatness of the module-heatsink contact area were recognized as requiring control, but limits were primarily set for low cost manufacturing methods and aesthetics. Initially some MSAs defined heatsinks, but due to the uniqueness of each system environment, system designers usually customized the designs. Increased module dissipation and functionality made it obvious that better thermal specifications were required.

This was recognized by the Optical Internetworking Forum, OIF, [3] who developed an Implementation Agreement (IA) [1] to specify general requirements for the thermal interface. The IA specifies that the MSAs [6, 8, 9] and [10] define the location and size of the contact areas where the majority of heat would be removed from high power modules and directly addresses the issue of removing heat from the top of the POMs. The IA defines resistance parameters of the interface between module and heatsink and specifies relevant information. It specifies the information POM suppliers

Form Factor	Description	Nominal Optical Output	Thermal Output (W)	Dimensions L x W x H (mm)
SFP SFP+	Small Form-Factor Pluggable	1 Gb/s 10 GB/s	0.5 - 1.0 $1.0 - 2.0$	56.5 x 13.4 x 8.5
XFP	10 Gigabit Small Form-Factor Pluggable	1x10 Gb/s	1.5 - 3.5	78 x 18.35 x 8.5
QSFP QSFP+ QSFP28	Quad Small Form-Factor Pluggable	4 x 2.5 Gb/s 4 x 10 Gg/s 4 x 28 Gb/s	1.0 - 2.5 $1.5 - 3.5$ $2.5 - 4.5$	72.4 x 18.35 x 8.5
CFP	Centum Form-Factor Pluggable	4 x 28 Gb/s, 10 x 10 Gb/s	8.0 - 32.0	144.75 x 75 x 13.6
CFP2	$\sim$ ½ size of CFP to double port density.	4 x 28 Gb/s, 10 x 10 Gb/s	3.0 – 15.0	107.5 x 41.5 x 12.4
CFP4	~¼ size of CFP to quadruple port density	4 x 10 Gb/s, 4 x 28 Gb/s, 10 x 10 Gb/s	1.5 – 6.0	88 x 21.7 x 9.5

Table 1: Selected Pluggable Optical Module Form Factors

must provide to facilitate thermal integration of the module within the host system for both the initial assessment and detailed design stages. These include specifications for temperature drop and thermal resistance between the module and an "ideal" heatsink. It defines a thermal interface resistance that includes interface contact and spreading effects. The IA recommends tighter tolerances for surface finish and flatness for well controlled interfaces. It defines power density classes for the thermal interface and describes a method for measuring the thermal interface resistance between the module and a cold plate with an "ideal" mating surface. In part 2 of the paper its appropriateness for the calibration of internal sensors used for module thermal alarms is discussed.

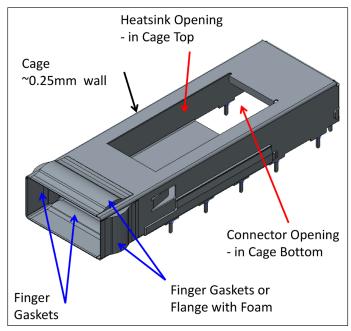
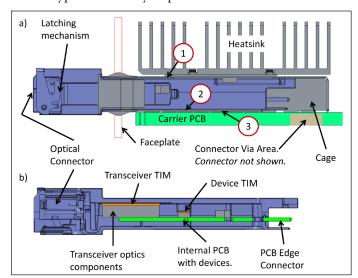


Figure 1: QSFP cage design - features are typical of most form factors

#### 2. THE THERMAL ENVIRONMENT

Pluggable optics modules combine fibre optic transmitters and receivers (transceivers) and some signal processing into one package. The transmitter side converts an electrical signal into light for transmission over optical fibre while the receiver section converts the light signal into an electrical signal. The modules plug into connectors on the host board for additional signal processing, switching etc. For all but CFPs, the modules are housed in a cage which guides the modules to the connectors and contains EMC solutions for the faceplate ports. The larger CFP modules use guide rails for alignment and have separate faceplate EMC features. The modules extend through the faceplate, and can be hot swapped. Figures 1 and 2 show typical thermally-important features of POMs.



**Figure 2: a)** QSFP in cage section at inside edge of cage, **b)** QSFP section showing typical internal layout. Narrow air gaps locations: 1) Module to top of cage, 2) Module to bottom of cage, 3) Bottom of cage to PCB, and not shown 4) sides of module to sides of cage.

The air gaps,  $\sim 0.2$ mm to 0.3mm nominal, between the module case and the cage, and between the cage and PCB provide an inconsistent thermal resistance because the tolerances and misalignments associated with manufacture and assembly are significant relative to the gaps. This precludes design using conduction to the PCB as a reliable method of cooling. In comparison, the electrical connection to the host PCB provides a well-defined thermal connection that can transfer heat into the module from neighbouring heat sources, or out to the PCB if it is relatively cool.

Figure 3 depicts the ways that heat is transferred

between the module and the system. The relative merits of side-to-side or front-to back airflow are discussed in <sup>[2]</sup> where system and heatsink strategies for POM cooling are examined. A smaller amount of heat naturally convects from the module to the environment outside the faceplate. The thermal designer may have some influence on layout to prevent heating of the PCB near the connector. As noted in <sup>[2]</sup>, in side-to-side air flow, cooling air arriving at the module and its heatsink is often much hotter than ambient, particularly for downstream modules in a densely filled faceplate.

For low power POMs on a cool PCB, a cage perforated with holes and conduction to PCB through the connector may be adequate for cooling. In this paper we are dealing with cases that require a heatsink. As illustrated in <sup>[2]</sup>, there are several aspects to the heatsink design: the fin side, the base spreading, and the contact resistance between the module and the heatsink. The last two of these requires input and co-ordination between the system designers and the module suppliers/designers and is the focus of <sup>[1]</sup>.

### 3. FLATNESS AND MODULE LAYOUT STUDIES ON CFP2

The initial work done in support of IA# OIF-Thermal-01.0 IA included a study of the thermal interface resistance between a CFP2 lid and heatsink base including heat spreading effects. The study examined three contact scenarios: 1) a transverse bump in the center of the lid, 2) a transverse hollow in the center of the lid and 3) a transverse contact in the center and ends of the lid. The stylized net-flatness-shapes of the three scenarios were used to bound the problem and are based on the authors' module and heatsink surface measurements. All three scenarios were defined to have the same contact area. These simplified contact geometries are depicted in Figure 4 and

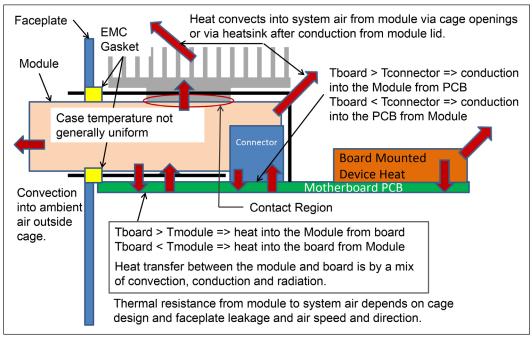


Figure 3: Typical Module Thermal Environment – Side View

the contact gap ranges from what would be an extremely fine production surface flatness to where both surfaces are out-of-flat by the maximum allowed by the MSA for the CFP2 contact surface. It was assumed for the study that both surfaces had the same type of out-of flatness so that modelling of the net gap between surfaces was easily implemented in the commercial CFD software<sup>[4]</sup> used for the analysis.

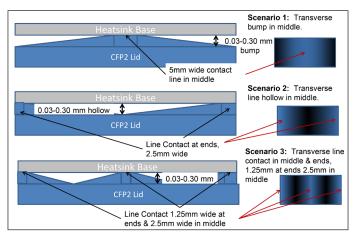


Figure 4: CFP2 Contact Interface Flatness Scenarios.

The resistance in the contact areas between the heatsink and the module was modelled using the method described by Yovanovich et al.<sup>[4]</sup>. Where Joint Resistance

$$h_j = h_{contact} + h_{gap}$$

Reference 10 provides details for determination of  $h_{contact}$  and  $h_{gap}$  using properties of T6063 Aluminum for both case and heatsink.

Giving, for max out-of-flatness:

$$h_j$$
 = 589 + 3328 = 3917 [W /  $m^2$  K]  
 $r_i$  = 1 /  $h_i$  = 2.55 [cm<sup>2</sup> K / W]

For comparison, a completely flat interface area with lapped surface finish gives:

$$r_j = 0.4 \text{ [cm}^2 \text{ K / W]} \Rightarrow R_j = 0.015 \text{ [K/W]}$$

The simplified CFP2 thermal model layout is shown in Figure 5. Internally, the CFP2 has up to 6 devices that can be set to dissipate power and to contact the lid. Results were obtained for varying gaps due to out-of-flatness and different source locations. Intake air is 55°C at 1m/s across the enclosure cross-section upstream of the module. Total power for the CFP2 is 12W in all cases. Other model details are given in<sup>[11]</sup>. CFP2 lid temperature is monitored directly above the centre of each of devices A – F.

#### Defining:

$$\begin{split} &T_{\text{Lid max}} = \text{maximum lid temperature} \\ &T_{\text{HS ave}} = \text{average heatsink pad temperature} \\ &dT_{\text{Lid}} = \text{temperature difference among lid locations A} - F \\ &dT_{\text{Lid max to HS ave}} = T_{\text{Lid max}'} - T_{\text{HS ave}} \end{split}$$

These are plotted in Figures 6 and 7 versus net flatness over the range of 0.03 mm to 0.3 mm flatness, for scenarios 1, 2, and 3.

Results are shown in Figure 6 with contact per Figure 4 and 3 W heat dissipation applied to devices A and B and 6 W to the rear PCB location per Figure 5. Note that the MSA maximum for the CFP2 alone is 0.15 mm flatness. The

maximum CFP2 lid temperature varies by more than 6.5°C at a total interface flatness of 0.15 mm. The temperature drop between the lid and the average heatsink base temperature is also 6.5°C for this same flatness. This is almost ½ of the 15°C available with 70°C max case CFP2 at an upstream location for a shelf-level Telcordia telecommunications environmental short-term condition<sup>[7]</sup>.

Per Figure 7, when the PCB heat is set to 0W, and heat is applied to both the front and back devices, A, B, E, and F and they are all connected to the lid, the temperature above A and B remains hottest but is ~2.3°C lower than with only A and B connected to the lid. Additionally shown in [11], moving the heated devices from the front locations, A & B, to the back locations, E & F, and the PCB heat to the front from the rear reduces the maximum case temperature by ~7°C. Taken together, these results show that the lowest lid temperatures result when heatsink contact is closest to dissipating devices thermally connected to the lid.

Figure 6 and 7 results show that for flatness variations where surfaces are in close compliance at 0.03 mm net gap to the maximum allowed by the MSA at 0.3 mm (0.15 mm on both the CFP2 lid contact area, and the heatsink contact area)  $T_{\rm Lid\,max}$  can vary by ~5.5 °C to ~8 °C depending on the flatness scenario and the location of heat dissipation and its connection to the lid. Additionally they show that  $dT_{\rm Lid}$  changes very little after the maximum net gap exceeds 0.15 mm. Below that, the difference reduces with net gap indicating that the spreading in the heatsink base provides some effect. Finally,  $dT_{\rm Lid\,max\,to\,HS\,ave}$  is strongly dependent on the net interface flatness with the value at 0.3 mm being approximately twice that at 0.03 mm net flatness. For the source locations modelled, the centre hollow has the lowest difference between the maximum lid

temperature and heatsink base average temperature.

#### 4. SUMMARY

Thermal interface resistance of a pluggable optics module is affected by design factors under the control of both the system designer and the module designer. In particular, surface finish and flatness have a strong influence within normally accepted manufacturing and machining practices.

Part 2 of this paper will examine the effects of increasing the thermal conductivity of the case as well as the effects of host PCB heat sources. It will also look at how to calibrate POM internal sensors.

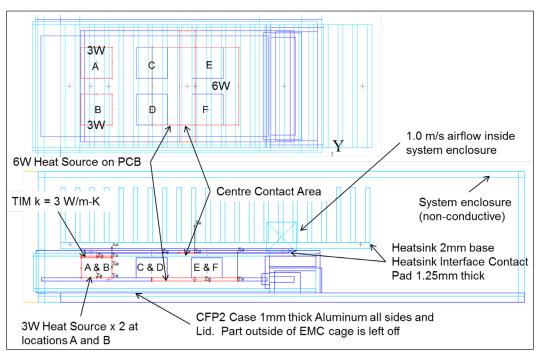


Figure 5: CFP2 flatness model layout showing front device, rear CFP2 PCB heat and central contact location

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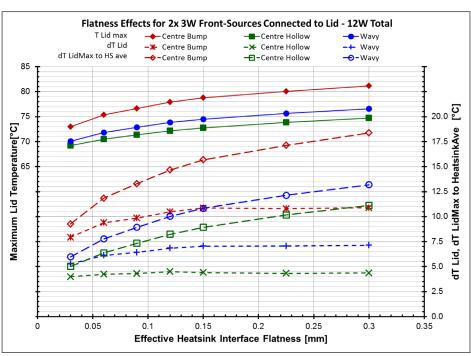


Figure 6: Range of flatness results with front device, and rear PCB heat dissipation.

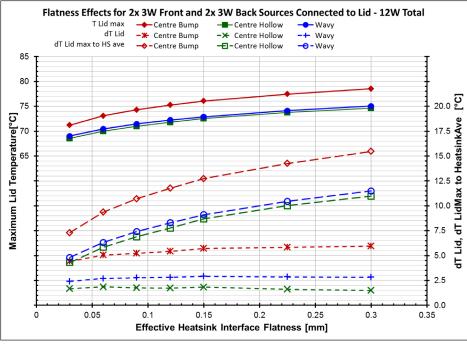


Figure 7: Range of flatness results with heat dissipation on front and rear devices with OW PCB dissipation.

## Application of Phase Change Materials in Handheld Computing Devices

**Electronics Cooling Solutions Inc. (ECS)** 

#### 1. INTRODUCTION

**TITH PEAK LOADS OFTEN IN** the order of minutes and ergonomic considerations limiting surface temperatures and acoustical noise, handheld devices, such as smart phones or tablets, are excellent candidates for use of phase change materials (PCMs).

Processor loads in handheld products are highly variable. There are many situations where temporary power in system on a chip (SoC) packages can increase due to multiple functionality; for example, social media activity while listening to music, or a short phone call while playing games.

Additionally, handheld consumer products are subject to many ergonomic constraints as a result of their proximity to and direct contact with the user. Surface temperatures must be kept within a comfortable and safe range. If fans are used acoustic noise must be kept below acceptable limits. There are many additional

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physical constraints on size and weight that restrict the product's ability to dissipate heat and restrict cooling options. Few existing electronic products are designed specifically for transient thermal loads. In order to manage high temperatures and thermal loads, most rely on throttling and/or added mass to increase thermal capacitance of the materials used in construction.

The design of handheld products with PCMs can extend product working operating range, minimize throttling, and reduce reliance on fans for transient load use cases to reduce acoustic noise and extend battery life. For these reasons, consumer devices are excellent candidates for the introduction of phase change materials. This study looks at opportunities and challenges for applying PCMs to handheld and computing devices using a forced convection tablet as an example.

A typical temperature-time heating profile of a PCM under a thermal load, (Figure 1) exhibits linear sensible heating initially, and then undergoes phase transition at a particular melt temperature. During the phase transition heat energy is absorbed by the material while it maintains a constant temperature. Once the phase change is complete, the material continues sensible heating.

PCMs have been extensively studied [1,2] and have long been used by industry. The HVAC (heating, ventilating, and airconditioning) industry, for example, has used PCMs for thermal energy storage. PCM materials have flexibility with respect to their composition and melt temperatures and can be customized to target specific operating temperatures. They have minimal reliability concerns and can be repeatedly cycled without degrading.

Paraffin based PCMs are well suited to electronics applications because they have a high heat of fusion and transition temperatures typically in the range of

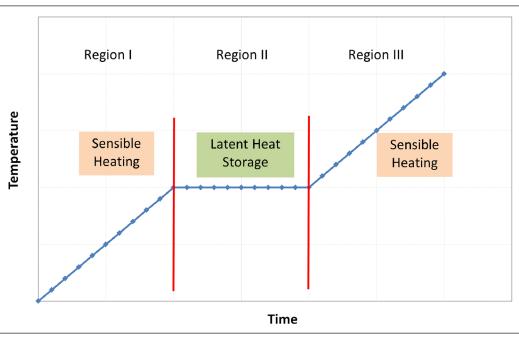


Figure 1: Typical PCM heating curve

5-70°C. The material used for this study was a commercially-available composite of paraffin gel material infused into a graphite foam matrix, whose properties are presented in Table  $1^{[3]}$ . These properties are "effective" ones, in that they represent the combined effect of the graphite matrix and the paraffin gel." The graphite matrix provides stability for the material and improves its thermal conductivity. The phase change temperature can also be formulated to a range of temperatures.

Material	PCM
Type	Paraffin / Graphite Composite
Phase Transition Temperature	42 – 45 C
Latent Heat of Fusion	180 kJ/kg
Thermal Conductivity	1.2 W/mK
Specific Gravity	0.8 g/cm <sup>3</sup>

**Table 1:** PCM thermophysical properties of PCM material used in study [3]

#### 2. MATERIAL PERFORMANCE AND MODEL VERIFICATION.

A simple exploratory experiment was performed with the PCM before applying it to a more complex forced convection tablet environment in order to characterize its behavior and to validate the computational method to be used for the study. The experimental apparatus included a heatsink, a 10 W heat source, 9.5 g of PCM material, and thermocouples placed at various points on both sides of the PCM.

For this study a commercial computational fluid dynamics (CFD) software<sup>[4]</sup> was used to predict the thermal response of the PCM and test assembly under analysis. The software does not currently allow for the direct simulation of the change in phase of the PCM, so for this analysis the heat of fusion was added to the specific heat versus temperature parameter for the PCM material within the software. This results in an 'equivalent specific heat' that incorporates the latent heat storage of the material as a discrete peak in the temperature varying specific heat parameter.

$$c_{equiv} = c_p + \frac{h}{\delta T}$$

In this case the heat of fusion for the PCM material was distributed over a 3°C temperature range from 42 to 45°C.

The computational and experimental results are compared in Figure 2, and for the heatsink base temperature are seen to agree within 5°C. The only adjustment required to the computational model to achieve a match to the experimental results was to introduce a contact resistance of  $0.02 \text{Cm}^2/\text{W}$  between the heatsink and PCM. This identified surface contact resistance as an important concern in the implementation of PCMs of this type within handheld devices which must be addressed in the design process.

Sensitivity studies were also run where the time step and mesh density were varied and found to show no significant variation in the resulting transient curves, demonstrating that the solution was computationally grid independent.

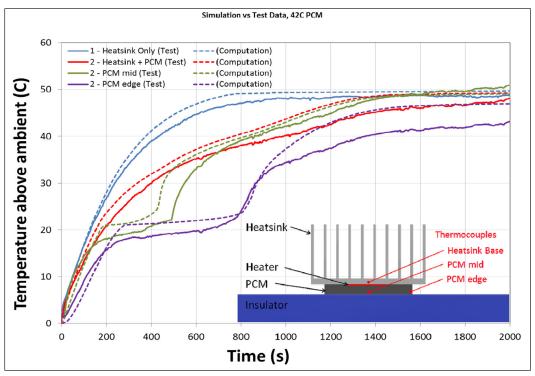


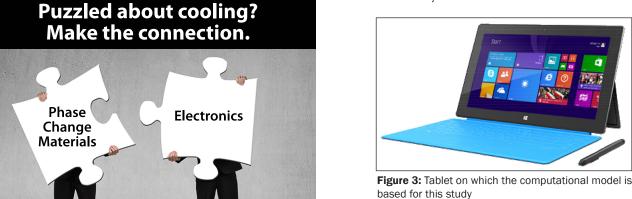
Figure 2: Experimental (solid) versus computational (dashed) results for the test assembly (inset)

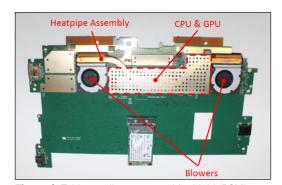
The results in Figure 2 show that the time period for the system to reach a temperature of approximately 40°C with the addition of the PCM is almost twice that of the system without the PCM. This delay, in the order of 400 seconds or 7 minutes, may be useful in systems with transient loads that occur within that time period.

## 3. SIMULATED APPLICATION OF PCM IN A FORCED CONVECTION TABLET

For the main portion of this study the application of PCM material to a popular forced convection tablet, shown in Figure 3, was considered. Previous analyses of this tablet [5,6] generated a

detailed and well calibrated computational model which is used for this study.





**Figure 4:** Tablet cooling system with shield (PCM) area highlighted (red dashed line)

The central processing unit (CPU) and graphics processing unit GPU are the main heat generating components in the tablet. They are mounted adjacent to each other and thermally coupled to a copper heat spreader and dual heat pipe assembly. The condenser ends of the heat pipe are cooled by two small blowers. The heat pipe and blower assembly can be seen toward the top of the image in Figure 4, with the CPU and GPU sitting below

the shield approximately midway between the blowers.

While there is little space available within the tablet for the addition of PCM materials. the shield that sits over the CPU and heat pipe region encloses a volume of approximately 15 cm³, which is ideally situated for the application of the PCM in the vicinity of the main heat sources.

Attempts to evaluate the PCM experimentally within the tablet were unsuccessful due to the difficulty in maintaining pressure contact between the PCM and heat pipe. The following results are based on the simulated inclusion of approximately 11.8 g of the PCM material placed over the CPU and beneath the shield. The transient heating response of the CPU heat spreader is examined for a 10 W power step. Using the PCM material properties from Table 1 as a baseline, various PCM parameters were varied in order to examine their effects on the transient heating within the tablet environment.

#### **PHASE CHANGE TEMPERATURE**

Phase change temperature is a primary consideration in the selection of PCMs. Figure 5 shows the predicted transient system response curves for PCM with phase transition temperatures ranging from 32 to 47°C.

The value of most interest in implementing a PCM solution is the time delay,

or increase in the time required for a given temperature to be reached. Figure 6 displays the time delay achieved at four values of critical design temperature (32, 37, 42, and 47°C) for a given PCM melt temperature. For example, at critical design temperature of 50°C, a time delay in excess of 10 minutes is only achieved with a 37°C melt temperature PCM. In order to select the appropriate PCM properties, a good understanding

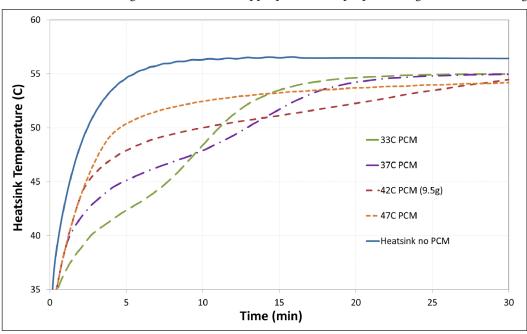


Figure 5: Predicted transient response to varying PCM transition temperature with 11.8 g of PCM material (except where noted) in simulated tablet environment

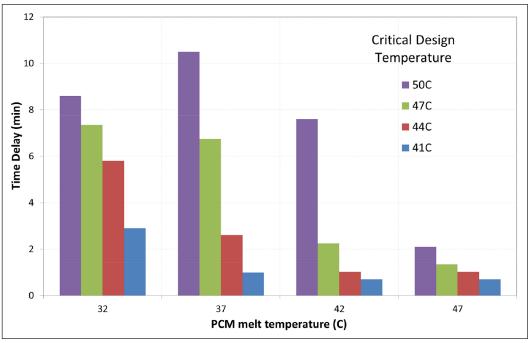


Figure 6: Predicted transient heating time delay at stated values of critical design temperature, resulting from varying PCM transition temperature

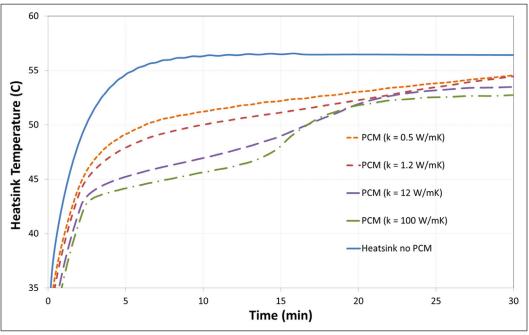


Figure 7: Predicted transient response to varying PCM thermal conductivity

of the system performance and application environments/ conditions is required to determine the appropriate critical design temperature for the system.

### 5. PCM THERMAL CONDUCTIVITY

Most PCMs that have transition temperatures and properties suitable for use in electronics thermal management have very poor thermal conductivities. That is the case for paraffin-based PCMs, for which thermal conductivity is normally in the range of 0.1-0.3 W/m-K <sup>[7,8]</sup>. Due to their low conductivity, heat spreads slowly through the material and the absorption of energy through phase change occurs gradually.

Simulation results in Figure 7 illustrate how improved conductivity can significantly increase the heating time delay experienced by the system and cause the phase transition

step to be much more defined. The higher conductivities modeled in these scenarios cannot be achieved with existing materials. Instead, the low conductivity of the materials must



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be compensated for in the design by the addition of elements such as graphite or metal spreaders to distribute the heat over the PCM.

Figure 8 further illustrates the effects of spreading on the PCM over the heatpipe and blower assembly. The high temperature gradients in the 1.2 W/m-K PCM material make the outline of the heatpipe assembly clearly visible and the addition of spreaders is recommended in order to better distribute heat through the PCM in this case.

### 6. HEAT CAPACITY / VOLUME OF PCM

The specific and latent heat

capacity of the materials is another important parameter, as it dictates how much heat can be stored and therefore the time delay that can be achieved in system heating. To achieve a required time delay, a high heat of fusion is desired to minimize material volume.

While the volume of PCM required to achieve a given time delay can initially be estimated based on balancing mass and heat of fusion against power dissipation and time, the results in Figures 7 and 9 show that factors such as conductivity and transition temperature will also have a significant effect on the time delay and the volume required must be assessed by accounting for all of these details and the specific environment.

#### 7. CONCLUSIONS

For consumer devices, such as phones and tablets, there are many potential advantages to the use of PCMs. In operating conditions involving short term peak loads, they can be used to limit component and hot spot temperatures and can reduce the need for reliance on measures such as fans running at full speed, or throttling of component power. The results of this study indicate that a time delay of 7 to 10 minutes might be achieved for a power dissipation of 10 W if appropriately integrated into the tablet environment. This may be enough to absorb short term peaks in power without the need for throttling or fan speed increases.

There are, however, some disadvantages and difficulties to the implementation of PCMs in hand held devices. The PCM adds weight and complexity to the design, and due to the low thermal conductivity of most PCMs additional spreaders may be required. Contact resistances can be high and the materials must be retained effectively while still allowing for expansion and contraction during changes of phase.

The use of PCMs requires careful design to compensate for these shortcomings and to optimize their performance; never-the-less for suitable applications they can provide a useful means for transient thermal management in handheld devices.

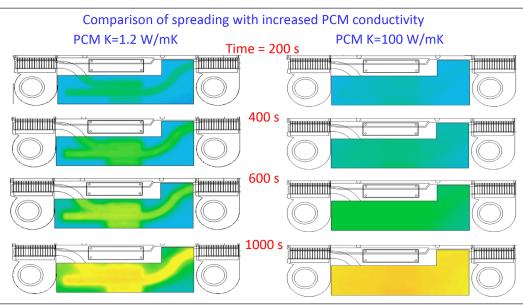


Figure 8: Comparison of spreading through PCM in heatpipe / blower assembly, with increased conductivity.

#### **ACKNOWLEDGMENTS**

The authors would like to thank the following for their assistance:

- Outlast Technologies for providing the PCM samples used for the study.
- Mentor Graphics for providing a *Flotherm XT* advanced license with transient analysis capabilities.

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