ElectronicsCooling

Volume 16, Number 3
Fall 2010

CREATING PCB THERMAL CONDUCTIVITY MAPS USING IMAGE PROCESSING

EVALUATION OF COOLING SOLUTIONS FOR OUTDOOR ELECTRONICS

TRANSIENT DUAL INTERFACE MEASUREMENT OF THE RTH-JC OF POWER SEMICONDUCTOR PACKAGES

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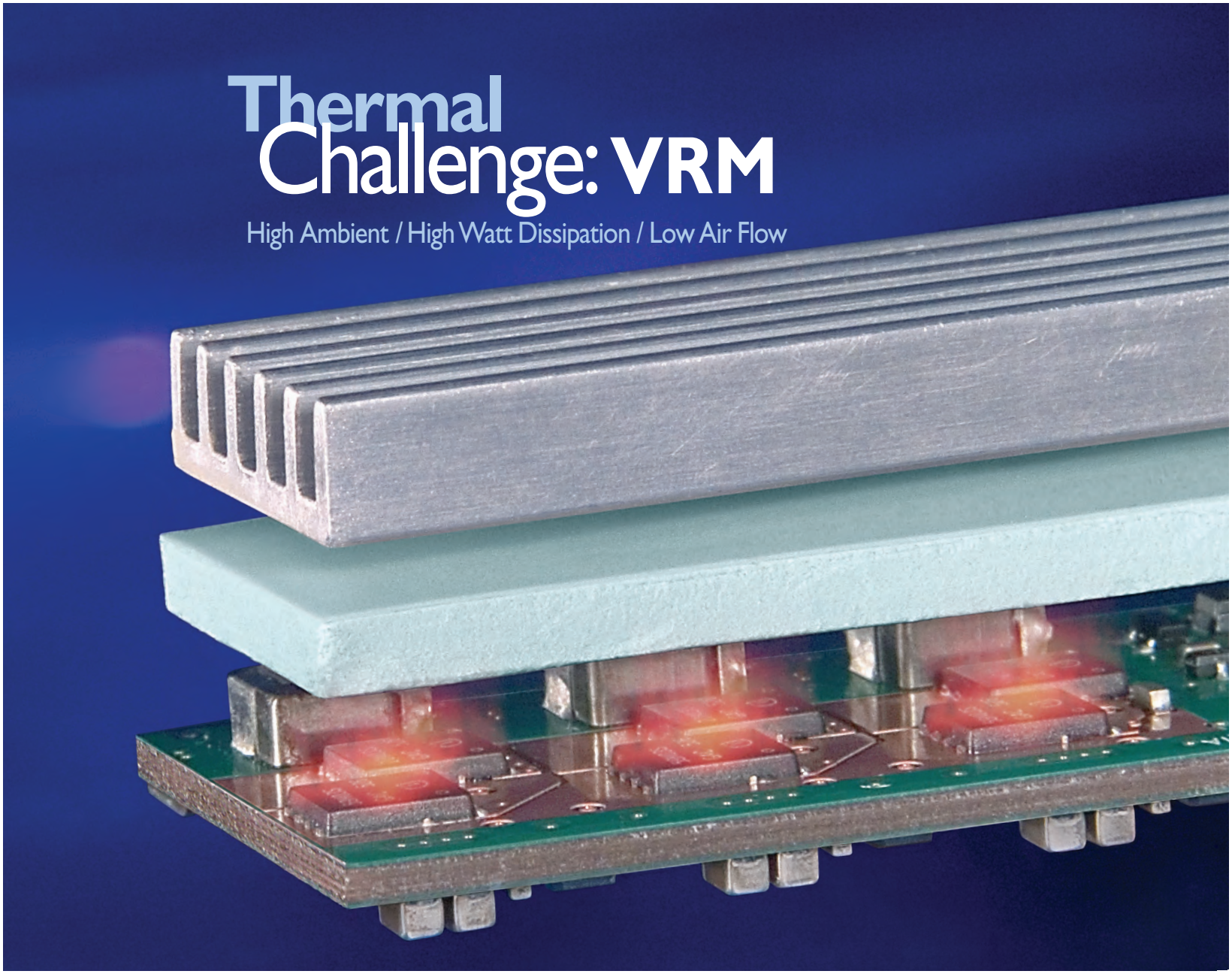
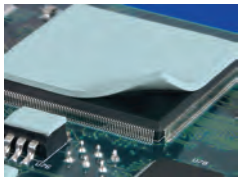
Thermal Challenge: VRM

High Ambient / High Watt Dissipation / Low Air Flow



Solution: New Bergquist S-Class Gap Pad® 5000S35



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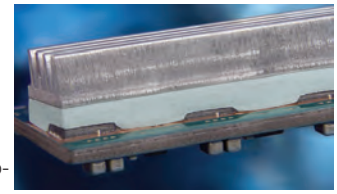

Excellent interfacing and wet-out makes GP 5000S35 ideal for fragile components with demanding contours and stack-up tolerances.

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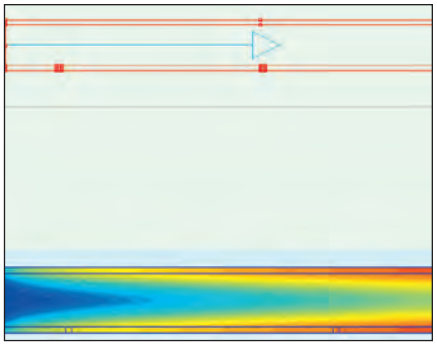

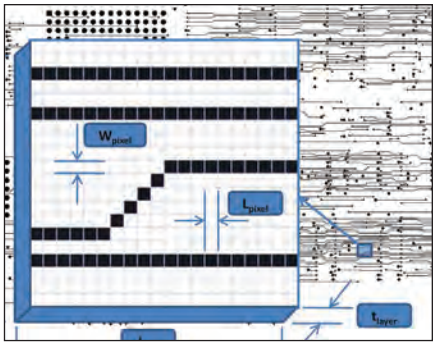

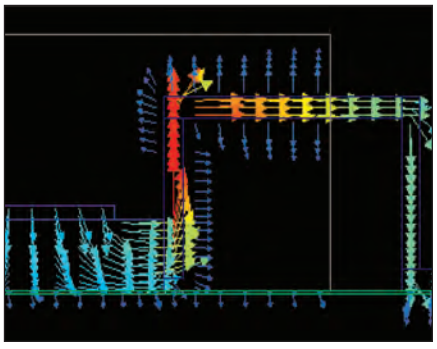

FRONT COVER
Close up of a print circuit board.
Design by Amelia McKean.

editorial

Clemens J.M. Lasance
Editor-in-Chief, Fall 2010 Issue

why standardization is mandatory: on the incorrect use of thermal impedance in the TIM world

Some time ago I devoted my editorial to the problems caused by the veeerrryyy slow adherence to the use of SI units to which the U.S. committed itself in 1872. When talking globalization we should speak the same scientific language, and when there are conflicts of interest, logical reasoning should prevail to decide upon the best solution, and when this turns out to be difficult some standardization body should produce the verdict. One example is the incorrect use of thermal impedance by some vendors to describe the thermal resistance of a Thermal Interface Material (TIM). The logical reasoning to get rid of this habit is the following,

"Thermal impedance," with unit m2K/W is not the right word to indicate unit area thermal resistance, because it violates the electrothermal analogy commonly in use. First, the term is historically reserved to describe time-dependent thermal resistance with unit K/W. In limiting cases, for frequency zero or large enough times approaching steady state, the impedance becomes equal to the resistance. Second, in the electrical world 'electrical resistance' and 'electrical impedance' have the same unit, namely Ohm. Consequently, 'thermal impedance' should have the dimension K/W, not m2K/W. But the real problem is that sticking to the current definition of "thermal impedance" will cause a lot of confusion in the future, because the use of dynamic test methods is the obvious choice for application-specific tests, one output of which is a thermal impedance. It should be added that regarding TIMs, in situ testing is the only way for a designer to achieve a value that makes sense in real life. When quoting the performance of a TIM per area, we propose to use 'unit area thermal resistance' or 'unit thermal resistance' or 'area thermal resistance'. The final word is to a standardization body.

Let us summarize the pros and cons.

Pro: The use of the word is generally accepted by some vendors and users in the TIM branch of industry.

Cons: (assumption: we agree on the usefulness of the electrothermal analogy)

- Thermal impedance (m2K/W) is not the right word to describe the output of steady state TIM testers, for reasons outlined above.
- An increasing use of dynamic test methods is expected, one output of which is a thermal impedance (K/W), leading to a lot of confusion.
- Conflict with the established use of dynamic thermal impedance (Zth) in the power device industry.

Alternatively, we could decide to refrain from using m2K/W. However, using m2K/W has its merits:, because the unit area Rth is directly comparable to the inverse of the heat transfer coefficient, or alternatively, equal to the ratio of thickness over effective thermal conductivity, a metric to compare the thermal resistance of various TIMs with different areas. As an example, take the generally accepted feeling that future TIMs should exhibit an Rth < 5 mm2K/W. Let's assume the Rth of the cooling solution should be less than 20% of the Rth of the TIM, otherwise improving the cooling would not be effective. What does this mean for heff? heff> 1.000.000 W/m2K ! (Recall that we talk effective h, including the area enlargement by a heat sink.)

How to improve upon this situation? Customers unite! Refuse to buy from steady state thermal impedance believers!

Following an example of a letter you could write:

Dear TIM vendor,

I hope you agree with your valued customer who is considered king by your sales department that your choice of continuing to use 'thermal impedance' to describe what is essentially a unit area thermal resistance, with dimensions m2K/W, is not in my interest. It leads to unacceptable confusion because thermal impedance is a historically defined parameter to describe the thermal transient response with units of K/W.

Thanks for your understanding.

ElectronicsCooling

Website: www.electronics-cooling.com

Published by
ITEM Publications
1000 Germantown Pike, F-2
Plymouth Meeting, PA 19462 USA
Phone: +1 484-688-0300
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a spreadsheet based matrix solution for a thermal resistance network: part 1

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A thermal resistance network analysis begins by defining discrete points within a system, known as nodes, and the thermal resistance between each set of nodes. Boundary conditions for external heat inputs and reference temperature(s) are applied to the appropriate nodes. Equations to relate nodal temperatures can be generated by applying an energy balance on each node in the system. This is identical to the approach used in electrical engineering to determine voltages at each point in an electrical resistance network.

One significant limitation of the thermal resistance analysis, as compared to the electrical analysis, is that there is much less difference in conductivity between thermal insulators and conductors (~4 orders of magnitude) than in their electrical counterparts (~20 orders of magnitude) [1]. Therefore, the analyst using a thermal resistance network needs to recognize that there are no perfect thermal insulators and all the nodes in a network are connected to some extent. While this can limit the precision of the approach, thermal resistance analysis can be an effective tool for understanding general behavior of a system and identifying those design factors that are most critical. This is especially true early in the design of a new system when limited knowledge of specific geometric parameters may limit the analyst's ability to create a meaningful finite element model. One may think of resistance network analysis as one method for bridging the gap between 'back of the envelope' calculations and high level finite element analysis using dedicated analysis software.

A matrix analysis is a very effective method for solving nodal temperatures in a resistance network. The mechanisms for applying the matrix method have been presented in numerous publications, including [2]. Therefore the complete mathematical derivations will not be repeated here. As indicated in [2], mathematical software packages such as MathCAD or Matlab are ideal for solving matrix equations. However, many practicing engineers do not use these programs on a regular basis (if they even have access to them) and learning the software may take more time than solving the actual problem. Moreover, if the matrix solution software is not widely used within a company, it may be difficult to share the calculation tool with colleagues.

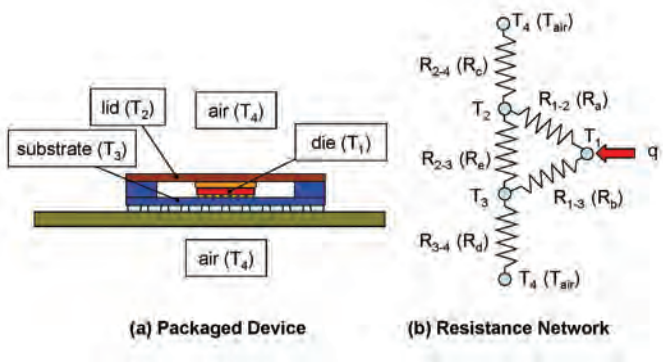

Figure 1. Simplified resistance network for packaged device.

On the other hand, the majority of engineers use a spreadsheet, such as Microsoft Excel, on a regular basis. While it is recognized that spreadsheets aren't as efficient for solving these types of problems as dedicated mathematical software, their ubiquity of use by engineers does make them very easy to share with others and to integrate the solutions into other spreadsheet based tools. This article will describe a step-by-step process for defining a thermal resistance network in Excel and using standard functions to solve for nodal temperatures in steady state heat transfer.

To illustrate the basic approach for using Excel to solve a thermal resistance network, the same problem outlined in [2] will be used. In that problem, a number of individual resistance terms were included in assessing the overall thermal characteristics of an integrated circuit package attached to a circuit board. A representation of the packaged device and the resulting simplified resistance network are shown in Figure 1. This network includes four nodes: Node 1 is the silicon die, Node 2 is the top of the package, Node 3 is the package substrate and Node 4 is the surrounding air. The resistances between the nodes are generally combinations of multiple series resistances.

In this article, the nomenclature used for each resistance indicates which two nodes it connects (i.e., R_{2-3} represents

the total thermal resistance between Node 2 and Node 3). This nomenclature differs from that used in Ref. [2]; the symbols in parentheses in Figure 1 indicate the resistance shown in Figure 2 of Ref. [2].

As described in [2], an energy balance can be applied to each node and equations that relate the node temperatures to their thermal resistances can be generated. The equations are written using values of conductances, K, which are the inverses of the thermal resistances, R ($K_{i-j} = 1/R_{i-j}$). The individual energy balance equations can be written into matrix form with the conductance matrix, [C], multiplied by the temperature vector, {T}, being equal to the boundary condition vector, {Q}, which represents the effects of dissipated power and reference temperature. Figure 2 shows this matrix equation.

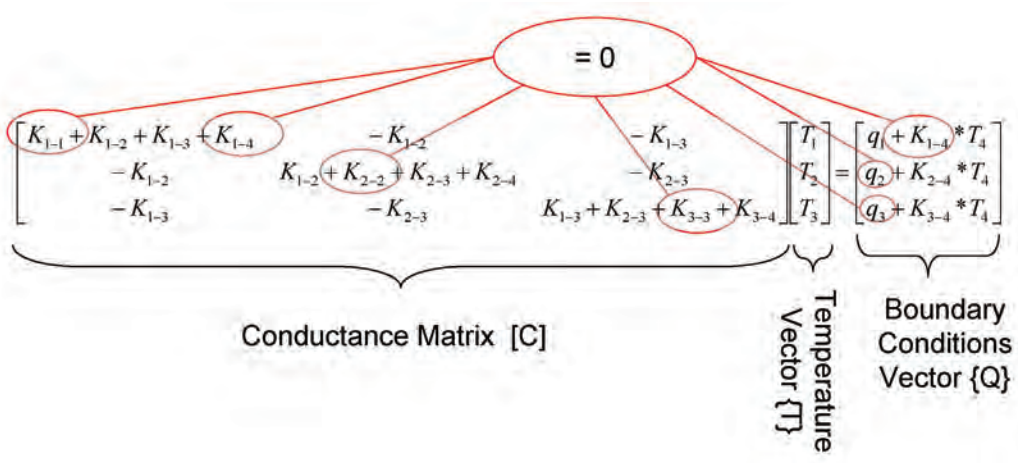

Figure 2. Matrix form of energy balance equations.

The equation in Figure 2 is identical to equation (11) in Ref. [2] except that that it includes diagonal terms (K_{1-2}, K_{2-2}, etc.) as well as K_{1-4}, q_2 and q_3. These terms were not shown in the Ref. [2] equation because they are all equal to zero for the problem being discussed. They are included in Figure 3 however to illustrate general characteristics by which the conductance matrix and boundary condition vector can be generated. These are summarized in Table 1.

To solve for the nodal temperatures, the inverse of the conductance matrix is multiplied by the boundary condition vector, i.e., $\{T\} = [C]^{-1}\{Q\}$. A spreadsheet can not only solve this matrix equation, but can also be used to efficiently set up the matrices in a logical and understandable format. Figure 3 shows a portion of a spreadsheet that was set up to solve the thermal resistance network problem described in

[2]. The figure is annotated to show what is accomplished in various regions in the spreadsheet[1], starting on the left side where resistance values and boundary conditions are defined. These individual resistances are used to generate the resistance matrix to then define the K matrix. The rules in Table 1 are then used to generate the conductance matrix, [C] and the boundary condition vector, {Q}. Once [C] and {Q} have been calculated, the spreadsheet solves for nodal temperatures using matrix operations. The following paragraphs describe the specific Excel functions used to perform these steps.

To generate the resistance matrix, one must first define an n x n array of cells, in which n is the total number of nodes. Node number labels next to the left edge and above the array are used to define the location of the resistances. In the resistance matrix shown in Figure 4, the upper-right hand cells are defined by referencing the corresponding cell in the list of resistances (for example $R_{1\text{-}2}$ in the matrix points to cell D3 in the list of resistances). The diagonal terms in the resistance matrix (in yellow) are set to have essentially infinite thermal resistance of 1e6. Similarly, since Node 1 and Node 4 are not connected, the thermal resistance between them is also set to 1e6.

The resistance matrix is symmetric (the resistance between nodes 1 and 2, $R_{1\text{-}2}$ is identical to the resistance between nodes 2 and 1, $R_{2\text{-}1}$). The cells in bottom, left-hand portion of the matrix are generated using the =offset(reference cell, r, c) function, which returns the value of the cell that is r rows below and c columns to the right of the reference cell[2]. Through the appropriate use of absolute and relative references[3], a single equation can be input and copied to fill the rest of the lower, left-hand portion of the resistance matrix.

Once the resistance matrix has been established, the values of K can be determined by finding the inverse of each R-term. The function =round(value, z), rounds the result to z decimal places. In this case, a somewhat arbitrary value of z=4 was assigned; this rounded the values of K to 4 decimal places and caused the approximately infinite thermal resistance values of 1e6 to become truly infinite, as their reciprocals were rounded to 0 using this function. Figure 4 also shows that the sums of the K-values for each node were calculated using the =sum() function to add up the four terms in each node's column.

Finally, the boundary condition vector terms were calculated by adding the heat input value for each node (which were entered manually as the Heat Input Vector in Figure 3) to the reference temperature (T_4) multiplied by the thermal conductance (K) between the node and the reference temperature. If multiple reference temperatures are defined in a system, such as a system that is cooled internally by air at a different temperature than the outside air temperature, the boundary condition vector would include the sum of each reference temperature multiplied by the corresponding K value.

1.	Diagonal terms ($K_{1\text{-}1}$, $K_{2\text{-}2}$, etc.) and resistances between nodes that are not connected are designated as having infinite thermal resistance and the conductance is zero.
2.	All non-diagonal terms in the conductance matrix are equal to $-K_{i\text{-}j}$, i.e. $-1/R_{i\text{-}j}$.
3.	On the diagonals, the terms in the conductance matrix are the summation of all $K_{i\text{-}j}$ values for thermal resistances connected to that node.
4.	The terms in the boundary conditions vector are defined as the heat dissipation at the corresponding node added to the reference temperature (or temperatures) multiplied by the conductance between that node and the reference temperature(s).

Table 1. Rules to Generate Conductance Matrix and Boundary Condition Vector

The equations for calculating and utilizing the conductance matrix, [C], are shown in Figure 5. Since Node 4 is a defined boundary condition, it is not included in [C], the terms of which are determined using the =if(statement, true, false) function. Using the appropriate absolute/relative references[4],

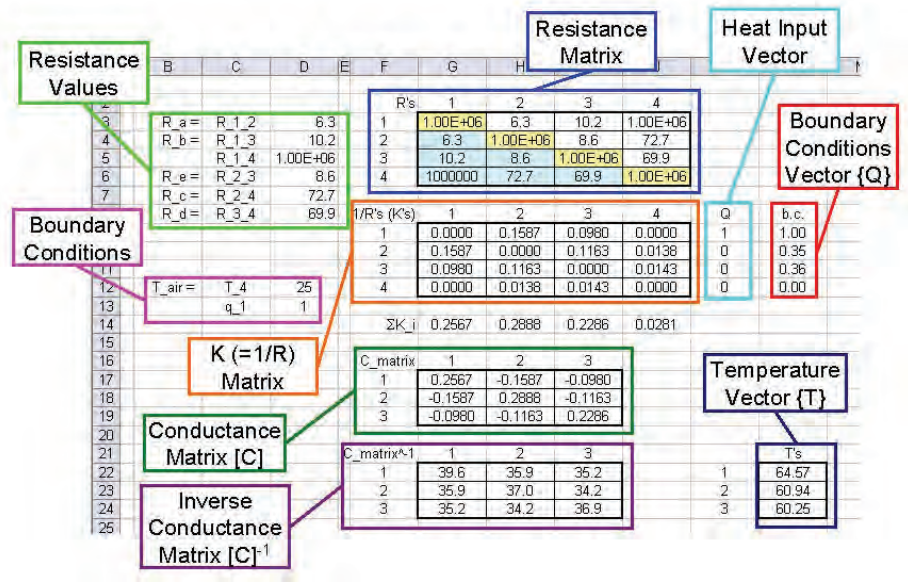

Figure 3. Spreadsheet matrix solver map.

[1]This map is simply a screen capture of the spreadsheet with annotations added to the image using PowerPoint. The author recommends creating such a map such as a general practice for all reasonably complex spreadsheets and including it as a separate worksheet – especially if the spreadsheet is to be used by others or may be resurrected after its initial creation.

[2]Figures 4 and 5 show formulas with arrows pointing to specific cells. Once these equations have been generated, they are copied to the entire area enclosed by the dashed lines. Regions of multiple cells enclosed by a solid line indicate matrix operations that are applied to all the cells in the array.

[3]Including a dollar sign in front of a row and/or column reference makes it an absolute reference that doesn't change when the cell is copied. For example, the term G$2 in an equation will always refer to a cell in row 2 but will shift to other columns if the cell is copied to the left or right.

the =if() function determines that a cell is along the diagonal if its row number equals its column number. If the cell in the conductance matrix is on the diagonal, its value is equal to the sum of conductance values for that node (ΣK_i). If a cell in the conductance matrix is not on the diagonal, its value is equal to –K for that cell. Again, this function is written in such a manner that it is entered once and then copied to fill the rest of the conductance matrix.

Once the conductance matrix has been defined, its inverse can be calculated using Excel matrix functions[5]. Matrix functions create arrays of cells, the size of which depend on the matrices that they are processing. To calculate the inverse of a matrix, select a separate set of cells that have the same number of rows and columns as the original matrix. Then type the function =minverse(reference_cells), in which reference cells is the entire range of the matrix to be inverted. At this point, do not simply 'Enter' the function but instead use 'Ctrl-Shift-Enter' to define it as a matrix function. This will generate the inverse conductance matrix in the cells that were initially selected. The node temperatures can then be calculated by multiplying the inverse conductance matrix with the boundary conditions vector using the =mmult(inverse conductance matrix, boundary conditions vector). This function, like =minverse(), is a matrix function so three cells (for the three nodes) must be highlighted and the equation must be entered using 'Ctrl-Shift-Enter'.

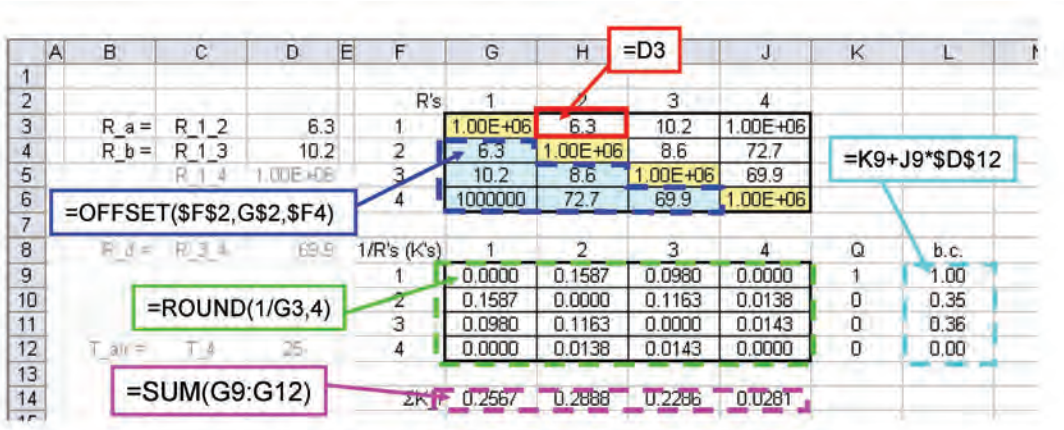

Figure 4. Generating resistance and K terms.

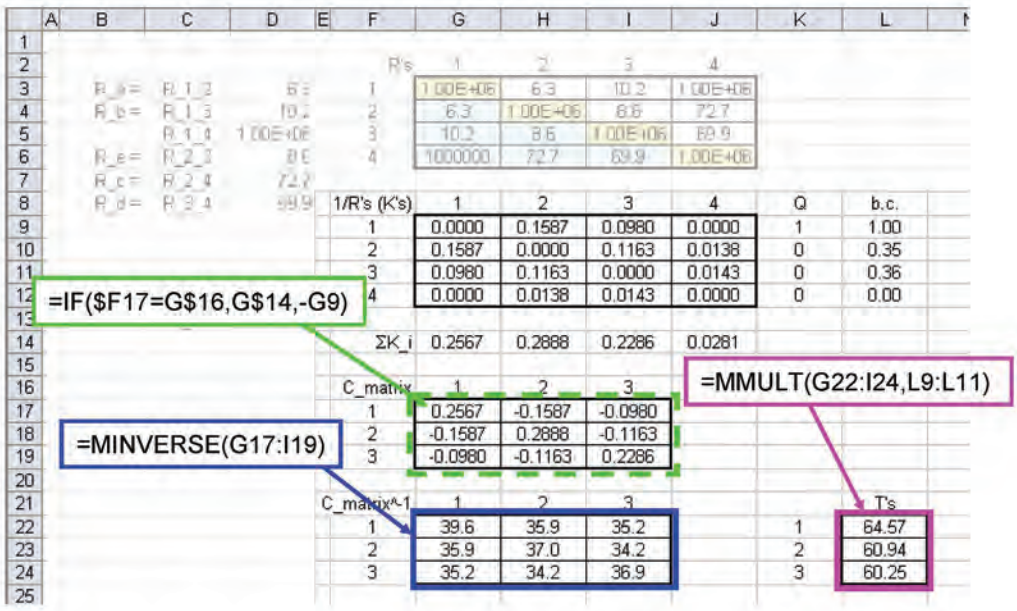

Figure 5. Calculating conductance matrix and using it to solve for temperatures.

In conclusion, while spreadsheets may not be the most efficient method for solving matrix equations, they can be an effective alternative to other methods that may not be as accessible to many engineers. Part 2 of this series will discuss application-specific issues for creating and adding thermal resistances as well as describe an actual industry analysis that used the thermal resistance network approach to assess an electronics system.

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3. http://orion.math.iastate.edu/mathbus/sp/current/excel/tutorial2.xls

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[4]Note that one can scroll through the four possible absolute/relative references for a specific cell after selecting it by pressing the F4 key.

[5]Readers may refer to online tutorials, such as [3], to learn about using Excel for matrix analysis in more detail.

thermal facts and fairy tales

fully-developed channel flow: why is Nu constant?

Clemens J.M. Lasance
Philips Research Laboratories Emeritus

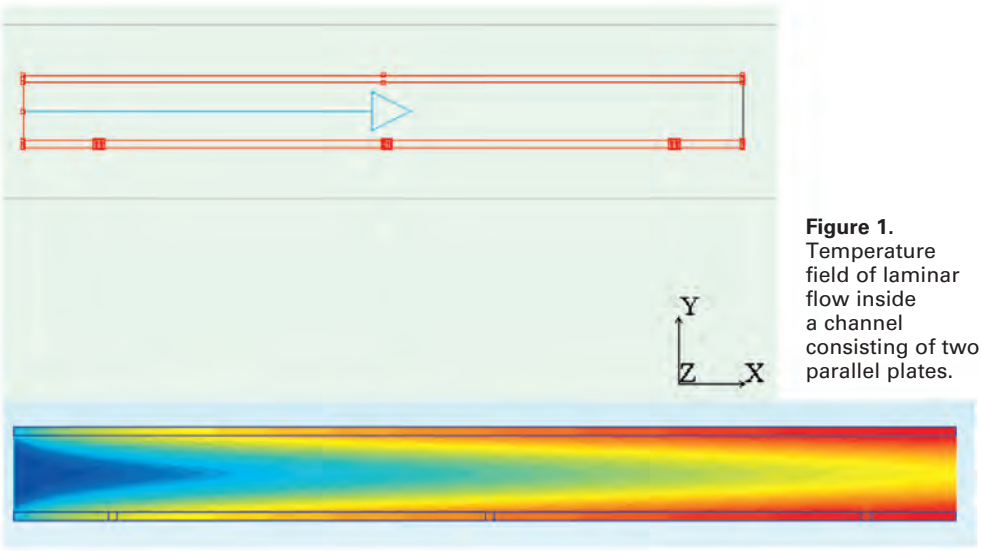

Figure 1. Temperature field of laminar flow inside a channel consisting of two parallel plates.

The last time the subject of my column was: 'Most of us don't live in wind tunnels, neither in the world of Nusselt.' I promised more comments about the (mis)use of the heat transfer coefficient h in real-life applications where we are dealing with multiple sources, anisotropic PCBs and multilayers. In this column I would like to share with you my thoughts on something that bothered me from the moment I started research in the field of thermal management. It concerns the fact, as most of you know, that Nu is constant for fully-developed channel flow with constant boundary conditions, for example constant temperature or constant heat flux. This is a typical example of a purely academic problem because in practice we (almost) always have a mixture of the two due to lateral heat spreading in the channel wall.

Because Nu equals h·D/k, with D the hydraulic diameter of the channel and k the thermal conductivity of the fluid, the consequence is that h is constant, hence, among other things, h is independent of the velocity. This strikes me as pretty strange. In my view, given the mere fact that we have defined h as a metric for heat transfer (per unit area per degree C), I would have expected that when the heat transfer increases so does the metric that describes it. If this is not the case, the obvious conclusion is that the way h is calculated is not correct, from a philosophical point of view at least.

Of course the heat transfer calculated using the constant h does change when the velocity changes, dependent on the boundary condition. For constant flux the fluid temperature decreases with increasing velocity, and hence the wall temperature decreases which means that the heat transfer increases. For constant temperature the fluid temperature equals the wall temperature far enough from the inlet, hence there is no heat transfer at all. Of course, because $q = h \cdot A \cdot \Delta T$, with A the heat transfer area, q is zero because ΔT is zero, even when h is constant. Nevertheless, my intuition tells me that the heat transfer coefficient should go to zero because there is no heat transfer.

Note: I had some interesting discussions with Bob Moffat, the 'inventor' of the adiabatic heat transfer concept [1]. I could not convince him of the way I looked at the problem. Hence, to prevent being seen as a Don Quixote: I don't challenge the Nu being constant using the standard definition, I challenge the definition itself. I don't even challenge its usefulness. My argument is not that h_{adiab} is practical in this case, it is not. Of course nobody is going to use hadiab for channel flow; what I want to demonstrate is that the concept of constant h is incorrect, even if it is useful in practice! For many people the concept of God is useful but this does not automatically imply that God exists. As a bonus: Bob Moffat told me that in a time long past Bill Kays, his mentor, was of the opinion that h should go to zero when ΔT goes to zero. I am in good company!

I asked myself the question: suppose we could define a physically correct adiabatic h, how would this h behave when we change the velocity? To address this I used a full-blown numerical analysis of fully-developed laminar flow inside two parallel plates. The idea is that we may consider the channel wall as consisting of many sources separated by an insulation layer of negligible thickness. Figure 1 shows the layout of the setup.

To ensure fully-developed flow a number of requirements should be met, and I had many interesting discussions with Bob Moffat on how to realize this because even a small departure from

fully-developed would probably render the results useless. For the experts: based on the eigenfunction solutions, x^+ should be at least 0.2 to guarantee fully-developed flow. Following his advice I used the following input data:

Channel width: 8mm
Channel length: up to 250 mm
Fluid velocity: 2-20 cm/s
Adiabatic cell size: 0.25-1 mm
Uniform heat flux: 100 W/m^2

The problem to be addressed is: How can we define a local adiabatic h? By adhering to its definition: the reference temperature is found by switching off the dissipation and recording the adiabatic or unpowered temperature: $q = h_{adiab} \cdot A \cdot (T_{wall} - T_{adiab})$. In our setup this is realized by setting the lateral thermal conductivity of the channel wall to 'zero' and perpendicular to this to 'infinite', to prevent lateral heat spreading altogether. Additionally, starting from a uniform heat flux for the channel walls, an extra negative source was added to the adiabatic cell to result in zero heat flux in order to find the local adiabatic temperature. Of course one of the parameters is the size and location of the cell. The smaller the cell, the less the effect of setting the dissipation to zero has on the downstream flow. Figure 2 shows a plot of the channel wall temperatures when one adiabatic cell on the bottom wall at position 5 mm. Also the air temperature at midplane is shown.

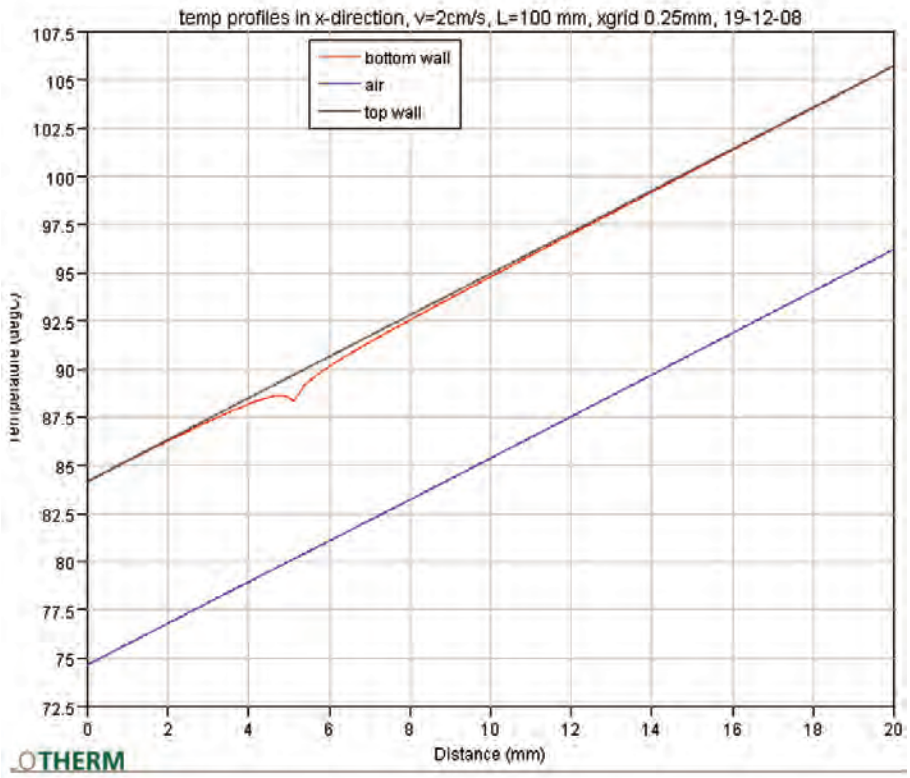

Figure 2. Temperature profiles in x-direction with one cell adiabatic.

As a check, the mean mixed temperature for several positions in the channel and the resulting standard Nu number were calculated. It turned out that the Nu value was within 1% of the theoretical value (8.235), giving confidence to the calculations.

The h based upon this Nu can then be calculated to be 13.4 W/m^{2}K.

The question is: how does h_{adiab} behave when we change the velocity? Well, just as I thought: it depends on it. Figure 3 shows some results.

From the graph you see that for zero velocity there is still appreciable heat transfer, caused, of course, by pure conduction through the fluid. However, this conduction contribution is not easy to calculate because it is not 1D! The 1D conduction heat transfer would result in an effective h of roughly 3 W/m^{2}K; because of heat spreading from the adiabatic cell, this value is much larger in practice.

But this is not the end of the story. Some interesting questions pop up, such as:

- What happens when the cell width goes to zero?
- What is the influence of lateral conduction in the fluid?
- What exactly happens when we apply a step function in the heat flux along the wall with the adiabatic heat transfer coefficient along the wall?
- How does the cell width influence the results?

Back to the original question. I personally did not buy an h that is constant whatever the velocity, it just does not make sense. But I wonder also if this is just a matter of semantics, in other words, should a heat transfer coefficient indeed describe heat transfer?

I would appreciate your opinion.

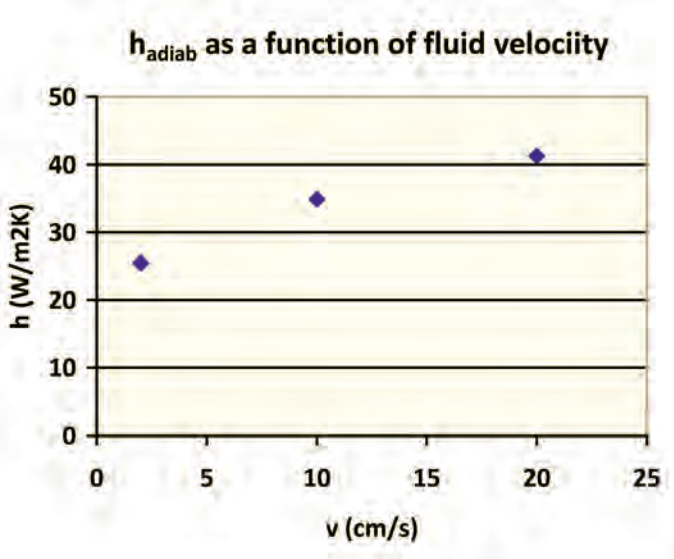

Figure 3. h_{adiab} as a function of fluid velocity.

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creating PCB thermal conductivity maps using image processing

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INTRODUCTION

Thermal conduction into a printed circuit board (PCB) is often an important part of the critical heat transfer path in electronic devices. Efficiently capturing the effect of the heterogeneous and anisotropic nature of the PCB's copper distribution on local thermal resistance in a simulation has long been a goal of the electronics thermal analyst community. There are many modeling options available that offer simplicity at the expense of accuracy, and vice versa. The method discussed here may be viewed as a compromise between computational effort and achieved accuracy.

The least computationally intensive approaches are those that employ a global orthotropic material for the entire board. The values used for the orthotropic thermal conductivities range in the literature from semi-experimental formulations [1, 2] to thermal resistance network analytical derivations [3]. Using a single material property for a PCB is adequate for simulations that do not have the board on the critical heat transfer path, but the failure to capture the local effective thermal conductivity variation and heat spreading limits its usefulness in most other applications [4].

Methods that move the single material assumption to the layer scale have become common in applications concerning package characterization or design [5, 6, 7]. Using this approach, estimates are made based on copper content for the in-plane and through plane conductivities and a single material is used for each metallic and dielectric layer. This is an improvement over the single material method, but has questionable validity when the layer demonstrates strong non-uniformity in copper distribution. There have also been several methods introduced to consider local variations of thermal conductivity within the layer involving finite element and finite difference iterative calculations [8, 9].

The approach presented here also aims to refine the thermal conductivity description within the metallic and dielectric layers. An array of rectangular tiles, fitting together, without overlap (tessellated), is used to map the thermal conductivity distribution for all layers on a PCB based on monotone images exported from board layout tools. Structured pixel counting within the defined tiles, along with thermal resistance network theory, is used to estimate the local thermal conductivity val-

ues expeditiously, and with accuracy sufficient to produce results within engineering tolerances. This tiled thermal conductivity method is well suited to be applied to finite volume solutions, a popular method used to solve conjugate heat transfer problems in the electronics industry.

THERMAL CONDUCTIVITY MAPPING

Creating a tessellated thermal conductivity map for a PCB is contingent upon the extraction of monotone images from the board layout tool for each metallic layer and the electrical vias. The black pixels in the images represent copper, and the white pixels represent dielectric material.

Each image is then reduced to a tiled array based on settings for:

- Resolution of Longest Side: This setting controls the number of tiles to be used along the longest dimension of the PCB. A large number here indicates that a large number of tiles is desired in the resultant thermal conductivity map for this layer.
- Number of %Cu Bands: Each tile created will be sorted into one of many pre-defined intervals of orthotropic (k_x, k_y, k_z) thermal conductivity. This setting controls how many intervals ('bands') will be considered for k_x, k_y and k_z, and thus controls the precision at which the thermal conductivities are computed.

THERMAL CONDUCTIVITY DERIVATION

Each tile will be assigned an orthotropic material property based on the characteristics of its corresponding image section. Figure 1 is an enlarged view of an individual tile from a metallic layer image.

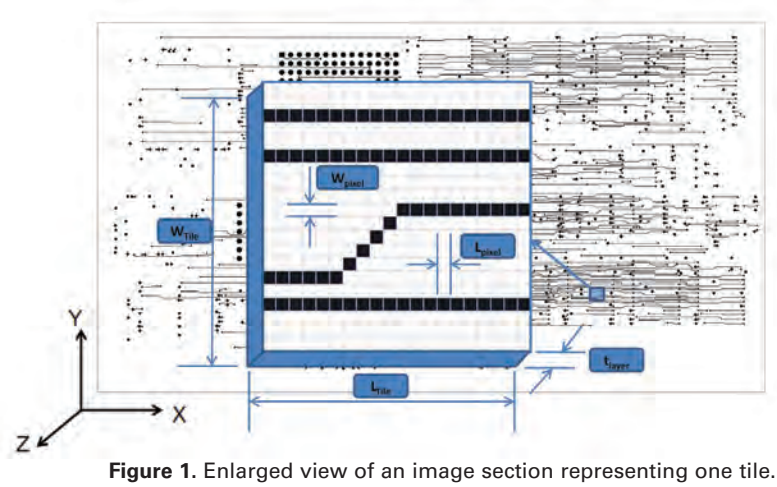

Figure 1. Enlarged view of an image section representing one tile.

A black pixel in this figure represents the conductor material and a white pixel represents the dielectric material. Each of the image tiles is analyzed to determine values for the in-plane thermal conductivities (k_x, k_y) and the through plane thermal conductivity (k_z).

The through plane conductivity (the z-direction in Figure 1) for a tile on a single layer is calculated by assuming that all the dielectric and conductor pixels in the image section are thermally in parallel.

$$1/R_{Total} = 1/R_{Conductor} + 1/R_{Dielectric}$$

$$k_z \cdot A_{Tile}/t_{Layer} = k_{Conductor} \cdot A_{Conductor}/t_{Layer} + k_{Dielectric} \cdot A_{Dielectric}/t_{Layer}$$
$$k_z = [A_{Conductor}/A_{Tile}] \cdot k_{Conductor} + [A_{Dielectric}/A_{Tile}] \cdot k_{Dielectric}$$

where:

$$A_{Conductor} = [\text{Black Pixel Count}] \cdot L_{Pixel} \cdot W_{Pixel}$$
$$A_{Dielectric} = [\text{White Pixel Count}] \cdot L_{Pixel} \cdot W_{Pixel}$$
$$A_{Tile} = L_{Tile} \cdot W_{Tile}$$

Both in-plane conductivities are computed in a similar manner. For the x-direction, each horizontal row of pixels is assumed to be thermally in parallel. The thermal resistance of each horizontal row is calculated by assuming all pixels in that row are thermally in series.

For each row, the thermal resistance is:

$$R_{row} = (\text{Row White Pixel Count}) \cdot L_{Pixel}/[k_{Dielectric} \cdot W_{Pixel} \cdot t_{Layer}] + (\text{Row Black Pixel Count}) \cdot L_{Pixel}/[k_{Conductor} \cdot W_{Pixel} \cdot t_{Layer}]$$

The effective thermal conductivity in the x-direction is then:

$$1/R_{total} = \Sigma 1/R_{row}$$
$$k_x = [L_{Tile}/(W_{Tile} \cdot t_{Layer})] \cdot [\Sigma 1/R_{row}]$$

The calculation for the y-direction is the same, but the pixel columns are used in the expressions above rather than the rows.

This procedure is followed for all defined tiles to create the thermal conductivity map of the layer. A three dimensional, orthotropic thermal conductivity mapping of the entire board is created by repeating this approach for all metallic and dielectric layers.

VALIDATION

To confirm the quality of the approximations made in this approach, the technique of using detailed simulations to numerically generate data points for comparison purposes was employed. Explicit models of a single layer board with traces included in several typical orientations and a single footprint heat source were created and compared with corresponding 10x10 tiled thermal conductivity map approximations. The average discrepancy in component temperature was recorded as 3.3%, with a maximum discrepancy of 15.3%. A complete description of these test cases and results is available in [13].

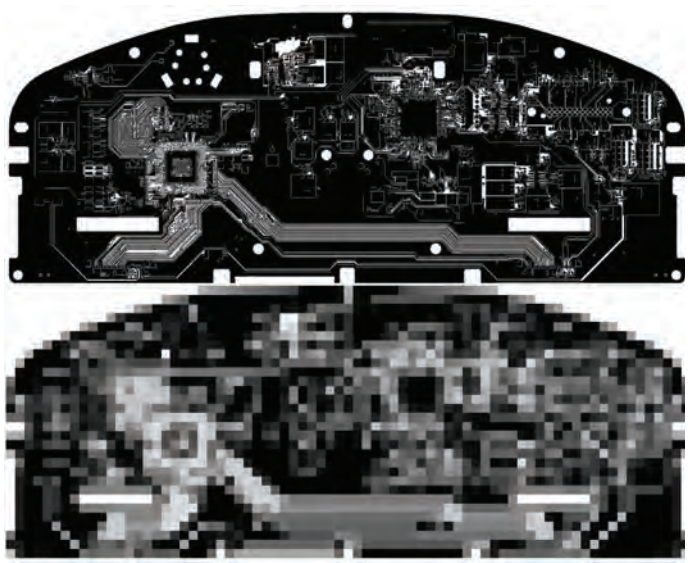

Figure 2. One of the images extracted from the layout tool and the resultant tessellated thermal conductivity map with these settings.

For further validation, this approach was also applied to a PCB for which empirical temperature data was available. The experiment consisted of an automotive board cooled via natural convection and radiation and is described fully in [13].

All of the components with significant dissipated heat load on the board were included in the analysis model as 2-R models, the best thermal representation available. The dissipated heat loads were taken from experimental measurements or from calculations where measurements were difficult. The PCB was modeled using the layer stack up and thickness for the design, along with tiled thermal conductivity maps for all of the layers. Each thermal conductivity map was created with identical image processing settings:

- Resolution of Longest Side: 75
- Number of %Cu Bands: 256

Figure 2 shows one of the images extracted from the layout tool and the resultant tessellated thermal conductivity map with these settings.

The PCB model was positioned in a simulated replica of the test environment and solved. Both measured and predicted case temperatures for the 2-R components are shown in Figure 3. The average level of discrepancy was 5.7%. This is an excellent level of correlation, well within typical accuracy expectations [12] for 2-R component models, and matching well with the deviations observed in the detailed simulation validation exercise.

TESSELLATION SETTING SENSITIVITY

An important practice in the field of computational fluid dynamics is verifying that the solution is mesh independent, i.e., additional computational mesh cells will not result in a gain in accuracy. An analog to grid independent solutions exists when utilizing this method to capture local thermal conductivity variations. The tessellation resolution must reach sufficient granularity such that the thermal conductivity mapping procedure no longer influences the predicted results.

To determine how sensitive the previous results are to the 'Resolution of Longest Side' and 'Number of %Cu Bands' settings a Design of Experiments [10] set was constructed and solved using the previous model as the baseline case. Six parameters were identified for study:

- Resolution of Longest Side for
  - Internal Layers
  - External Layers
  - Vias
- Number of %Cu bands
  - Internal Layers
  - External Layers
  - Vias

The range chosen for all of the 'Resolution of Longest Side' parameters is 1-75 (the upper limit of 75 matches the settings of the baseline results to which the forthcoming sensitivity data will be compared). The 'Number of %Cu

Bands' doesn't have a range per se, but rather a series of discrete options. The options considered for this study were: 256, 129, 65, 33, and 17.

Response surfaces [11] that yield expressions explicitly stating each component's case temperature as a function of the six design parameters and expected confidence levels were created. These response surfaces were then used to investigate the sensitivity of the thermal results to tessellation settings. The full set of results is presented in [13].

The metallic layer processing results indicate that a moderate level of resolution is able to attain results within 5% of the baseline temperatures.The requirements ranged from 25-50 for the components investigated. This range translates to a tile dimension range of 6.8 -13.6 mm. While these dimensions do not correlate with any component dimension, it qualitatively is the point where most copper features are identifiable in a bulk sense despite the image tessellation occurring. The choice of %Cu bands was relatively unimportant in most cases. It is expected that this quantity could be much more critical for metallic layers with smaller amounts of copper however.

The vias processing results indicate that the choice of %Cu bands is more important than using a high level of resolution. A modest resolution selection (5-10) with the maximum 256 %Cu bands is appropriate for this application.

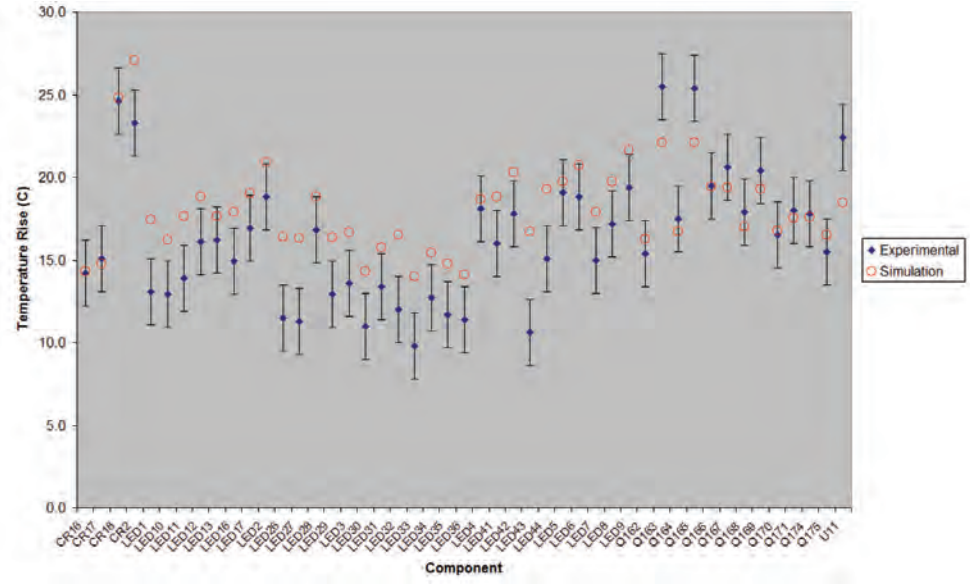

Figure 3. Predicted and measured case temperatures.

CONCLUSIONS

A tiled thermal conductivity map derived with structured pixel counting from monotone images representing the copper and dielectric distribution on the layers of a PCB was shown to correlate well with explicit, detailed trace simulations and with experimental data.

The temperatures predicted with this approach are dependant upon the settings used to describe the tessellation geometry. The sensitivity results presented [13] suggest that a tessellation resolution point exists where increasing the granularity of the tiled thermal conductivity map no longer influences the simulation results. For the PCB considered in the Validation section, tessellation independent results are achieved with modest settings for resolution of all layers and maintaining a high setting for %Cu bands. It is expected that tessellation independent status would be achieved at different settings for boards and layers with lesser amounts of copper.

ACKNOWLEDGEMENTS

The author wishes to thank Sam Gustafson of Johnson Controls for the provision of the experimental data referenced here.

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transient dual interface measurement of the rth-jc of power semiconductor packages

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Dirk Schweitzer works as a thermal engineer at Infineon Technologies AG. With more than 10 years of experience in electronics cooling, he has extensive experience in thermal simulation and measurement of semiconductor devices. He is an active member of the JEDEC JC15.1 committee and contributed to the development of boundary condition independent thermal compact models in the EU-funded PROFIT project. He authored/co-authored a total of 18 publications, 13 in the field of thermal engineering and received the Best Paper Award at SEMITHERM in 2008. Prior to his employment at Infineon, he worked as a research assistant at the University of Augsburg, studying ion beam assisted crystal growth processes by means of molecular dynamics simulations. He received his degree in Physics at the University of Augsburg, Germany.

INTRODUCTION

The junction-to-case thermal resistance Rth-JC is an important thermal characteristic especially for power semiconductor devices. Its value is often one of the main criteria for the decision whether a device can be used in a specific application and a low Rth-JC is a competitive advantage for the semiconductor manufacturer. However, it must be ensured that the data-sheet Rth-JC value does not underestimate the real value. Accurate and reproducible methods to measure the Rth-JC are required. Unfortunately these requirements are not easy to meet, which is reflected by the fact that to date no JEDEC standard for the measurement of Rth-JC has been defined. The traditional and quasi-standard measurement procedure – referred to herein as "thermocouple (TC) method" – (compare also MIL-STD-883G, method 1012.1 [1]) closely follows the definition of Rth-JC in JESD51-1 [2]: "**Thermal resistance, junction-to-case:** The thermal resistance from the operating portion of a semiconductor device to outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across that surface."

Accordingly the thermocouple-method requires the measurement of the junction temperature T_J, the case temperature T_C, and the power dissipation P, while the device (according to the above definition) is properly heat-sunk, i.e., in contact with a heat sink. The junction-to-case thermal resistance is then calculated using:

$$R_{th-JC} = \frac{T_J - T_C}{P} \tag{1}$$

This value shall be referred to herein as "steady-state Rth-JC", since it is determined under steady-state heat flow conditions.

The measurement of the case temperature is quite prone to errors. A hole or groove in the heat sink must be provided for the thermocouple wires; this however will distort the temperature field and therefore will have an impact on the results. Since the case temperature is non-uniform, the measured temperature depends on the exact position of the thermocouple. Last but not least it is extremely difficult to ensure that the thermocouple actually measures the case temperature and not

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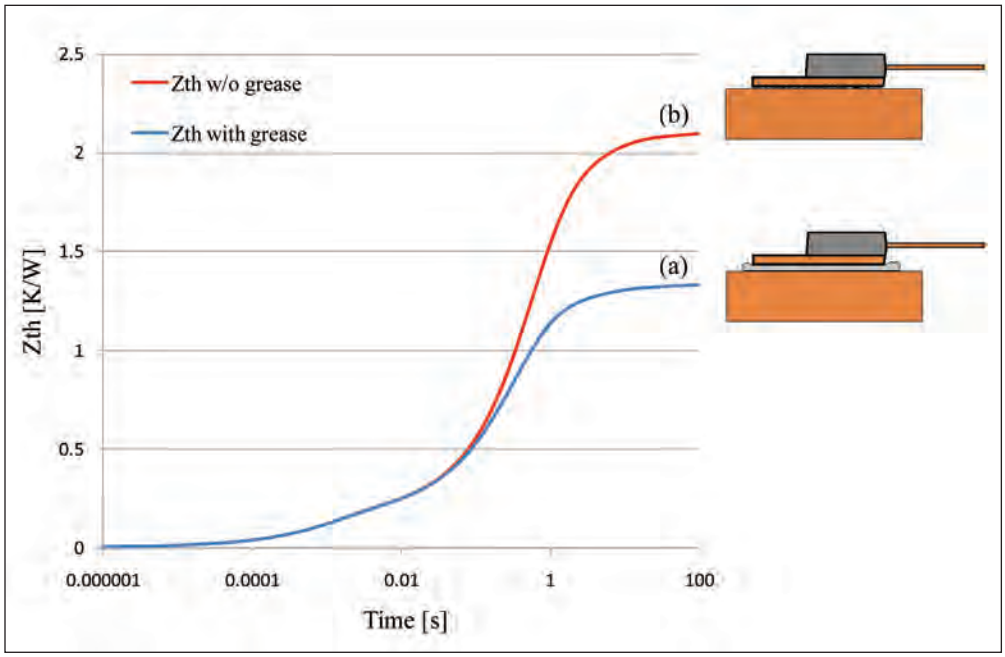

Figure 1. TDI measurement (a) with and (b) without thermal grease.

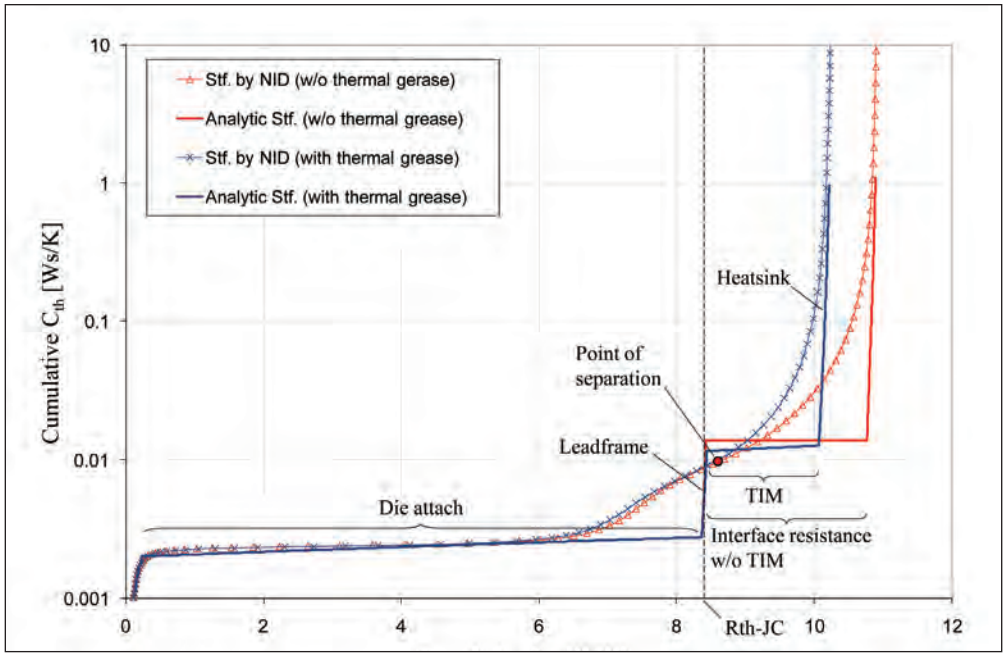

Figure 2. Comparison of structure functions obtained by NID and using a semi-analytical approach.

the temperature of the heat-sink or some value in between. Given these difficulties the reproducibility of thermocouple measurements obtained with one and the same set-up is often surprisingly good – meticulous mounting of thermocouple and device provided – but different measurement set-ups are likely to produce divergent Rth-JC values.

To overcome these problems, transient methods which do not require a thermocouple measurement have been proposed, e.g., by Siegal [3]. While in [3] the problem of determining the thermal interface resistance between package and heat sink remains unsolved, Szabo et al. presented a method to identify the Rth-JC comparing the structure functions obtained by two transient measurements with different interface layers between package and heat sink [4, 5]. Based on their work we have further developed the transient dual interface measurement (TDIM) and propose it now as a JEDEC standard for power semiconductor devices with heat flow through a single dominant path as in heat-slug or exposed pad packages.

MEASUREMENT PRINCIPLE

The TDIM method requires two Zth measurements of the same power semiconductor device in contact with a liquid-cooled heat-sink. Assuming that the chip is heated by a constant power dissipation P which is switched on (off) at time $t = 0$, the Zth is the change of junction temperature $\Delta T_j(t)$ per Watt as a function of the heating (cooling) time t:

$$Z_{th}(t) = \frac{\Delta T_J(t)}{P}. \qquad (2)$$

Each measurement is performed with a different interface layer between package and cold-plate, causing the two Zth-curves to separate at some point of time (Figure 1). Compared to the TC-method the thermocouple measurement of T_c is not necessary any more, thus avoiding the related problems. We propose to perform one Zth-measurement (a) with a thin layer of thermal grease and the other measurement (b) with no thermal interface material (TIM). The increased interface resistance in case (b) due to the microscopic surface roughness between package and cold-plate ensures a clear separation of the Zth-curves.

DETERMINATION OF RTH-JC

This dual measurement can be evaluated in different ways: One possibility is to convert the Zth-curves into structure-functions and determine the Rth-JC from their point of separation. The accuracy of this approach is limited mainly by the resolution of the NID (network identification by deconvolution) algorithm used to compute the structure-functions [6, 8].

A finite element simulation of the TDI measurement helps to get a clearer picture of the deviations to be expected. Figure 2 shows the cumulative structure-functions obtained by NID of the simulated Zth-curves of an exposed die pad device (curves marked with x or triangles). For comparison the same structure functions have been computed semi-analytically (plain curves), using an approximate model of the heat flow path (Figure 3).

Assuming that the heat flow path can be modeled by a series of truncated cones (thus taking into account the heat spreading), the thermal resistance $\Delta R_{th,i}$ and capacitance $\Delta C_{th,i}$ of the i-th slice of this discretization can be approximated using

$$\Delta R_{th,i} = \frac{\Delta x_i}{k_i A_i}; \quad \Delta C_{th,i} = \rho_i c_i A_i \Delta x_i, \tag{3}$$

Δxi, Ai, ki, ρi, ci being thickness, cross-section, thermal conductivity, density, and specific heat of that slice, respectively. For a small enough Δxi the cumulative capacitance $\Sigma\Delta C_{th,i}$ of these slices vs. their cumulative resistance $\Sigma\Delta R_{th,i}$ should approximate the actual cumulative structure function well enough for a qualitative analysis. The heat spreading angle ϕ has been adjusted for each material individually such that Rth-JC and Rth-JA of the semi-analytical model are equal to those of the FE model.

Even though the structure functions obtained by NID are too blurred to reveal the structure of the device accurately, their point of separation is close to its Rth-JC (Figure 2). Or rather: Especially because they deviate from their semi-analytical counterparts, they already separate somewhere in the TIM region, i.e., shortly after the true Rth-JC. Only if the TIM between the package and the heat-sink has a very low Rth (e.g., "liquid metal") the associated plateau in the cumulative structure function is very small and the cumulative structure functions might already separate before this point.

In the example in Figure 3 the (NID) structure functions separate at Rth = 8.7 K/W whereas the true value is Rth-JC = 8.4 K/W. Unfortunately the error does not scale linearly with the size of the Rth-JC. While for this example an error of 0.3 K/W (3.6%) is totally acceptable, it is not, if the Rth-JC itself is only about this size. Furthermore we observed, especially for devices with a small Rth-JC, that the exact determination of the separation point of the structure functions is often impeded by numerical artifacts produced by the NID algorithm.

For devices with a low Rth-JC we therefore propose another evaluation method similar to the approach suggested by Siegal [3]. This method is based upon a determination of the separation point of the Zth-curves and is only applicable to devices with thermally high conductive die attach (e.g., solder). The starting point is the observation that for these devices the Zth-value at the point of separation is always very close to the Rth-JC of the device (Figure 1).

The somewhat "intuitive" explanation for this is often that "the curves start to diverge when the heat-flow has arrived at the device/heat-sink interface." While this explanation is not exactly wrong it definitely lacks some precision and shall be investigated more closely.

The temperature difference between any two points A and B within the same solid is always connected with a heat-flow

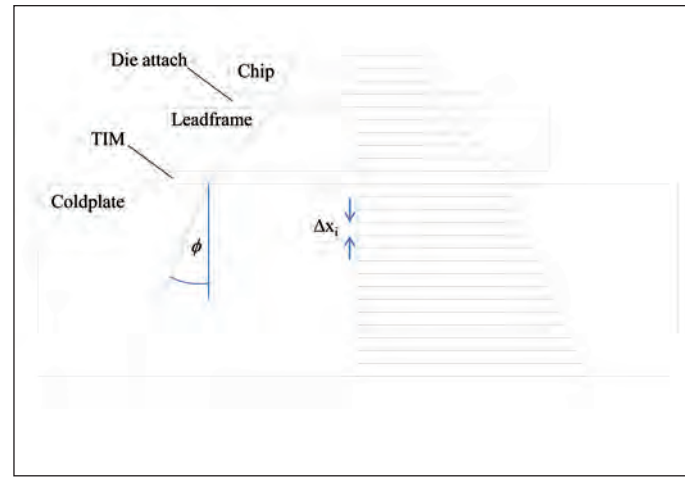

Figure 3. Approximate model for a semi-analytical computation of the cumulative structure function.

(W) between these points. The temperature gradient at location x = (x, y, z) is

$$\text{grad}\, T(\mathbf{x},t) = -\frac{\mathbf{p}(\mathbf{x},t)}{k(\mathbf{x})} \tag{4}$$

with thermal conductivity k(x) and heat-flux vector p(x, t) (W/m^2). If we move by a step ds = (dx, dy, dz) the temperature changes by

$$dT(\mathbf{x},t) = -\frac{\mathbf{p}(\mathbf{x},t)}{k(\mathbf{x})} \cdot \mathbf{ds} \quad \text{(inner product of } \mathbf{p} \text{ and } \mathbf{ds}) \tag{5}$$

Consequently the temperature difference between A and B can be expressed by the path integral

$$\Delta T(t) = -\int_{\Gamma} \frac{\mathbf{p}(\mathbf{x},t)}{k(\mathbf{x})} \cdot d\mathbf{s} \tag{6}$$

for an arbitrary path Γbetween A and B. Applied to the temperature difference $\Delta T_{JF}(t) = \Delta T_J(t)$ between junction (at $z = 0$) and fluid (at $z = z_{Fluid}$) for a semiconductor device on a liquid-cooled cold-plate, this means

$$\Delta T_{JF}(t) = \int_0^{z_{Fluid}} \frac{p(z,t)}{k(z)} dz \tag{7}$$

using the integration path Γ along the z-axis shown in Figure 4 (the minus sign has been dropped here because we are only interested in the absolute value of ΔT_{JF}). For the temperature difference $\Delta T_{JC}(t)$ between junction the path integral goes only from $z = 0$ to $z = z_{Case}$:

$$\Delta T_{JC}(t) = \int_0^{z_{Case}} \frac{p(z,t)}{k(z)} dz \tag{8}$$

Based on these equations the relationship between Rth-JC and the splitting point of the Zth-curves shall now be investigated. As an example the Zth-curves (Figure 5a), their difference (b), the heat-flux distribution along the z-axis (c), and the temperature gradient (d) have been computed for a

MOSFET with solder die attach very similar to the device shown in Figure 4. If we assume that the resolution of a Zth-measurement is 0.001°C/W (e.g., for temperature resolution 0.01°C and power dissipation 10W), the separation of the Zth-curves could be observed earliest at time t_s = 0.013s (Figure 5a and 5b). The Zth-value at that point of time is $Z_{th}(t_s)$ = 1.06 K/W.

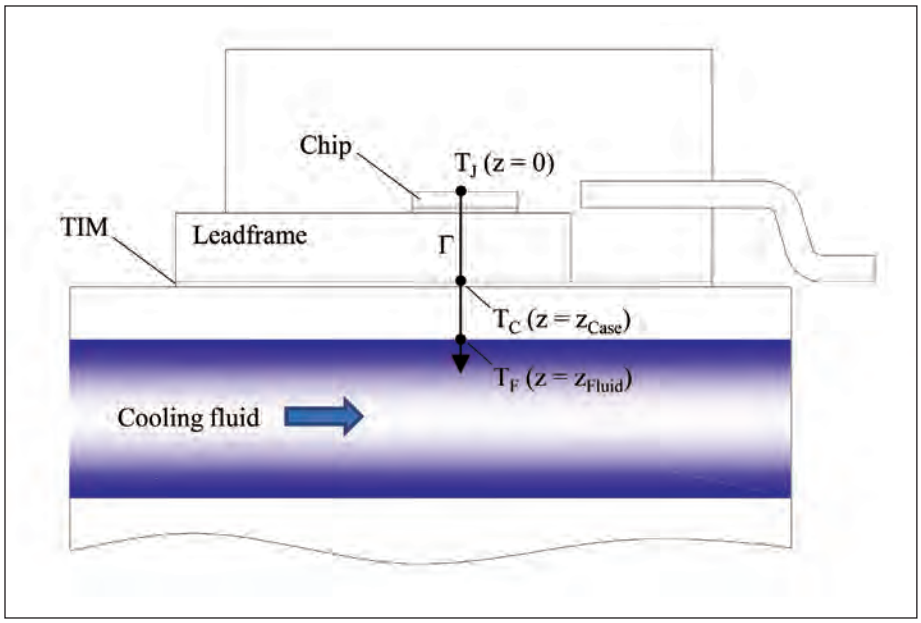

Figure 4. Integration path Γ for a device on a cold-plate.

Due to heat-spreading, the heat-flux decreases quickly with increasing distance from the chip surface. Figure 5c compares the heat-flux distributions at time t_s = 0.013s (dashed line) and in steady-state (solid line). When the Zth-curves separate, the heat-flux throughout the device has not yet developed its final strength; however there is already a non-negligible flux through the TIM layer between device and cold-plate (this being the reason why the curves start to separate) and even inside the cold-plate.

If the heat-flux $p(z)$ is divided by the piecewise constant thermal conductivity $k(z)$, one obtains the temperature gradient curve (Figure 5d). Again the dashed (solid) line shows the temperature gra-

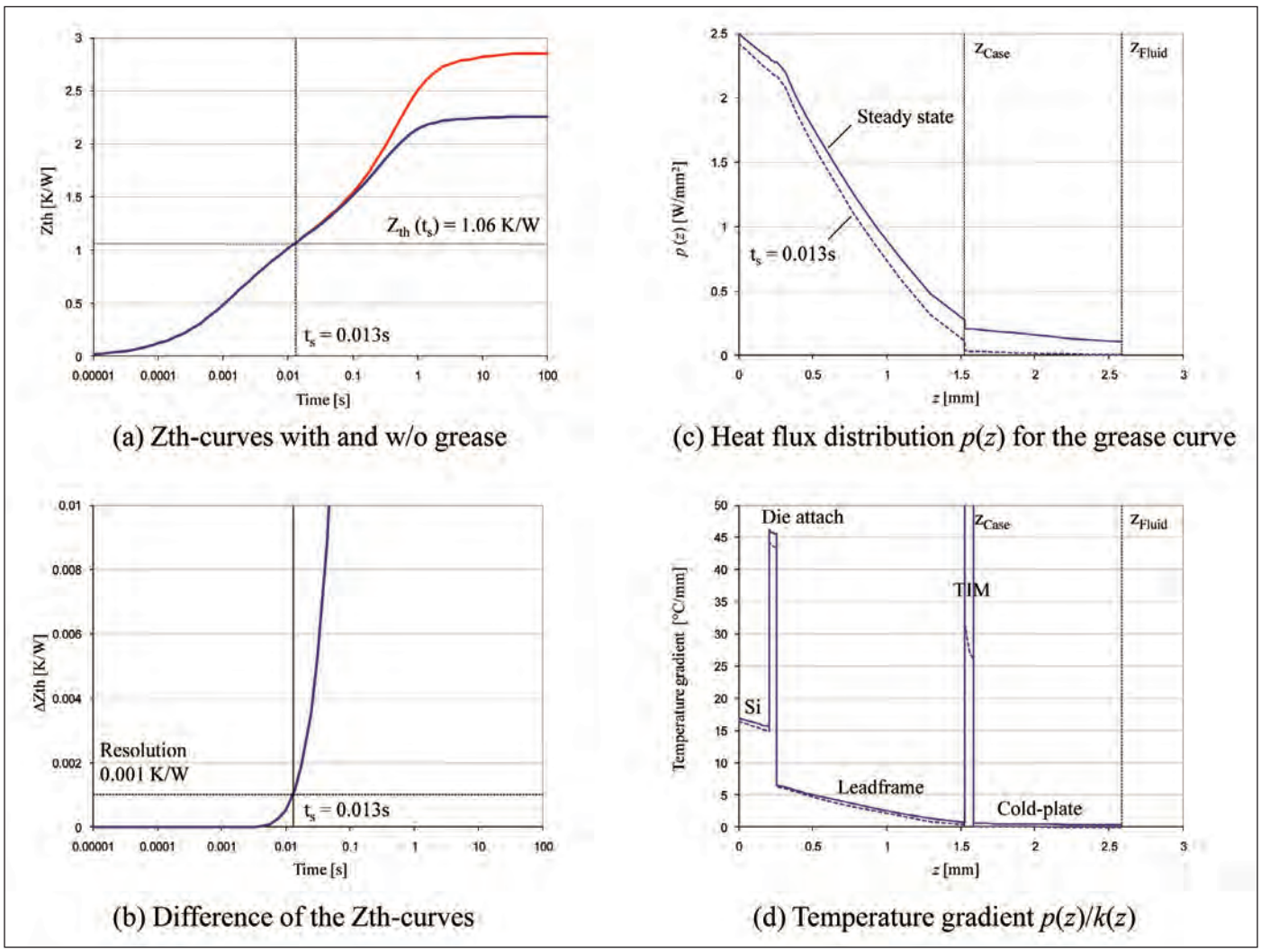

Figure 5. Analysis of a TDI measurement (FE simulation results).

dient at time t_s = 0.013s (steady-state). In this example the thermal conductivities are 148W/mK (silicon), 50W/mK (solder), 350W/mK (Cu), 1.2W/mK (thermal grease), and 350W/mK (Cu) in the chip, die-attach, leadframe, TIM, and cold-plate region, respectively. According to equations (7) and (8) the total temperature increase $\Delta T_J(t) = \Delta T_{JE}(t)$ equals the total area under the gradient-curve whereas the temperature difference $\Delta T_{JC}(t)$ between junction and case corresponds to the partial area in the range [0, z_{Case}].

Figure 5c + d illustrate the following: At time t_s, when the Zth-curves start to diverge, the heat-flux has nowhere yet reached its final strength. The resulting temperature difference $\Delta T_{JC}(t_S)$ between junction and case at that time is therefore lower than in steady-state: $\Delta T_{JC}(t_S) < \Delta T_{JC}(t = \infty)$. But a comparison of the corresponding areas under the gradient-curves in Figure 5d shows that the deviation between $\Delta T_{JC}(t_S)$ and $\Delta T_{JC}(t = \infty)$ is quite small. This deviation is compensated (in this example over-compensated) by the additional contribution of the TIM layer to the measured $\Delta T_J(t_s)$ at time t_s (area under the TIM peak in Figure 5d). Therefore we can use the following approximation to determine Rth-JC:

$$\Delta T_{JC}(t=\infty) \approx \Delta T_J(t_s)$$

or

$$R_{th-JC} \approx Z_{th}(t_s) = \frac{\Delta T_J(t_s)}{P}. \quad (9)$$

As mentioned above this approximation cannot be applied if the device contains an internal barrier to the heat-flow, such as a thermally low conductive glue die-attach. In that case the two Zth-curves might separate "too early", i.e., the Zth-value at the point of separation can be considerably smaller than the Rth-JC of the device: $Z_{th}(t_s) < R_{th-JC}$ [7]. The explanation is that an internal heat-flow barrier delays the increase of the heat-flux inside the device, i.e., the difference between the heat-fluxes at time t_s and in steady state becomes bigger. In the region of the thermally low conductive layer the heat-flux difference causes also a higher difference between $\Delta T_{JC}(t_S)$ and $\Delta T_{JC}(t = \infty)$ due to the larger factor $1/k$ in integral (8).

ACCURACY CONSIDERATIONS

The accuracy of approximation (9) depends on many factors: the resolution of the Zth-measurement which determines the point of separation, the thermal conductivity and thickness of the materials inside the device, and the thermal resistance of the TIM layer between device and heat-sink. Even the thermal resistance of the cold-plate has an influence on the resulting Rth-JC. All these influencing factors must be standardized as far as possible in order to ensure the reproducibility of the transient Rth-JC measurement. Some factors such as the thickness of the thermal grease cannot be controlled, which puts a limit to the achievable accuracy and reproducibility of the TDIM method. An estimate of the measurement error for Rth-JC is difficult since no reliable reference values exist. The traditional thermocouple measurement is too inaccurate to serve as a reference. In most cases the measured Rth-JC values could be confirmed by finite element simulations within ±15% or better. Repeated Rth-JC measurements of the same device are usually reproducible within at least ±5%. For the simulation example above the steady-state Rth-JC is R_{th-JC} = 0.99K/W, whereas $Z_{th}(t_s)$ = 1.06 K/W, i.e., the Rth-JC is over-estimated by 7%.

One can easily imagine that even a small vertical shift of one of the Zth-curves of the dual interface measurement can have a big influence on the position of the splitting point. Such a shift can be caused by a wrong offset correction of the Zth-curve. In practice it is therefore advantageous to determine the point of separation from the derivatives of the Zth-curves; that way a constant offset has no influence on the result [8]. A distance ε should be defined as separation criterion: the point of separation is the smallest time t_s for which the difference of the derivatives is $\geq \varepsilon$. The correct value for ε can be determined by finite element simulations, see [8] for a detailed description.

CONCLUSIONS

For power semiconductor packages with a single dominant heat flow path (heat-slug and exposed die-pad packages) the transient dual interface measurement is an alternative to the traditional thermocouple measurement of Rth-JC with higher accuracy and reproducibility.

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evaluation of cooling solutions for outdoor electronics

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Dr. Avijit Goswami is the managing director of Applied Thermal Technologies. During his 15 year career in fluid mechanics and heat transfer, he has worked on a wide range of applications in electronics cooling including consumer electronics, telecommunication, renewable energy and others. He obtained his Ph.D. from Stanford University specializing in the area of Computational Fluid Dynamics. Dr. Goswami earned his B.Tech. from the Indian Institute of Technology, Bombay and M.S. from the University of Texas.

INTRODUCTION

Outdoor enclosures for housing electronic circuit boards are widely used in a variety of technologies, including telecommunications, industrial and military applications. These enclosures protect the equipment against a wide variety of environmental hazards, such as sun, moisture, dust and debris. As electronic components have become more powerful and complex, power dissipation from them keeps rising and thermal management has become a critical issue. In addition, solar loading further complicates this problem depending upon the size of the enclosure, surroundings and orientation with respect to the sun. Ignoring the effect of the sun can result in excessively high internal enclosure temperatures causing equipment reliability problems or even failure.

A large variety of cooling techniques have been proposed and used to cool outdoor electronic enclosures. These include conventional techniques, ranging from passive natural convection to the use of commercial air conditioners or heat pumps and concepts using thermosyphons and phase change materials (PCMs). The internal heat is transferred primarily by convection to the inside surfaces of the enclosure by conduction through the walls of the enclosure and then by convection to the external ambient.

CFD SIMULATION CONFIGURATIONS

Figure 1 shows a schematic of typical thermal resistances related to an enclosed box with internal heat generation. For such a heat dissipating box, CFD simulations were done with a commercial code [2] dedicated for electronics cooling. A total of 12 different cooling configurations were simulated. Out of these, nine configurations were created by making combinations of three types of commonly used airflow management options and three types of enclosure surface coatings. Besides these three, special configurations were selected, including a solar radiation shield, double-wall enclosure and a heat exchanger; using a typical aluminum enclosure measuring 300 x 300 x 400 mm.

There were eight printed circuit boards (PCBs) inside, each dissipating 12.5 W uniformly, bringing the total internal power dissipation to 100W. The distance between each PCB was 30 mm. The PCB measured 240 x 180 mm and 3 mm

thick. There was a gap of 35 mm between the extreme PCBs and the side faces of the enclosure. Three types of enclosures were selected – the first was completely sealed; the second was sealed with internal circulation fans and the third had vents to allow air exchange with the outside.

Three varieties of outside coating were examined, including white, black and no coating (plain aluminum finish). These coatings were selected based on their radiation characteristics, i.e., solar absorptivity (α) and radiation emissivity (ε). The white oil coating had a low value of α (0.25) and a high value of ε (0.91), making it very favorable for cooling under solar heat loads. The black coating had a high value of α (0.88) and a high value for ε (0.88). The plain aluminum finish had low values for α and ε (0.08, 0.09). In order to minimize the effect of solar loads, various options were analyzed, including employing a radiation shield, a double-walled enclosure with air circulation and a heat pipe based air-to-air heat exchanger (Figure 2). Table 1 summarizes all enclosure configurations considered for evaluation.

The sealed enclosure with internal fans case was modeled as two fans placed above the PCB assembly and oriented in suction mode pulling the air through the PCB assembly slots. The fan selected was 80 x 80 x 20 mm and had a maximum flow capacity 0.022 m^3/s and a maximum pressure capacity of 61Pa. The enclosure with louvered vents case was modeled as two opposite enclosure walls perpendicular to the PCBs having cut-outs at the bottom and top side. The double walled enclosure had an air gap of 20 mm between the inner and outer walls. A fan was placed at the top of the outer wall sucking the air between the inner and outer walls through four openings at the bottom of each outer side wall (Figure 3). For this case, the fan selected was 120 x 120 x 25 mm, having a maximum flow capacity 0.053 m^3/s and a maximum pressure capacity of 107 Pa.

For the case with radiation shield, an umbrella was used to shield the sunlight. In the simulation, this was modeled with zero solar loads on the enclosure and no radiation heat transfer from the top wall. The heat exchanger system consisted of two parallel heat pipes with condenser ends coming out of the enclosure (Figure 2). Fins were attached to the heat pipes inside the enclosure as well as outside the enclosure. Fans were used to blow air through both sets of fins. Fans selected for this case were 80 x 80 x 20 mm and had a maximum flow capacity 0.022 m^3/s and a maximum pressure capacity of 61Pa. Figure 2 also shows a schematic of the air circulation pattern and the heat flow from inside the enclosure to the outside.

Simulations were run with solar heat load as well as without. For the cases with solar load, the maximum load was assumed to be 600 W/m^2 for Pune City (India) in March, which is one of the hottest months of the year. The sun's rays were assumed to be incident on three adjacent surfaces – the top surface and two sides. This works out to a total solar load of anywhere between 0 and 200W, depending upon the solar absorptivity of the outer surface. This shows that the solar load can be of the same magnitude as the internal thermal load.

CFD SIMULATION RESULTS WITHOUT SOLAR LOAD

Initially, a set of simulation runs were carried out without any solar heat loads. Figure 4 depicts the simulation ΔT values

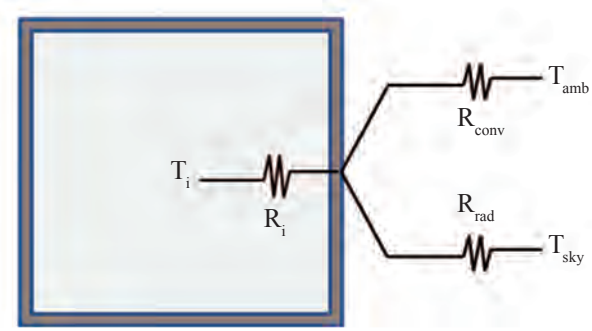

Figure 1. Schematic of typical thermal resistances related to an enclosed box with internal heat generation.

for middle PCB surface. The air inside the enclosure follows essentially the same trend (see [1] for more details).

It can be seen that, by just having an internal circulation fan, the internal temperatures can be significantly reduced. It is also well below the configuration having vents. In fact, it can be seen that vents have a relatively small impact on the temperatures. Having a black or a white coated surface can also be very effective. The case having a white coated enclosure with heat exchanger had the lowest ΔT values. In this case, a significant amount of heat is dissipated to the outside through the heat exchanger. In the cases of double-walled enclosure and radiation shield there isn't any improvement since there was no solar load.

CFD SIMULATION RESULTS WITH SOLAR LOADING

For cases with a solar heat load, the ΔT values for the middle

Config. Number	Enclosure Type		Surface Conditions (Configuration abbreviation)		
	Description	Abbreviations	No coating (NC)	Black Coating (BC)	White Coating (WC)
1	Sealed enclosure, no fans	SL	NC_SL	BC_SL	WC_SL
2	Louvered enclosure, no fans	LV	NC_LV	BC_LV	WC_LV
3	Sealed enclosure with internal fans	WF	NC_WF	BC_WF	WC_WF
4	Sealed enclosure with radiation shield, no fan	SL-SHLD			WC_SL_SHLD
5	Sealed double wall enclosure with fan	SL_DW			WC_SL_DW
6	Sealed enclosure with a heat exchanger and internal and external fans	SL-HX			WC_SL_HX

Table 1. Details and Nomenclature of Enclosure Configuration

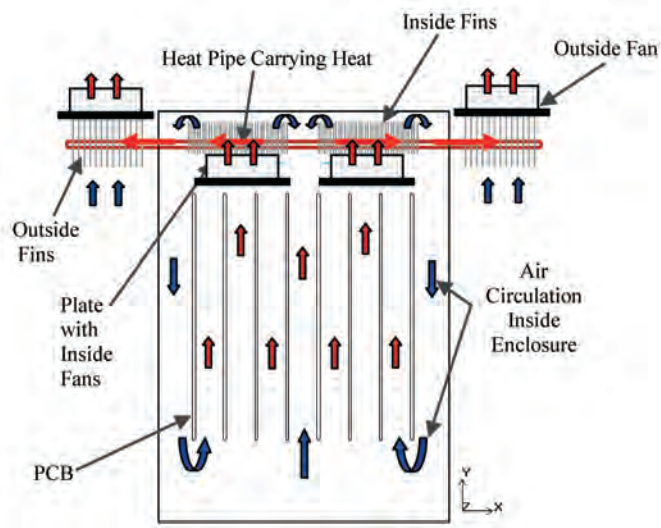

Figure 2. Heat transfer mechanism inside enclosure with heat exchanger system.

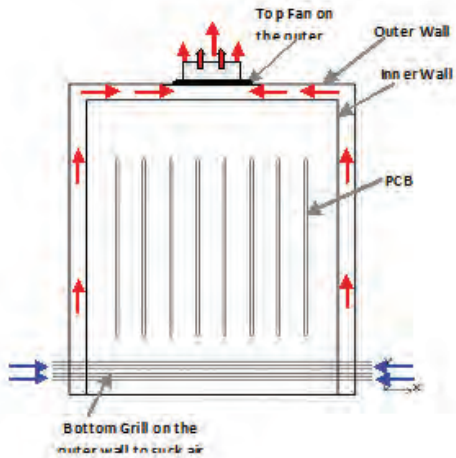

Figure 3. Schematic of double wall enclosure.

PCB are almost 20% higher for the sealed black enclosure (see Figure 5), showing that solar loading can be substantial for outdoor enclosures. Similar trends were observed compared to the cases without solar loading. The results again show that just having an internal circulation fan can significantly reduce the internal temperatures. Also, a black or preferably white coated surface can be very effective for cooling compared to a plain aluminum finish. This is because the white coating has a very favorable combination for low solar absorptivity and high radiation emissivity. The temperatures were the least in the case of the air-to-air heat exchanger. It was found that, in this case, nearly 60 W (40 %) were dissipated through the heat exchanger.

EXPERIMENTAL VALIDATION

To validate the CFD results a mock-up of the system was built and tested. Three types of enclosures were built similar to the CFD modeling configurations: a perfectly sealed enclosure, one with louvered vents, and a sealed enclosure with internal fans. Each configuration was further tested with three types of coatings: white, black, and a plain aluminum finish (Figure 6). Experiments were conducted for all configurations without solar load and for one BC_SL configuration with solar load at Pune (India) in March, in the afternoon (solar load of 600W/m^2). Figure 7 represents schematic of the enclosure set-up and the temperature measurement locations.

The enclosures were constructed using 1 mm thick aluminum sheets assembled with nuts and bolts. The PCBs were made using resistor coils sandwiched between two commercially available copper clad boards. The PCB assembly was placed inside the enclosure suspended from two rods. The thermocouples and DC source wiring were taken out through an opening created on the top side of the enclosure. The power supplied to the enclosure was 100 W through an external DC power supply and was kept constant for all the cases. To monitor the temperatures a data acquisition system (DAS) was used. Temperatures were measured on the surfaces of the middle and extreme PCBs, and also the enclosure air temperatures were measured at the bottom and at the top of the PCB assembly using T-type thermocouples. For the test case with internal fans, the fans were placed above the PCBs and oriented in the suction mode pulling air through the PCB slots

It is seen that the tested ΔT values are quite close to the CFD results for all the tested configurations without solar load (see Figure 4). For a configuration with a solar load (BC_SL) the test result for temperature rise of the middle PCB over ambient is 65°C against a simulation value of 70°C. It should be realized that it is extremely difficult to get a reliable match between experimental and numerical results for a complex electronic system because it is essentially impossible to solve all boundary layers around all objects of interest to a degree that the physics are captured correctly. Furthermore, many properties that influence the analysis are not sufficiently well known: thermal conductivities of the PCB, emissivities and

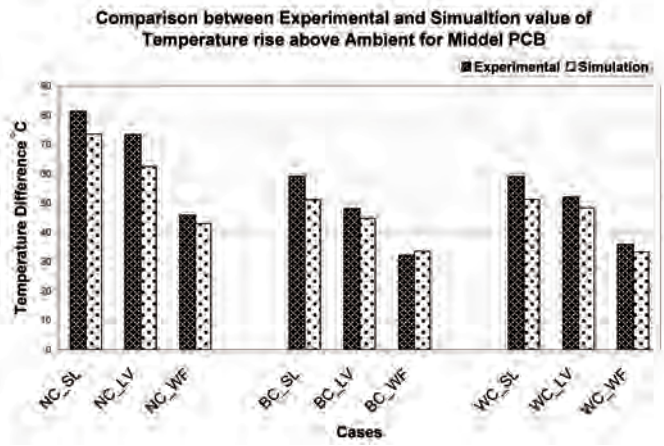

Figure 4. Simulation and experimental ΔT value for middle PCB.

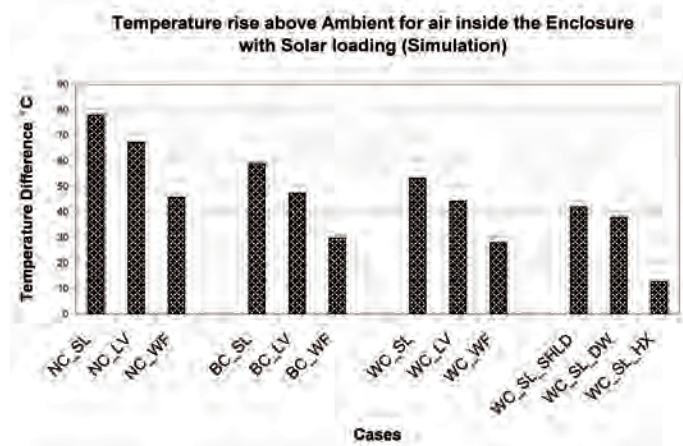

Figure 5. Simulation values of ΔT with solar loading for air inside the enclosure.

absorptivities, air resistance coefficients, etc. (see [7]).

CONCLUSION

It was found from this study that the effect of solar heat load on an outdoor system can be quite significant and can increase the internal air temperature by 20%. Different cooling approaches for outdoor electronic enclosures were analyzed and compared. The results indicate the relative effectiveness of these different cooling solutions. Relative to the sealed enclosure without any coating it was found that a black coating, or preferably a white coating, on the outside enclosure wall is a very simple and effective cooling solution that can reduce internal temperatures by around 25%. It was also found that having vents did not reduce the temperatures as significantly as having internal circulation fans. In fact, there is around a 50-55% reduction in the ΔT due to the internal fans compared to a sealed enclosure with no fans. Having a radiation shield and a double-walled enclosure with air circulation provided relatively modest improvements of around 25%. The most dramatic improvement was almost 75% in case of the air-to-air heat exchanger.

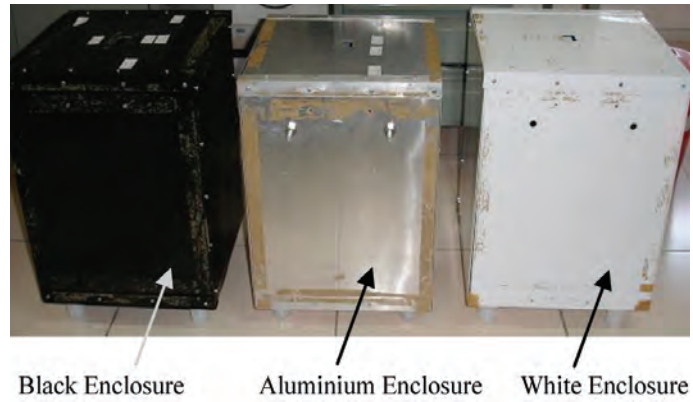

Figure 6. Enclosures with three different surfaces.

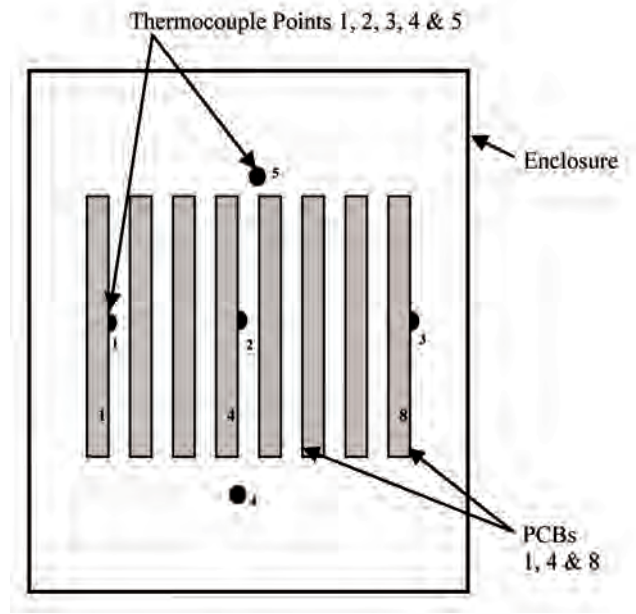

Figure 7. Schematic of enclosure set-up and temperature measurement locations.

ACKNOWLEDGEMENT

The authors of this article thank Dr. Sukhvinder S. Kang for his valuable review of the paper and suggestions during the work.

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thermal bottlenecks and shortcut opportunities; innovations in electronics thermal design simulation

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INTRODUCTION

Cooling an electronics system involves transferring heat from various heat sources to the outside ambient. Thermal simulation software provides practitioners with predictions of the temperature and heat flux distributions in and around the system, making it easy to assess the impact of design changes. While the raw simulation results enable us to measure and visualize the thermal state of a design, they do not constitute a complete analytical toolkit. What is lacking is an understanding of the mechanics driving the observed temperature field and indications about where and how the design might be improved.

Heat transfer is highly 3-dimensional within an electronics system, resulting in many possible paths that heat could follow to the ambient. Some paths will carry a lot of heat and may also offer a relatively large resistance to the heat flow, characterized by a large temperature gradient, and so present a bottleneck. There will also be opportunities to introduce new heat flow paths (shortcuts) that circumvent such bottlenecks, thermally connecting hot areas of the design to locally cooler regions.

The goal of this article is to introduce and define two novel numbers[1] derived as 3D field variables, computed as part of the thermal simulation, that taken together provide a way to decide where design improvements will have the most impact. This technical brief illustrates their use on a package-level example.

THE BOTTLENECK NUMBER

The dimensionalized BottleNeck (Bn) number is the dot product of the heat flux and temperature gradient vectors:

In vector notation: Bn = Heat Flux • Temperature Gradient

In scalar notation: Bn = |Heat Flux x Temperature Gradient x cos(Θ) |

If the angle between the two vectors is zero, i.e., the heat flux is aligned with the temperature gradient as it would be for conductive heat flow in a homogenous thermally isotropic material, then Bn is the product of the magnitudes of the vectors, since cos(0°) =1 .

Large values of this Bn scalar, computed as a part of the thermal simulation, pinpoint areas of high heat flow experiencing a large local thermal resistance (characterized by a large, aligned temperature gradient), and thus identify the thermal bottlenecks in a design. Normalizing this scalar by the maximum value in a model will provide an indication of the relative levels of bottleneck in a single simulation model.

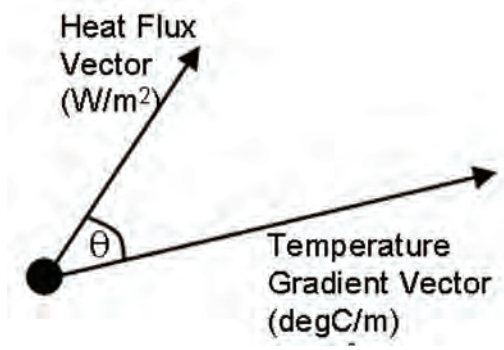

Figure 1. Misaligned heat flux and temperature gradient vectors.

SHORTCUT NUMBER

The dimensionalized ShortCut (Sc) number is also calculated from the heat flux and temperature gradient vector fields. The Sc scalar value at any point is calculated as the magnitude of the cross product of the two vector quantities.

In vector notation: Sc = Heat Flux x Temperature Gradient

In scalar notation: Sc = | Heat Flux x Temperature Gradient x sin(Θ) |

If the temperature gradient is orthogonal to the heat flux, then Sc is simply the product of the vector magnitudes, since sin(90°) =1.

Large values of the Sc field pinpoint areas where large heat flux vectors are misaligned with large temperature gradient vectors (i.e., the heat is not moving directly toward a significantly cooler area), and thus identify locations where the benefit in establishing a new heat transfer path to shortcut the heat to colder areas of the design is highest. Normalizing this scalar by the maximum value in a model will provide an indication of the relative levels of shortcut opportunities in a single simulation model.

ILLUSTRATIVE EXAMPLE

Electronics thermal simulations have always provided an indication of component junction and case temperature, information that can be used to judge thermal compliance by comparing the simulated temperatures against the maximum

[1]The descriptions of the BottleNeck (Bn) and ShortCut (Sc) numbers and their application to the post-processing of simulation data are proprietary and a patent is pending at the time of publication.

rated values. This is useful, but provides very little insight about **why** the temperature field is the way it is, and more importantly from a designer's perspective, **how** and **where** to improve it.

To illustrate the Bn and Sc numbers in practice we have chosen a TO263 package mounted on a small test board in natural convection. The package is modelled in detail, with an isotropic trace layer included on the top of the board.

Thermal simulations can allow further insights into the heat removal paths by, for example, examining heat flux vectors. However, indications of the direction and magnitude of the heat flux vectors do not provide a measure of the ease by which the heat is leaving the system. Nor does it provide insight into where and how the heat flux distribution could be better balanced or re-configured to improve performance.

The Bn number is shown on a slice through the package symmetry plane, and in the top trace layer of the PCB in Figure 4.

The Bn field shows bottlenecks where the heat enters the top trace layer. Using these locations as a guide, the designer can then introduce targeted changes to relieve these bottlenecks and thereby reduce package temperatures. In this case, a solder pad on the PCB could be placed beyond the end and on the sides of the Cu-EFTEC-64T package tab, where the Bn field shows red in Figure 4.

The Sc number exhibits non-zero values at the interfaces between materials, highlighting the areas where conduction shortcuts should start. Similarly, high Sc numbers in the air adjacent to a solid surface indicate regions where convective shortcuts should be considered, extending the surface area in contact with the air by introducing a heat sink.

The Sc field is shown on the same planes in Figure 5. High Sc numbers in the package tab at the tab-PCB interface indicate possible regions to insert thermal vias. High Sc numbers on the top of the package and on the underside of the board indicate regions of the air where heat transfer may be further enhanced through the addition of area-extending heatsinks.

Together the Bn and Sc fields offer tremendous insight into why the thermal performance of a design is what it is, and better, provide graphical information as to where the best opportunities for design improvement can be found. The Bn field provides clear identification of thermal bottlenecks and the Sc field indicates opportunities to introduce thermal shortcuts.

Unlike design-of-experiment methods, the Bn and Sc fields provide physical insight, helping both new and experienced thermal designers make targeted remedial thermal design modifications quickly and effectively. Application and interpretation of the Bn and Sc distributions within typical electronics design constraints offers a systematic methodology for determining the most promising thermal design modifications, by providing evidence beyond engineering intuition and experience where such modifications should be pursued.

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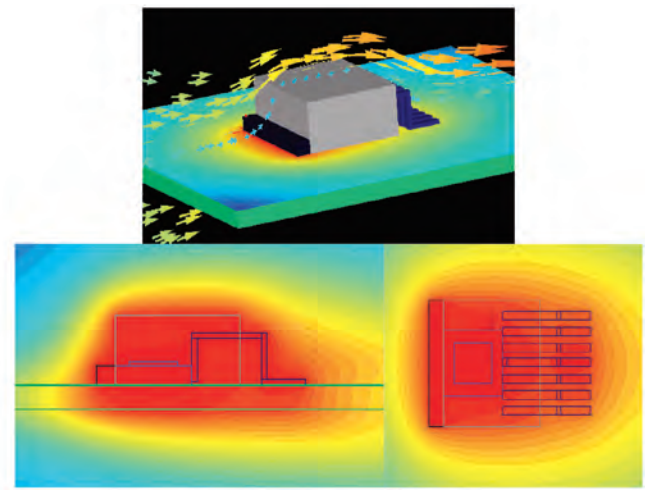


Figure 2. Thermal simulation of a TO263 package showing temperatures and air flow.

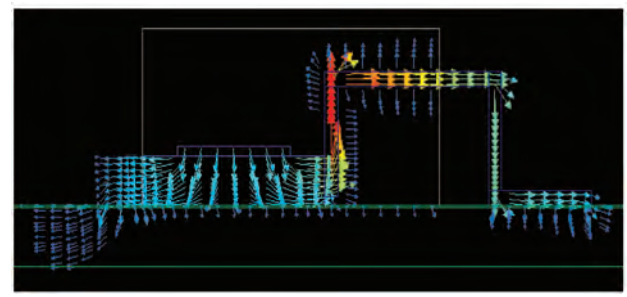


Figure 3. Typical thermal simulation results showing heat flux vectors.

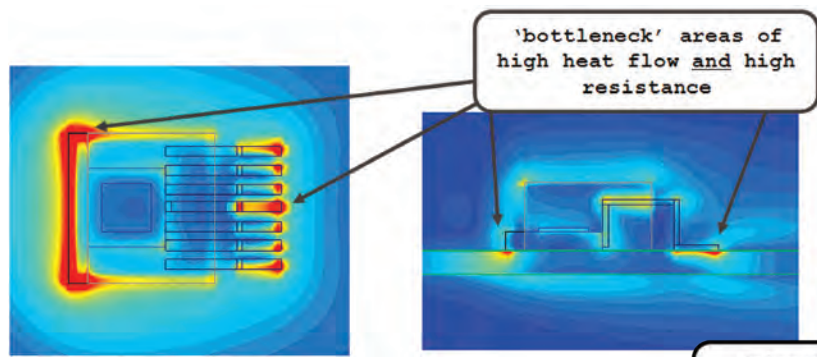


Figure 4. Thermal bottlenecks in a generic TO 263 package.

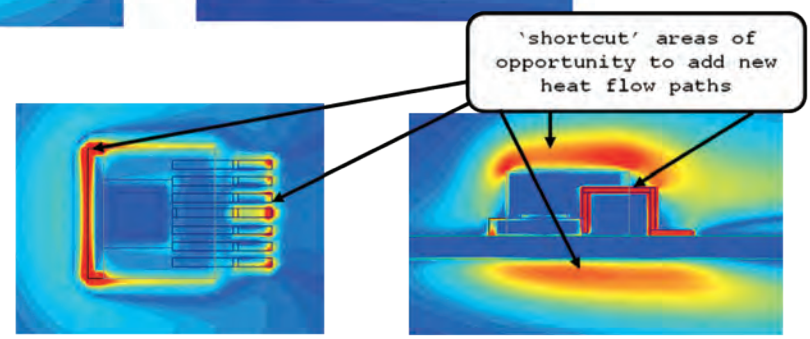
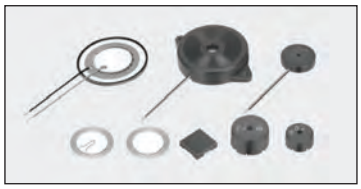


Figure 5. Potential thermal shortcuts in a generic TO263 package.

Ultra-Thin Waterproof Piezoelectric Speaker



Murata Electronics North America recently launched an ultra-thin waterproof piezoelectric speaker. With a thickness of only 0.9mm, this 19.5mm x 14.1mm speaker enables greater design freedom for the rapidly growing and evolving mobile market. The speaker achieves IPX7 grade waterproof protection without the need of a waterproof acoustic membrane. Using acoustic mesh and double-sided tape to seal the speaker to the front cavity, this waterproof speaker application allows for decreased application costs, thin size, and good sound performance. The high torque nature of the speaker's piezoelectric motor also makes it ideal for operation in very small and thin back cavities where dynamic speakers struggle to operate. As such, these features make the speaker ideal for mobile phones, music players, digital still cameras, digital video cameras, IC recorders, e-books and other mobile equipment.

Source: Murata

New TIM Catalog Released

Fujipoly has released its new Thermal Interface Material and Elastomeric Connector product catalog. The free 52-page product overview and technical design guide includes installation suggestions, as well as detailed thermal performance and electrical conductivity data points.

Several new pages of high-performance and low-cost thermal materials have been added to complement the company's current product assortment. Fujipoly's new expanded catalog also features a complete section dedicated to high density, low resistance, electrically conductive silicone connectors.

Source: Fujipoly

Light Tack Adhesive Eases Fitting of Thermal Interface Pads

MH&W International now provides U 90 silicone-free thermal interface materials with a new light tack adhesive to provide high thermal conductivity where contamination threats prevent the use of silicone-based thermal pads, and allow their easy positioning between components and heat sinks.

MH&W's Keratherm U 90 thermal interface material is a ceramic-filled polyurethane film with a thermal conductivity of 6.0 W/mK and thermal impedance of 0.05 Kin2/W. A lower cost version, Keratherm U 80, also silicone-free, provides 1.8 W/mK of thermal conductivity and 0.11 Kin2/W of thermal impedance.

Source: MH&W

Product Line for Cooling Applications Requiring Fan Guards

Orion Fans now offers a complete line of wire mesh, plastic, louvered, push-on, metal and filtered fan guards and kits, providing design engineers multiple guard options when evaluating fans for their specific applications. Whether the fan application requires finger protection and/or additional filtering to prevent dirt and dust from entering equipment, Orion Fans offers every type of guard option for applications including enclosures, industrial automation, network equipment, medical equipment, truck and automotive.

Get more details from Orion Fans.

Source: Orion

Testing Station Allows Thermal Analysis of Electronics Chassis

Advanced Thermal Solutions, Inc. (ATS) introduces a new testing station that allows in-house, low cost, thermal analysis and testing of electronics chassis and PCBs. The iTHERM-200™ is an integral system of instruments for precisely measuring and recording airflow velocity and temperature data at multiple points inside electronics housings and on circuit cards. The new system includes a freestanding wind tunnel, an automated wind tunnel controller, sensors and a temperature and air velocity scanner. The system's large test chamber and eight candlestick-style sensors allows characterization testing on active or prototype boards and racks, including single ATCA, MicroTCA, cPCI and AMC.

Source: ATS

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New CP3000NV UPS Series (60-160 kVA)

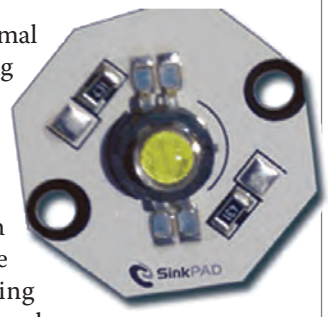
Targeting medium-sized data centers, light industrial systems, and other mid-range power protection applications, Chloride introduces its CP3000NV series of three-phase UPS with module ratings from 60 kVA to 160 kVA.

In line with Chloride's green commitment, the CP3000NV Series supports environmental objectives by featuring AC-AC operating efficiencies of 95%, a flat load/efficiency curve, lower heat rejection to reduce cooling loads, and Green Battery Management™ technology that minimizes power consumption through intelligent battery charging, resulting in a longer battery life.

To minimize direct electrical and cooling costs, the CP3000NV series is transformer-less at 208/208V and 480/480V, a benefit that also translates into lower overall weight, a smaller footprint, and faster installation. The advanced IGBT front end assures low input harmonics and simple generator interface.

Source: Chloride

Thermal Management Printed Circuit Board for LED Cooling Applications



SinkPAD Corporation is a thermal management company addressing thermal challenges facing the solid state lighting industry specifically in aluminum PCB (LED PCB) applications.

IMS PCBs with efficient through plane thermal conductivities are important for high heat generating LEDs. Although high thermally conductive metals are used, IMS PCB performance is dependent upon the contact area, material thickness and thermal resistance of each material located between heat source and the atmosphere.

SinkPAD™ technology for aluminum IMS PCB significantly improves LED thermal management in all LED systems but is most effective in high-power and high-bright surface mount LED systems that can't efficiently dissipate heat rendering them unviable for commercialization.

SinkPAD™ conducts heat out of the LED system (LED cooling) by enabling a direct thermal path between the LED and surrounding atmosphere, which eliminates thermal resistance introduced by the dielectric material in a traditional IMS PCB or MCPCB. The SinkPAD™ design completely removes the substance with the lowest thermal conductivity/highest thermal resistance from the structure. SinkPAD™ still uses a dielectric, but this dielectric isolates the metal base electrically and leaves it thermally connected.

Source: SinkPAD

Silicone Elastomer Handbook Released

The Silicone Elastometer Handbook, A guide to applied silicone elastometer technology, explores all up-to-date aspects of silicone technology and offers case histories to reinforce principles being relayed and display real-world problem solving. Written by David M. Brassard, founder and technical director of Silicone Solutions, the book is based on a short course the author teaches at the University of Akron, College of Polymer Science and Polymer Engineering. The handbook can help companies explore the possibilities of entering the silicone market, including, but not limited to formulations, raw materials, current suppliers, as well as necessary equipment.

Source: Silicone Solutions

Thermal Gap Fillers Combine High Performance, Low Pricing

New TP-S30 thermal interface pads from MH&W International provide 3.0 W/mK of thermal conductivity between hot components and heat sinks at lower costs than competing gap filler materials. Pads of TP-S30 thermal gap fillers are soft and compliant for easy compression and filling of air gaps between mounting surfaces to optimize heat transfer. Applications for these gap fillers include alternative energy, consumer electronics, telecommunications, power supplies, flat panel displays, and portable electronics.

Source: MH&W International

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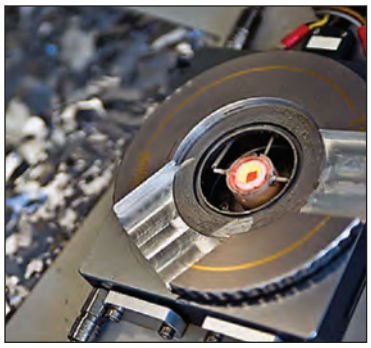
what's happening

Melting-While-Cooling Silicon Could Improve Solar Cells



Researchers at the Massachusetts Institute of Technology (MIT) have recently discovered that by dissolving certain metals into silicon, they can add that silicon compound to the relatively short list of exotic substances that exhibit retrograde melting. Their accomplishment could ultimately result in less expensive solar cells and electronic devices.

The team started by creating a "sandwich", made from two thin sheets of silicon on the outside, and a mixture of copper, iron and nickel between them. This was heated to a point that was below the normal melting point of silicon, but high enough to cause the filling to dissolve, thus causing the silicon to become supersaturated with the metals.

This means manufacturers could use less pure, less expensive grades of silicon for items such as solar cells or electronics, and purify them in the production process, the MIT team says.

— Source: MIT

Nanowick at Heart of New System To Cool 'Power Electronics'

Researchers have shown that an advanced cooling technology being developed for high-power electronics in military and automotive systems is capable of handling roughly 10 times the heat generated by conventional computer chips, according to a research paper appearing online in the International Journal of Heat and Mass Transfer. Written by mechanical engineering doctoral student Justin Weibel, Garimella and Mark North, an engineer with Thermacore, the paper will be published in the journal's September issue.

The miniature, lightweight device uses tiny copper spheres and carbon nanotubes to passively wick a coolant toward hot electronics.

This wicking technology represents the heart of a new ultrathin "thermal ground plane," a flat, hollow plate containing water.

— Source: Eurekalert

Interest in LEDs Grows as Historic Bridge, Cities Get Funding

Built in 1872 and listed on the National Register of Historic Places, the West Dummerston covered bridge in Dummerston, Vt., had been lit by high-pressure-sodium (HPS) lights until they were replaced recently by Philips Gardco LED luminaires. According to the Building Green blog, local resident, electrician and regular bridge-crosser Stan Howe led a movement to have the HPS lights replaced by LED luminaires. A photosensor automatically controls the lights on the 267-foot span, and motion sensors can dim the lights when no automobiles are present.

Meanwhile, the Massachusetts Department of Energy Resources (DOER) has awarded the city of Easthampton $174,985 for an LED streetlight project; the city of Gothenburg, Neb. is receiving a $206,080 grant for LED streetlights from the Nebraska Energy Office; and New Streetlights reported that Berwick, Nova Scotia, Canada has received CAN $101,573 to replace 234 mercury vapor and HPS lights with LEDs lights.

— Source: LED Magazine

Sony Recalls VAIO Laptop Computers Due to Burn Hazard

Sony Electronics Inc. has announced a recall of about 233,000 Sony VAIO 233000 notebook computers after it received 30 reports of the deformed keyboards and casing owing to overheating. This overheating poses a burn hazard in case the heated affected part is touched. None of the 30 reports indicated of any injuries as a result of this overheating. The overheating is caused by the malfunction of internal cooling system and protection circuits.

— Source: U.S. Consumer Product Safety Commission

[Diary Dates]

Some important 2010 events in the electronic thermal management community. Visit us online at www.electronics-cooling.com for the latest listings.

Advanced Technology Workshop and Tabletop Exhibition on Thermal Management

- **WHEN:** Sept. 28-30
- **WHERE:** Dinah's Garden Hotel, Palo Alto, Calif.
- **WHAT:** THERMINIC Workshops are a series of events to discuss the essential thermal questions of microelectronic microstructures and electronic parts in general. This year the workshop will address in addition to the "traditional" thermal management problems, also stress and thermal-stress-related-reliability issues, both in micro- and opto-electronics fields.

  INFORMATION: www.imaps.org/callfor/thermal2010.htm

16th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)

- **WHEN:** Oct. 6-8
- **WHERE:** Novotel Barcelona City, Barcelona, Spain
- **WHAT:** This workshop is organized each year by IMAPS to promote discussion of leading-edge developments in thermal management components, materials, and systems solutions for removing, spreading, and dissipating heat from microelectronic devices and systems. The workshop emphasis is for practical, high-performance solutions to meet current and evolving requirements in computing, telcom, and power semiconductor devices and systems.
- **INFORMATION:** http://cmp.imag.fr/conferences/therminic/therminic2010/

Thermal Management and Technology Symposium

- **WHEN:** Oct. 19-20
- **WHERE:** Gaylord Texan, Dallas, Texas
- **WHAT:** Thermal Management and Technology Symposium highlights the latest advancements in thermal technology for product design, system development and process management. This event will feature presentations on the latest advancements in thermal management and thermal technology for electronics packaging and cooling, thermal process control, temperature sensing and control, thermal materials, systems design and management for optimizing thermal properties.
- **INFORMATION:** www.thermalnews.com/conf_10/TN10_index.php

11th Annual LEDs 2010

- **WHEN**: Oct. 25-27
- **WHERE:** San Diego Convention Center & Hotel Solamar
- **WHAT:** The event will include afternoon tracks focusing in depth on technology topics, speakers and panels representing the whole supply chain; timely technical content from nuts-and-bolts of the LEDs themselves to application level talks, industrial trends and new product updates.
- **INFORMATION:** www.ledsconference.com/Home.aspx

Materials Research Society (MRS) Fall Meeting

Magneto Calorics and Magnetic Cooling

- **WHEN:** Nov. 29–Dec. 3
- **WHERE:** Boston, Mass.
- **WHAT:** Consisting of topical symposia, the MRS meeting offers materials researchers the opportunity to present their work, get information on up-to-the minute developments in their field, and network.
- **INFORMATION:** www.mrs.org/meetings

PowerMEMS 2010

- **WHEN:** Nov. 30–Dec. 3
- **WHERE:** Leuven, Belgium
- **WHAT**: Technical topics of interest include, energy harvesting for remote sensors and Microsystems; thermoelectric and photovoltaic materials and systems; piezoelectric, electrostatic and electromagnetic conversion; energy management and microsystem integration; and nano-structured materials for energy and thermal management.
- **INFORMATION:** http://www.powermems.org/

Third International Conference on Thermal Issues in Emerging Technologies

- **WHEN:** Dec. 19-22
- **WHERE:** Sofitel El Gazirah, Cairo, Egypt
- **WHAT:** Topics will include micro and nano-scale heat transfer, microfluidics, thermal modeling of electronic systems, temperature aware computer systems design, cooling of electronic systems and data centers, compact thermal models, thermo-mechanical effects, new and renewable energies, and more.
- **INFORMATION**: www.thetaconf.org/index.htm

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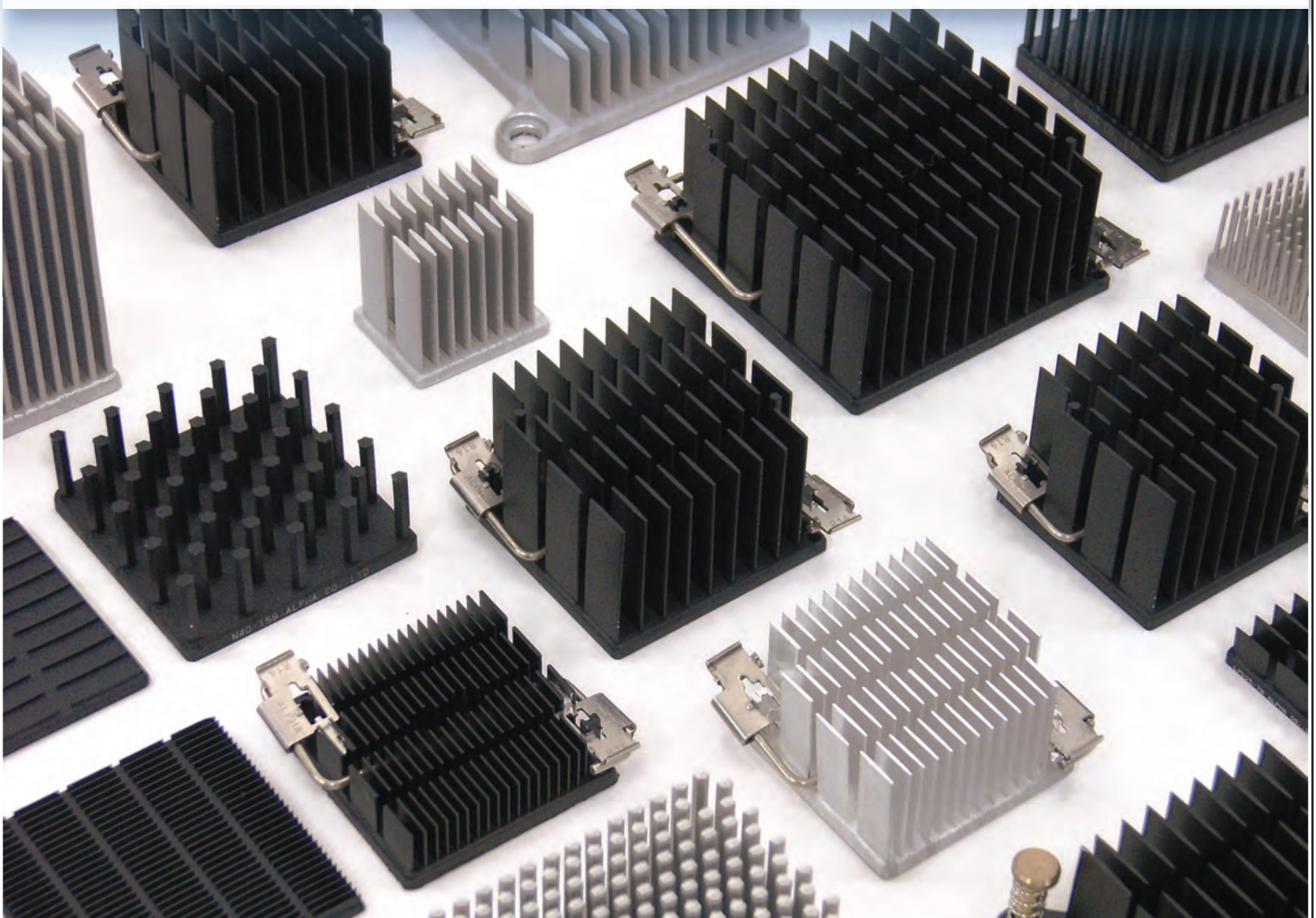

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