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The dramatic trajectory of Moore’s law has produced a number of changes in key areas of technology that are critical to our industry: 1) greater packaging and system complexity; 2) increased power dissipation; and 3) enhanced software tools and computing performance. The first two we put into the challenge category. They are the things that continually test our ingenuity and work ethic. The third one is in the solution category. There has been a dramatic growth in the computing power available to engineers. This has been accompanied by a significant evolution in the functionality and level of automation in both the design and analysis software tools and in the data exchange between them. This has changed the way we perform thermal analyses.

In previous decades, thermal analysis was performed with dramatically less computing power than is available today. Before an analysis could be performed, it was first necessary for engineers to have considerable insight into the heat transfer processes that were operative. In order to limit the required calculations to a manageable amount, it was also necessary to give priority to those calculations associated with the greatest design risk. Only then could they set up the mathematics to calculate the required outputs. The insight that this process engendered often proved to be of significant value in enabling the engineer to "size up" new designs with respect to their ability to achieve thermal performance goals. Also, their facility in performing analytical calculations supplemented their intuition by rapidly quantifying the impact of critical design features.

In today’s time-constrained, turnkey software analysis environment, there is a tendency to focus on expediting the process of importing design databases and other inputs and optimizing the computation process to maximize the production of results. This emphasis can thwart the intellectual growth of an engineer in developing a more nuanced understanding of heat transfer in a proposed design and a greater ability to assess the relative risk of different design approaches.

Without a doubt, when a thermal analysis using state-of-the-art tools is executed effectively, the end result is more accurate and represents a greater level of detail than that possible with more traditional calculation methods. However, the greater complexity of these approaches also brings with it certain liabilities. For example, they can be less efficient than traditional methods in evaluating early design concepts. Also, it can be more difficult to confirm that a complex analysis is error free. In this regard, the traditional methods, because of their simplicity, are easier to error check. They can supplement the state-of-the-art methods by providing reference solutions to aid in the detection of gross errors, such as those resulting from an incorrect input.

Since its inception, this publication has strived to present articles that provide insight into the fundamental heat transfer processes that are operative in many application environments along with the appropriate mathematics needed to characterize them. We hope that they will promote an appropriate balance in the use of simple, conceptually satisfying models and state-of-the-art computationally complex methods.

Futurists point to a time when human intelligence will be dwarfed by that of computers. Therefore, it becomes even more important that we continue to develop our capability for critical thinking in order to anticipate and manage risks that are not accounted for in computer models and that continue to grow.
Use our Talon Clip® to securely affix your heat sink. The Talon Clip® eliminates Fall Off problems.
The application of thermoelectric devices to cool electronic components has been of interest to thermal engineers for many years. Thermoelectric (TE) cooling modules offer the potential to either reduce component operating temperatures at a given heat load, or allow higher component heat dissipation at a given temperature level. Readers who are unfamiliar with TE cooling modules may be interested in several articles on the subject previously published in *Electronics Cooling* [1-5]. This article is intended to present to the reader a method to estimate the cooling performance of TE cooling modules in actual applications using readily available vendor data.

Figure 1 provides a typical example of a TE module cooling application. In this application, a TE cooling module is sandwiched between an electronic module dissipating heat and a heat sink rejecting heat to the cooling air. By passing electric current through the TE module in the appropriate direction, the side attached to the electronic module (Tc) becomes cooler, lowering the temperature of the component, and the side attached to the heat sink (Th) becomes warmer, providing a greater temperature difference for heat rejection to ambient (Tamb). In effect, the TE module “electronically” pumps the heat ( qp) dissipated by the component from the cold side to the hot side of the TE module. Of course nothing is free and the penalty that must be paid in this case is the Joule heating (qte) that takes place as current flows through the array of thermoelectric couples comprising the TE module. It should be noted at this point that, for steady-state operation, the heat pumped by the TE module must be equal to the heat dissipated by the electronic component being cooled and the heat rejected to the cooling fluid by the heat sink will be equal to the sum of the heat pumped by the TE module and the Joule heating within the TE module.

In an earlier article, Luo [5] presented the following equations for heat pumping with a thermoelectric cooling module

\[ q_p = S_m T_c I - \frac{1}{2} I^2 R_m - K_m (T_h - T_c) \]  

and the corresponding TE heat dissipation

\[ q_{te} = I S_m (T_h - T_c) - I^2 R_m \]  

in terms of the module parameters defined in the nomenclature. In addition to the above two thermoelectric equations we have the following heat transfer equations relating the TE module hot side temperature to the temperature of the ambient cooling fluid

\[ T_h = T_{amb} + (q_p + q_{te}) R_{th} \]  

where \( R_{th} \) is the heat sink thermal resistance from base to ambient. For the purposes of the calculations in this article, I have chosen to neglect the thermal interface material (TIM) resistance between the hot side of the TE module and the

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base of the heat sink, so that the temperatures at the hot side of the TE module and the base of the heat sink are the same.

Before these equations can be applied to a specific TE module it is necessary to know the values of the TE module parameters $S_m$, $R_m$, and $K_m$. These values are not provided by TE module vendors, instead vendor data sheets will usually provide the values of $Q_{\text{max}}$, $I_{\text{max}}$ and $\Delta T_{\text{max}}$ at a specified hot side temperature. However, Luo’s article developed equations which may be used to obtain the necessary TE module parameters from vendor data. These equations are as follows:

\[ S_m = 2 \frac{Q_{\text{max}}}{I_{\text{max}}} \left( \frac{1}{T_h + \Delta T_{\text{max}}} \right) \]

(4)

\[ K_m = \frac{T_h - \Delta T_{\text{max}}}{T_h + \Delta T_{\text{max}}} \cdot \frac{Q_{\text{max}}}{\Delta T_{\text{max}}} \]

(5)

\[ Z = \frac{2 \Delta T_{\text{max}}}{(T_h - \Delta T_{\text{max}})^2} \]

(6)

\[ R_m = \frac{S_m}{K_m} \frac{2}{Z} \]

(7)

It is important to note that in these equations, and in the equations to follow, all temperatures are in Kelvin temperature units (i.e., Kelvin temperature = Centigrade temperature + 273.16).

Luo used equations (4-7) to determine the module parameters for actual vendor TE modules and then input values of $I$, $T_h$, $T_c$, and $T_{\text{amb}}$ in equations (1-3) to obtain values of $q_p$, $q_{\text{te}}$, and $R_{hs}$ for comparison with values obtained from vendor software. However when considering an actual application, the value of $T_h$ is not known a priori. Typically what is known, is the allowable component surface temperature and the expected heat dissipation of the component. So, we would like an expression relating the heat pumped by the selected TE module to a specified cold side temperature, TE current and module parameters, the heat sink thermal resistance and the ambient fluid temperature. We would also like an expression relating the TE module cold side temperature to the heat pumped, TE current and module parameters, the heat sink thermal resistance and the ambient fluid temperature. The desired relationships may be obtained using equations (1-3) and a little algebra.

Substituting equations (1) and (2) into equation (3) we obtain,

\[ \eta_h = T_{\text{amb}} + \left[ S_m T_c I - \frac{1}{2} I^2 R_m - K_m (T_h - T_c) + \left[ S_m I (T_h - T_c) + I^2 R_m \right] \right] R_{hs} \]

(8)

and then solving this equation for $T_h$ we obtain,

\[ T_h = \frac{T_{\text{amb}} + \frac{R_{hs}}{2} \left( I^2 R_m + K_m T_c \right)}{1 + R_{hs} (K_m - S_m I)} \]

(9)

which may then be substituted into equation (1) to obtain equation (10) for $q_p$ as a function of the specified cold temperature, $T_c$:

\[ q_p = \frac{S_m T_c I - \frac{1}{2} I^2 R_m - K_m \left( \frac{T_{\text{amb}} + R_{hs} \left( \frac{1}{2} I^2 R_m + K_m T_c \right)}{1 + R_{hs} (K_m - S_m I)} - T_c \right)}{S_m I + R_{hs} S_m I^2 + K_m} \]

(10)

Alternatively, equation (10) may be rearranged to solve for $T_c$ as a function of the heat pumped, $q_p$, which as noted earlier equals the component heat load,

\[ T_c = \frac{T_{\text{amb}} + \frac{R_{hs}}{2} \left( I^2 R_m + K_m T_c \right)}{1 + R_{hs} (K_m - S_m I)} - \frac{q_p}{S_m I + R_{hs} S_m I^2 + K_m} \]

(11)

An example of the application of equation (11) follows. In this example we will consider a 40 mm x 40 mm electronic module with a heat dissipation of 40 W. Accordingly, a 40 mm x 40 mm thermoelectric module is chosen to be secured between the top of the electronic module and the base of the heat sink. The published vendor data for the selected TE module are:

- $Q_{\text{max}} = 83.9$ W
- $\Delta T_{\text{max}} = 72^\circ$C
- $I_{\text{max}} = 6.7$ A

Using the above values in equations (4-7) the required TE module parameters are determined to be:

- $S_m = 0.068$ V/K
- $K_m = 0.712$ W/K
- $Z = 0.002815$ 1/K
- $R_m = 0.068$ Ω

These values are then used in equation (11) to generate values of TE cold side temperature for a range of TE electric current values, three different values of heat sink thermal resistance (i.e., 0.25, 0.50 and 0.75°C/W) and a cooling fluid temperature of 30°C. The results of these calculations are...
shown in Figure 2, illustrating the benefit derived by using a TE module for this application. For example, the minimum cold side temperatures of 53.6, 36.2 and 15.2°C obtained with the TE module-heat sink combination compare quite favorably to the heat sink base temperatures of 60.0, 50.0 and 40.0°C obtained with the heat sink alone.

These results also illustrate the typical behavior at the cold side of a TE module as the electric current is increased. Initially increasing current results in lower cold side temperatures until a minimum cold side temperature is reached. After that minimum value, Joule heating will become the predominant factor and further increases in current will result in increases in cold side temperature. It may also be seen that decreasing the heat sink thermal resistance makes it possible to take advantage of increased current to achieve lower TE module cold side temperatures before the cold side temperature rises with increased current.

Another important consideration when using TE modules is the electrical power that must be supplied to achieve the desired cooling effect. A relative measure of this is the COP or Coefficient of Performance. Some readers may recall the definition of COP from their undergraduate thermodynamics course, which is the ratio of heat transferred to the work input. In this case the COP of a thermoelectric cooling module is the ratio of $q_p$ in equation (1) to $q_{te}$ in equation (2). COP as a function of electric current for the present example is shown in Figure 3. Although a slightly different COP curve resulted for each of the three heat sink thermal resistances considered, the differences were so small that only one curve is shown (i.e., for $R_{th} = 0.25$°C/W). Since the heat pumped in all cases is equal to the component heat load of 40 W, the COPs in Figure 3 indicate that the amount of power required for the TE module varies from 15.5 W at 2.5 amps to 102 W at 6 amps.

As was noted earlier, the TIM thermal resistance between the base of the heat sink and the TE cooling module was ignored in this example. However, the effect of TIM thermal resistance can easily be accounted for using the preceding equations. To account for the increase in the TE hot side and cold side temperature, the TIM thermal resistance between the TE cooler and the base of the heat sink is added to the value of the heat sink thermal resistance used in equations (10) and (11). As an example, if we consider a TIM area thermal resistance of $10$°C-mm$^2$/W, the TIM thermal resistance for the 40 mm x 40 mm module considered in the preceding example would add 0.0063°C/W to the external thermal resistance. Using a heat sink thermal resistance of 0.256 in equation (11), the minimum achievable cold side temperature of 15.2°C shown in Figure 2 would become 15.8°C.

The equations presented here should provide a useful tool for an early estimate of whether or not a particular TE module may provide useful cooling enhancement. However, the reader is cautioned to remember that these equations may not be expected to provide exact results. Inherent in the equations and derivations presented is the underlying assumption that the thermal and electrical properties of the TE module are constant, which is certainly not the case. For example, Luo's [5] comparisons with vendor’s software results showed differences in predicted heat pumping values of 3 to 11%. It is expected that similar uncertainties can exist in the method presented here.

REFERENCES

Do you know the thermal conductivity of paper? This was the start of a phone call a few years ago. The conversation continued and the reason for the question became apparent. A thermal analysis of a printed circuit board had determined that a thermal interface material was needed under some hotter components to provide a better conduction path. The circuit card was edge cooled which meant that the thermal coupling between the component and the board was significant. In the course of the design, a thermal pad material had been identified, dimensional tolerances considered, and sheets of the thermal pad material obtained that were precut to fit. The boards were assembled and because these cards were subjected to a harsh environment, a conformal coating was applied for corrosion resistance.

The question related to the thermal properties of paper became relevant when it was discovered that the individual placing the thermal pads under the parts had confused the paper and the gap pad material and had placed the paper backing where the gap pad material was designed to go and threw away the gap pad portion. The hope was that the thermal properties of the paper backing were good enough to allow the boards to be used but ultimately, the boards had to be replaced because they were not compliant to the design specifications. In fairness to the assembly person, the thickness of the pad and paper were similar.

The reason for starting this column with this type of example is that I have been asked over the years for an accuracy assessment of both predictive thermal models and thermal measurements. Answering this question nearly always requires gathering additional information, especially when reviewing the work of others. What follows are some of my personal observations related to numerical simulation and the most common sources of uncertainty in thermal model predictions. A well-documented analysis should provide the reviewer with information related to these items as well as assist the analyst with providing a credible response related to accuracy concerns.

**PHYSICAL DESCRIPTION, MOTIVATION FOR ANALYSIS**

Understanding why the analysis was performed provides a necessary basis for evaluating the need for accuracy. Revisiting the reason the analysis was performed can reveal that the larger objective was lost in generating the details.

The physical description should include the heat source terms and the information used to determine the dissipation.

If the analysis included an estimate of a convection heat transfer coefficient as a boundary condition, the accuracy of this portion of the thermal model can be difficult to assess [1] and at a minimum should have some rationale as to the applicability of the method used to predict the convection coefficient. It can be difficult to determine the range of the tested data which is needed to avoid extrapolation. This creates the risk that the situation analyzed is outside the range of applicability of the correlations, leading to excessive error.

**MATERIAL PROPERTIES**

Document the material properties and the source of the information. Adhesives and solders property data usually have wider variation. In addition, the thermal properties of adhesives and solders can vary with processing conditions which usually requires obtaining data consistent with the manner in which they will be used. *ElectronicsCooling*’s past columns on technical data provide one source of information in this area.

**DISCRETIZATION AND MESHING**

Determining that predictions are not sensitive to meshing density reduces part of the uncertainty but unfortunately, grid-density convergence studies do not seem to be the norm. It is not enough that the mesh simply represent the geometry. A simple example is provided by considering a small heat source on the surface of a rectangular shape, such as might be encountered with developing thermal models at the semiconductor die level. Resolving the surface metallization features provides a starting point for mesh density along the top surface of the die. However, there are not any geometric driven reasons for a higher mesh density through the thickness. Temperature gradients near heat sources such as FET gates are concentrated and providing an accurate solution requires a higher mesh density than would be anticipated from geometric considerations alone [2]. Given the significant computer memory and processing speed available today, performing some level of a grid convergence study is a reasonable request.

An additional source of uncertainty related to thermal models is making sure that the geometry modeled actually represents the end product. For example, layout tools used to create the geometry may be sized to yield a different feature when processed. A certain width trace in an IC database may result in a different physical width after processing. The diligent thermal analyst will check for these types of potential discrepancies.

While this list is by no means exhaustive, my personal experience is that careful attention to these items significantly increases confidence in model predictions. Having information to answer these items also makes it much easier on others to review your work as well.

*For a list of references, go to www.electronics-cooling.com*
INTRODUCTION

Silicon validation platforms are purpose-built to validate processors, chipsets, and ASICs to ensure world-class quality and reliable products. These platforms are a crucial step in the process of releasing the silicon to market. However, due to growing complexities, it is becoming more challenging to design validation platforms for high speed Quick Path Interconnect (QPI™) links based processors for rapidly increasing data and memory bandwidth applications. Typical silicon debug validation platforms are open chassis and need to allow for accessibility to all components, probing, voltage and temperature margining as shown in Figure 1. Due to multiple options of the architecture to be validated for the same program, thermo-mechanical designs may need to support several board configurations. In these platform designs, cost is equal in priority with platform features and program schedule.

The major power dissipating components that need the thermal solution of validation platforms are CPUs, chipsets, memory, ASICs and voltage regulators, as PCIE, graphic cards and power supplies have their own cooling systems. While it is becoming more challenging to remove the high heat dissipation of a multi-core silicon architecture to support the increasing bus speeds in every process generation, the keep-out volume available for a cooling solution is form-factor constrained due to more compact component placements. Elevated chip temperatures cause various problems such as increased leakage, accelerating failure mechanisms and inducing timing failures. Consequently, thermal-related effects are considered as the major roadblocks in the design of next generation microprocessors.

Most of the industrial test standards do not apply to open systems directly. The tests have to be conducted to get necessary data which may show a big difference from the data sheet provided by the vendor due to different boundary conditions. In this article, experimental methodologies of thermal tests for open silicon validation platforms are presented as shown in Figure 2. Component level thermal testing data are correlated with computational fluid dynamics (CFD) simulations to
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All this is made possible by the broad knowledge we can draw on, not to mention our endless curiosity and our care for a greener planet. With all the passion we have, we want to create proven innovations for generations to come. More information: www.livingsolutions.dsmep.com
provide guidance for system simulations. The choice of second level thermal interface materials (TIM) is implemented using the detailed thermo-mechanical test data. Acoustic tests are performed to meet acoustic safety requirements by implementing fan control to minimize system noise while still meeting thermal requirements. These experimental techniques and results have effectively guided the thermal design decisions of silicon debug validation platforms with increased capabilities while meeting budget and schedule. The test methodologies presented in this article are applicable to validation and open platforms and not for OEM systems because typical OEM systems are closed systems with unidirectional airflow.

**TEST METHODOLOGIES**

**THERMAL TEST VALIDATION AND CORRELATION**

Commercially available CFD simulation tools allow users to analyze and predict the airflow and temperature within the electronic devices or systems, which reduces the design cycle and prototyping time. However, the accuracy of the simulation results is highly dependent on the reliable input of parameters such as the boundary conditions. Therefore, experimental test data are essential for validating prototype designs that are based on optimized numerical simulations.

The majority of the heat sink designs used in open system validation platforms are of the active air-cooled type with a fan directly attached to the heat sink. Hence, a wind tunnel is not applicable to characterize these heat sinks. Instead, the active heat sinks are tested in an open air environment. The overall experimental setup is illustrated in Figure 3 (a). The thermal test vehicle (TTV) was used to simulate the actual package and the heat source. The integrated heat spreader (IHS) of the TTV and the heat sink base were embedded with type T thermocouples. Both thermocouples were connected to a data logger in which the thermocouple readings were collected. Thermal grease was applied between the TTV and the heat sink. One other thermocouple was placed above the fan to capture the local inlet temperature near the heat sink fan. Figure 3 (b) shows the thermal resistance network from the TTV case to ambient.

Each prototype was tested for a range of power dissipation levels. The performance characteristic of the active heat sink is defined by the thermal resistance from case (IHS) to local ambient (Ψ_ca). Ψ_ca is obtained from the slope of the fitted line between the package case temperature rise (Tc – Tinlet) and different power levels. Ψ_ca is used since there is a significant secondary heat flow path to ambient [3]. Figure 4 summarizes the Ψ_ca values for heat sink samples. The mean case to ambient thermal resistance for the tested active heat sinks is 0.179°C/W with 3σ of 0.033°C/W.

The actual CPU case temperature can be calculated for certain ambient temperatures and power loss based on the mean plus three sigma of the Ψ_ca. The validation approach is to perform a correlation between simulation results and the experimental data. With the test data, the heat sink numerical thermal model can be validated accordingly. The numerical model built using a CFD tool included the details of the active heat sink including heat pipes, the TTV (including the substrate, die, TIM1, IHS), TIM2 between active HS and IHS, the socket, and the test board as shown in Figure 3(c). The heat sink fan was modeled with the fan curve and the air flowing from top to bottom. All the boundaries around the model were open conditions with no duct or chassis.

System level thermal simulation is always more complex due to the number of components in the system and the mutual preheating effect among the components. The airflow in closed systems is usually designed flowing in one direction. However, there is no unidirectional airflow pattern in an open chassis. The system fan is usually designed to cool memory, the passive heat sinks for ASICs and voltage regulators in the
system. The CPU and chipset typically have an active heat sink due to their higher power dissipations. With system fan air flowing in one direction while the active heat sink air is impinging through the active heat sink fins, there is no simple way of predicting the airflow pattern and temperatures of the heating components in the system. Thus, numerical modeling provides quick and predictable results for such a complex system. The component level active heat sink thermal model is correlated to experimental results and then the correlated model is used in open system level thermal simulations for studying the mutual effect among the components around the CPU heat sink.

**TEST VALIDATION OF THERMAL INTERFACE MATERIAL**

The thermal interface material (TIM) used in a silicon validation platform should have characteristics such as
(i) high thermal conductivity, (ii) ease of rework and application, (iii) electrical inertness, (iv) ability to spread well under pressure, (v) ability to fill air gaps, and (vi) long-term reliability since validation customers need to swap the processors frequently during the validation and debug tests. In addition, a TIM with a lower adhesion force is preferred in order to avoid the processor/chipset being pulled out from the socket when removing the heat sink.

There are many TIM choices available in the market ranging from gap pad fillers to phase change materials (PCM) to thermal greases. Thermal greases generally have high thermal conductivity, are easy to replace, and hence, are recommended for the TIM used on a CPU heat sink for the validation environment [1, 2]. Though data sheets provided by vendors are good reference to evaluate the TIM properties, there is no particular parameter in the data sheet or the test data provided by vendors that specifies the adhesion force of the thermal grease. Therefore, adhesion force test, discussed below, helps in quantifying the adhesive strength of the thermal grease under test. A TIM with the lowest adhesion was selected and evaluated for its thermal performance, then checked for its reliability through thermal performance testing and high temperature testing.

In the validation environment, the adhesive bonding strength of the TIM is critical to support the usage model of silicon insertion/extraction. Once the adhesion force exceeds the retention force of the package, the processor will be pulled out from the socket during heat sink removal. This may cause damage to the package and the socket and eventual damage of the validation boards. The test setup shown in Figure 5 is required to understand how the TIM will behave when subjected to tensile forces during heat sink removal. The grease under test was applied on the TTV. A compressive force was
first applied on the thermal grease by tightening down the retention screws on the active heat sink to ensure a good contact with the processor and the heat sink. Then, the heat sink screws were loosened. The breaking load was gradually increased to remove the heat sink until the joint ruptured. A digital force gauge was hooked onto the heat sink to measure the peak force during the heat sink removal.

Thermal performance of the TIM is a critical factor for the overall thermal management of the silicon. The test setup for the thermal performance studies completely followed the experimental setup described in the previous section on component level thermal test validation. The mounting screws for the heat sink were fully tightened at all four corners to ensure a uniform load on the thermal grease. Steps were repeated and the grease was cleaned and re-applied each time a different grease was tested. To ensure our test results were as accurate as possible, tests were repeated for each grease under test.

Reliability of the TIM is critical for providing stable and reliable thermal performance throughout the lifetime of the validation. The TIM used on CPU heat sinks needs to pass the high temperature test to avoid hardening and pump-out issues that could lead to overheating of the processor. In this test, the TTV was subjected to maximum CPU power dissipation and the TIM was subjected to 90°C for 24 hours to study the performance change of the TIM. Note that the adhesion force was measured at room temperature right after being subjected to 90°C for 24 hours. Figure 6 illustrates that the grease’s thermal performance and adhesion force decreased after being subjected to high temperature due to viscosity reduction. Grease F was chosen for the validation environment since it provided the best thermal performance with the least adhesive force as shown in Figure 6.

**ACOUSTIC TESTS**

High cooling power and an open chassis system for the validation platform drive the selection of high-speed fans causing undesirable acoustic noise. The acoustic data provided by the vendor for an individual fan is collected 1m away from the fan with the background noise of 15dBA. This does not provide the system acoustic data for each validation platform running in the realistic lab environment. Therefore, acoustic experiments are required: i) to select fans ii) to implement fan control, iii) to meet thermal/airflow/safety requirements, and iv) to enhance user experience. The industrial test system safety guideline [4] states that system noise should be less than 85 dBA at 1m away from a single system.

Experiments were performed at both component and system level to quantify the dominant source of the noise. Noise measurements were recorded in all directions using a handheld digital sound meter for design guidance and are not official tests with the acoustic test chambers.
Experiments were repeated to collect data from 0.0762m to 1.016m at the highest noise direction including the background noise. It was found that the system fans contributed to the noise most. Then, fan control experiments were performed to quantify the system noise reduction while still meeting all the thermal requirements. CFD simulations shown in Figure 7(a) indicate that fan speed can be reduced to ~80% to 40% based on different usage configurations. Fan control experiments show ~4 to 12 dBA noise reduction as shown in Figure 7(b).

SUMMARY
Experimental methodologies of thermal, TIM and acoustics are presented to design the open chassis validation platforms efficiently and reliably while meeting the shorter design cycle time and increasing complexities of the platforms. Component level thermal testing data are correlated with CFD simulations to provide guidance for system simulations. The choice of TIM2 was implemented using detailed thermo-mechanical test data. Next, the acoustic tests were performed to meet acoustic safety requirements and to implement fan control to minimize system noise. These tests provided guidance to validate the thermal designs and to drive design decisions before availability of new silicon. This helps in increasing the confidence level of the platforms delivered, and identifying design issues/failure modes not captured by the analyses.

REFERENCES

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INTRODUCTION

Today’s marketplace consists of many portable computing devices such as personal digital assistants and smart phones. Currently over one billion handset type units are shipped every year. The functionality and power levels within these devices continues to increase causing additional thermal management issues, which will require active cooling solutions in the future. For active cooling in such devices small scale fans will be needed to remove the heat generated, and hence much work needs to be undertaken at this scale[1]. Key issues are cost, acoustics[2], reliability, fan design [3] and cooling efficiency. There are numerous cooling solution designs where fans are placed directly over heat sinks resulting in an impingement type flow field. Currently there is a lack of understanding of the emerging flow field and the resulting local heat transfer rates on the target surface. The influence of motor supports is particularly important for small scale fans as the motor supports do not scale with reducing fan dimensions as can be seen from the small scale fans in the marketplace today. This article demonstrates that the emerging flow and resultant local heat transfer rates from an axial fan are dependent on motor support design and placement. This finding suggests the need for integrated designs of fan-heat sink cooling solutions as suggested previously for radial flow fans [4].

EXPERIMENTAL TECHNIQUE AND FAN

The direct measurement or calculation of local heat transfer coefficient is achieved using the infrared thermography and heated-thin-foil technique. The heated foil is a thin (12.5µm) stainless steel foil that has a constant heat flux boundary condition. The conduction within the foil, radiation and natural convection are accounted for using a technique developed by the current authors[5]. Figure 1(a) illustrates the fan employed in the study and also the experimental setup that is utilised in Figure 1(b). For all experiments the fan rotates at 9,000RPM and is parallel to the thin foil at a distance of 5mm, resulting in flow impinging directly on the foil. The IR camera detects a temperature distribution, which
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may then be converted to a local heat transfer coefficient, which is of interest to the thermal designer.

The work considers three limiting conditions of motor support designs on a commercially available small scale fan. Firstly, the motor supports are placed at the flow exit side of the fan, which is the most common in electronics cooling; secondly the motor supports are placed at the inlet to the fan and finally a fan without any motor supports and powered by an auxiliary motor is implemented. In the latter the fan and housing are identical to figure 1(a) with motor supports removed.

RESULTS

Figure 2(a) to (d) shows the calculated heat transfer coefficients from the measured temperature fields using the setup of Figure 1. Case (a) demonstrates the influence of the motor supports at the exit of the commercially available fan when used as intended by the manufacturer. In this case six zones are clearly identified caused by the interaction between the exit flow and the motor supports. Interestingly, the peak heat transfer coefficient of these six zones is \( \sim 130 \text{W/m}^2\text{K} \), while on the same circumferential radius the heat transfer coefficient reaches values of \( \sim 60 \text{ W/m}^2\text{K} \). Directly under the motor the heat transfer coefficient is further reduced. This indicates the importance of placement of motor supports relative to any particular location that needs to be aggressively cooled. Case (b) shows the influence of placing the same motor support structure at the fan inlet. Similar to case (a) high heat transfer zones are identifiable, but a more uniform annular type heat transfer coefficient is evident. Case (c) illustrates the resultant local heat transfer coefficient when the motor supports are removed, and a well ordered annular type jet flow is evident, which is symmetric about any line drawn through the centre. Moreover, the peak heat transfer coefficient is now \( \sim 140 \text{W/m}^2\text{K} \).

The circumferentially averaged local heat transfer coefficients of cases (a), (b) and (c) are shown in Figure 2(d). The influence of the motor supports on this averaged heat transfer is dramatic, where a 20% increase is measured in the region of the annular jet. Although the gains of 20% may not be possible due the practical necessity of requiring some motor supports for this type of fan arrangement, reducing the size and placing the supports at the inlet provides some improvement in the heat transfer coefficient. Such an approach would allow any given fan to run at a lower speed resulting in increase reliability combined with reduced power consumption and acoustic levels for the same cooling requirements. Alternatively, it could allow higher heat dissipation for the same package temperature when operating at the same speed. Hence this is a simple, cost effective approach, to improving the thermal management of devices where significant gains are attainable for minimal effort.
CONCLUSIONS
Although the influence of motor supports on the thermal performance of an axial flow fan is rarely considered, it is shown here to be important, with heat transfer coefficients increasing by up to 20% for different designs. Placing the motor supports at the inlets provided a small enhancement in heat transfer coefficient, while removing the motor supports completely resulted in greatly improved performance. Therefore the motor supports should be kept as small as possible and placed at the inlet of the fan to provide enhanced thermal performance. Furthermore, this result should be taken into account when designing heat sinks with an impingement cooling methodology, as it indicates that the design of a repeating fin matrix at the exit of an axial flow fan may not be optimum. Further work linking the fan designs and heat sink cooling surfaces needs to be undertaken.

REFERENCES

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INTRODUCTION

One of the key power generation technologies in the current “green” revolution is the solar photovoltaic cell (SPVC). This unit directly converts solar energy into useful amounts of electrical energy in an increasingly economically-efficient manner. But the SPVC is not a new device – in semiconductor device terms, it is just a diode, and has been around for many decades. The newness of the SPVC lies in the increased energy conversion efficiencies and the ability of industry to find ways to lower the manufacturing and implementation costs while improving the performance and reliability. A key element in the performance and reliability improvements has centered on better control of the cell’s junction temperature.

Even though a thermal measurement standard specific to the SPVC does not currently exist, the fact that it is “just a diode” provides implementation of existing measurement standards for both junction temperature and thermal resistance. This measurement capability is necessary for gauging the effectiveness of manufacturing and implementation techniques intended to better control junction temperature.

SPVC TYPES

There are several different technologies that can be used to directly convert solar energy into electricity [1]. However, the discussion herein will be limited to two of the most common semiconductor junction technologies – the Single Junction SPVC (SJ-SPVC) and the Multi-Junction SPVC (MJ-SPVC). The SJ-SPVC devices are made from silicon or germanium and are usually made by the normal semiconductor manufacturing process. This results in chips – which may be as large as 200 mm square for silicon chips and up to 100 mm square for germanium versions. These chips are mounted in the normal semiconductor fashion – either with eutectic, soft solder, or epoxy – to a mounting surface that acts as the “package.” The Multi-Junction SPVC (MJ-SPVC) devices are actually three diodes in series, all implemented in one chip. The chip material is usually a III-V compound with three different sets of junction materials. Each junction is “tuned” in for a different solar energy wavelength range using the
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bandgap associated with the different material combinations. The electrical equivalent circuits for these two types are shown in Figures 1 and 2, respectively.

The leakage and series resistances, junction capacitance, and ideal diode shown in the SJ-SPVC equivalent circuit are the circuit elements usually shown for just about any diode. The conductor resistance and capacitance elements are also common to diodes in general but can usually be neglected in most cases. But these cannot be neglected in the SPVC case because the conductor is relatively long, typically traveling across the whole cell, and because of the high currents involved. For reasons discussed below, both of these elements impact the measurement of SJ-SPVC thermal performance.

The MJ-SPVC equivalent circuit for these devices is similar to that shown in Figure 1, except that each junction has its own \( R_{\text{leakage}} \), \( R_{\text{series}} \), \( C_{\text{junction}} \), and \( D_{\text{ideal}} \); and the three junctions are all connected in series. Because the three junctions are made from different materials, the circuit elements for each series diode will be different from the other junctions in the stack. It is important to note that even though there are three distinct diodes in the stack, direct access to an individual diode is not present.

**PERFORMANCE LIMITERS**

A key measure of SPVC performance is the cell’s ability to convert incident solar energy (i.e., light) into electrical energy. Commercially available SPVC modules currently offer conversion efficiencies in the range of 12% for SJ and 28% for MJ units. The maximum theoretical conversion efficiency (about 30% and 68%, for SJ and MJ types, respectively) is determined by the Shockley–Queisser limit that deals with the amount of photon energy that can actually be converted into electrical energy [2]. The theoretical limit is not reachable because of the following key performance limiters:

**Semiconductor Processing Limitations:** The object of solar photovoltaic cells is to collect as much solar energy (i.e., light) as possible and convert that energy into electrical energy. By definition then, SPVCs are made as large as reasonably possible for both single and multi-junction cells. The large junction areas for either type make each susceptible to wafer fabrication defects. Defects that may not render the cell useless but will reduce the conversion efficiency and potentially cause hot spots on the cell.

**Conductor Series Resistance:** The backside conductor usually is not a problem because of its large area and it is out of the light path. However, the top conductor series resistance affects performance in two ways. First, a portion of the electrical energy generated by the photovoltaic diode is converted into Joule heating. This increases localized junction temperature and degrades the cell output. Second, the voltage dropped across the conductor reduces the output voltage, and hence the power, available as the cell’s output, thus reducing the cell conversion efficiency even further.

**Conductor Shadowing:** The natural tendency, based on the conductor series resistance issues above, is to increase the size of the conductor or use more conductors to reduce the resistance. However, any increase in the width of the conductor or the number of conductors will increase the shadowing of the cell’s active area, which will in turn reduce the conversion efficiency as well. Increasing the conductor thickness does help but also introduces manufacturing issues.

**Junction Temperature:** Like all diode devices, the junction forward voltage under given current flow decreases with junction temperature. As shown in Figure 3, the SPVC has a near constant current output up to some voltage that is temperature dependent. The higher this voltage for a given current, the higher the power output of the cell. Thus, maintaining the lowest possible junction temperature maximizes the power conversion efficiency and the electrical energy output. Although this generic I-V curve shown is for a SJ-SPVC, the temperature dependency for a MJ-SPVC is very similar, with the voltages about three times higher.

Three out of four key limiters directly impact overall SPVC
performance through temperature effects, thus making the lowest possible junction temperature maintenance paramount.

**INCIDENT POWER**

SPVCs are unique in the diode family when the source of the power dissipation is considered. Most diodes have internal power dissipation resulting from the application of external energy to the device. The SPVC has little internally generated power dissipation but a lot of incident externally-sourced power dissipation. However, some of the incident power is converted to electrical power out, thus reducing the thermal impact.

One sun, a term used in the solar photovoltaic industry to describe the incident power, is approximately 1,000 W/m², or 0.1 W/cm² [3, 4]. A concentration ratio of 100 suns, obtainable by using optical lens [5] or mirrors [6], would provide a power density of 100,000 W/m² or 10 W/cm². Applying these values to SPVC power dissipation considerations produces interesting results. The SJ-SPVC typically operates with 1 to 10 times the incident solar power, while the MJ-SPVC operates with much higher concentration values – 50 to 1000 times. Figure 4 shows the magnitude of the incident power for concentration ratios and for different cells.

For example, consider a 150 mm X 150 mm silicon SJ-SPVC operating at one sun would have about 22.5 W incident and about 19.8 W in thermal power assuming 12% conversion efficiency. Similarly, a 25 mm X 25 mm MJ-SPVC operating at 100 suns would have about 62.5 W incident and about 45 W in thermal power assuming 28% conversion efficiency. Power densities for these cases are 0.088 W/cm² and 7.2 W/cm², respectively. This thermal power is what the SPVC system, consisting of the cell and its mounting environment, has to properly dissipate to keep the cell junction temperature in the desired operating range.

**THERMAL MEASUREMENT**

As a diode, the SPVC of either type can use the same measurement methods applicable for standard diodes, provided that the unique attributes of the SPVC devices are properly taken into account. The basics of diode thermal measurement are to use the diode junction for both to measure the junction temperature and to cause power dissipation in the device [7, 8]. For optimum measurement accuracy, the VF is measured at low current values, sufficient to turn the junction on but not so high as to cause significant self-heating within the junction. These requirements usually translate into keeping the measurement current (IM) to less than 1% or 2% of the current applied for heating purposes – i.e., the heating current (IH). With the diode supplied with the proper IM and subjected to an environmental temperature change, as in a temperature-controlled test chamber, the VF – TJ will be basically linear over the normal temperature range of roughly 0º C to 150º C. The reciprocal of this line’s slope is referred to as K Factor (or just K) with units of ºC/mV.

For a given value of IM, typical K values...
for silicon single junction devices are in the 0.45°C/mV range and for III-V compound material multi-junction devices in the range of 0.60°C/mV. K at a specific IM must be determined for each group of devices to be measured to obtain the most accurate thermal measurements possible.

The Electrical Test Method (ETM) concept is to use the diode junction(s) both to cause power dissipation in the device and to determine the junction temperature. The basic thermal measurement circuitry (Figure 5) consists of two current sources, one for IM and one for IH, a high speed electronic switch to alternate between the two current sources, and a measurement circuit that can measure the voltage across the DUT at specific times. Figure 6 shows the waveforms this setup produces to generate the data results necessary to calculate both TJ and thermal resistance from the device junction to some reference point - ΘJX.

The only difference between measurements of SJ versus MJ-SPVC is that the Vf values are typically two or three times larger for the latter as compared to the former. This measurement setup produces a value of ΔVf – the change in Vf, from the initial thermal equilibrium state (Vf_i) to the steady-state condition when the heat has propagated to the desired reference point (Vf_f). Thus, T_i is the initial TJ at thermal equilibrium before the start of the measurement and the subscript X defines the reference condition in which the measurement is made.

There are two important aspects of the measurement that must be taken into account:

1. The junction begins to cool down the instant the heating power is removed from the device. If this is not accounted for in the measurement, then resultant measurement values will not represent the peak value of TJ.

2. The second is the fact that charge stored in the SPVC junction(s) may not recombine fast enough so as to not perturb the Vf_f measurement. The effect is that the junction appears heavily “turned-on” for some appreciable time after the heating current has been removed, thus delaying the Vf_f measurement. This problem occurs mostly with silicon cells but sometimes with III-V compound cells as well.

Methods for dealing with these measurement issues to obtain a more accurate peak junction temperature value are available in the literature [9, 10].

MEASUREMENT IMPLEMENTATION
Thermal measurements require a reference point. Figure 7 shows the MJ-SPVC chip sitting on material that acts as a heat spreader and/or an interface that absorbs mechanical stresses due to mismatched coefficients of thermal expansion between the chip and the substrate. The chip through the substrate is considered a package. Junction-to-Case thermal resistance is then from the chip junction to the center bottom side of the substrate, and includes all the materials and interfaces within the package. A plot of the junction temperature change versus the length of time external electrical heating power is applied to the junction will produce the curve shown in Figure 8. Under the proper set of circumstances, each material element in the heat flow can be identified on the curve. However, getting an accurate estimate using the transient response curve is by no means trivial, and a...
A proposal to solve this issue is currently being prepared by the JEDEC JC15 standardization committee. In this example, the large step between the heat spreader plateau and the substrate plateau indicates a poor attachment of the heat spreader to the substrate. The $\Theta_{JC}$ value can be calculated using the equations given above for the $\Delta VF$ value at four seconds.

Similar measurements implemented on direct-mounted SJ-SPVCs produce data that are harder to interpret because of the much larger “chip” and, typically, the comparatively huge heat sink mass. However, this does not negate the need for the measurements. But larger values of $I_{IP}$ typically two to three times the chip’s normal current rating, will be necessary to see the different elements in the heat flow path.

CONCLUSIONS

SPVC devices are unique in that, unlike most other semiconductor devices, the thermal power they must handle is not primarily internally generated but rather incident on the device surface and junction area.

SJ and MJ SPVC devices can be treated as a diode for thermal measurement purposes provided the distinct characteristics of each device type are properly addressed. While no industry-wide, SPVC-specific standard currently exists for these measurements, there are several existing diode thermal measurement standards that are applicable.

Further improvements in SPVC performance and reliability will be greatly influenced by thermal considerations. And having a way of validating thermal management designs will play a big part in future SPVC technology advances.

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Mitsubishi Adds LED-Based Cube to Display Wall Line-up

Mitsubishi Digital Electronics America's Presentation Products Division has expanded its SeventySeries display wall line with the SeventySeries: LED, an LED-based, rear-projection display wall cube designed specifically for control and command rooms for government, traffic and utility facilities, and network operations centers.

Mitsubishi's latest LED light source DLP® engine incorporates the company's Smart Seven Technology and other features that use next-generation technology to provide better reliability and brightness.

Applying Mitsubishi's control room expertise to new applications, its LED engines offer:

- **Pumpless Design**: Keeping LEDs cool is critical. Some manufacturers use a pump-driven water cooling system which can lead to mechanical difficulties. Mitsubishi's SeventySeries: LED displays cool its system with unique heat pipe technology and a 100K-hour cooling fan to help ensure reliability and reduced maintenance.

- **LED-Calibrated Automatic Brightness and Color**: Mitsubishi's new SeventySeries: LED engine uses Mitsubishi's automatic color control to ensure optimal brightness and color uniformity across the wall. This new generation color space control is optimized specifically for LED illumination sources, enabling ideal image quality throughout the display's lifetime.

- **Mitsubishi uses a proprietary power driver for its LED, allowing three power modes: bright, normal and ECO. ECO mode provides optimal power consumption and increases the lifetime of the LED.**

- **Easy Upgradeability**: Mitsubishi's SeventySeries: LED engine is compatible with all Mitsubishi SeventySeries cabinets and screens for an easy and cost-effective upgrade with minimal disruption. Users simply replace the optical engine instead of purchasing a whole new cube cabinet or screen.

New Cooling Technology Materializing the High Brightness Compact Projector

For the competition in the projector market, a compact and lightweight body becomes one of the important factors for selection, as well as high brightness and high resolution, for expanding the mobile use of projectors. However, the high brightness factor has a reciprocal relationship with the factor of a compact and lightweight body, since a high power lamp is generally required to achieve high brightness and then a large-sized cooling system is required for the high power lamp.

NEC Display Solutions Ltd. applies the small-sized air pump while improving cooling efficiency by reducing the packaging density in the unit, so that the size of the cooling system can be reduced to achieve higher brightness and a more compact body for the projector.

The spot cooling within the unit using a high static pressure and small-sized sirocco fan and the air duct. With the new cooling system, about 75 percent of the airflow required...
in the ordinary unit is sufficient for cooling the unit.

- Cooling for the power supply: In the ordinary power supply, the heat sink for cooling is installed on the side where circuit board components are packaged. Thus, electric components installed close together interfere with the airflow sent to the heat sink part, then the cooling efficiency for the heat sink deteriorates. We install only some electric components generating a large amount of heat and the heat sink on the backside of the circuit board to improve ventilation efficiency and cooling efficiency.

- Cooling for the DLP(R)chip: In an ordinary projector, the heat sink for cooling is installed on the backside of the DLP(R) chip, which is the display device for the DLP(R) projector and it radiates heat. We introduce a configuration where another heat sink for cooling is installed on the top side to radiate heat from the top side as well. With this configuration, the temperature of the DLP chip has been reduced by 5%.

- Cooling for the housing: Since the lamp becomes very hot in an ordinary projector, the temperature of the exhausted air is very hot. Sometimes it reaches temperatures of around 90°C. Since the exhaust grid part (resin materials) is exposed to this hot air, it becomes very hot as well. In order to cool this exhaust grid part, we provide metallic materials on the inner surface of the exhaust grid to diffuse heat on the grid. With this arrangement, the temperature can be reduced by around 30%, so that it can be cooled with a small amount of airflow.

Source: NEC

Air Houses for Aerospace and Automotive Assembly

Aerospace and other highly controlled manufacturing processes require large volumes of filtered, temperature and humidified controlled air. Thermal Engineering Corporation TEC® has developed Air Houses that meet this demand. The original concept was used in pharmaceutical manufacturing and automotive painting operations.

Thermal Engineering Air Houses have the ability to maintain temperatures at +/-3º F, +/-5% RH; sustaining consistent air quality in extreme climate conditions. We have installed air houses in the Imperial Valley desert of Mexico where
temperatures reach 127º F and humidity in single digits. TEC has also supplies equipment into climates that require large amounts of dehumidification e.g. South Florida.

The air volume of these units, range from 10,000 CFM to 150,000 CFM. They are made of structural steel and insulated walls. Outside mounted units have synthetic membrane roofs and electric heaters to prevent freezing when off line in cold climates. Each section of the air house comes with its own man door and lighting for maintenance and service work. Sections provide heating, cooling, filtration, humidification, and dehumidification.

Thermal Engineering Corporation, established in 1961 is a custom manufacturer of finishing systems for a wide range of painting, coating & filtration applications.

High-Accuracy 2.25 V Digital Temperature Sensor

Extreme Engineering Solutions (X-ES) in Middleton, Wis., is introducing the 8.8 pound XPand4200, a sub-half-ATR, forced-air-cooled enclosure for conduction-cooled modules for embedded computing in vetronics and avionics applications in unmanned aerial vehicles (UAVs), helicopters, fixed-wing aircraft, armor vehicles, and unmanned ground vehicles (UGVs).

Electronics thermal management in the XPand4200 conducts heat from conduction-cooled boards to heat exchangers, where the heat is dissipated to the ambient environment by forced-air cooling. The design supports conduction-cooled boards in an air-tight enclosure, and provides enhanced shock and vibration protection and isolation of the boards from the outside environment.

The XPand4200 is designed to reduce the size, weight, and power (SWaP) of deployed military systems. A populated XPand4200 weighs less than 15 pounds and can accommodate many as six conduction-cooled, 0.8-inch-pitch 3U VPX or 3U CompactPCI X-ES single-board computers or power supply modules, and the XPand4200 can be configured with custom I/O with conduction-cooled PMC or XMC modules from X-ES or from other companies.

The XPand4200 has an optional removable memory module attachment that supports the XPort6191 solid state disk (SSD) removable storage module, with 64 gigabytes of storage capacity. The unit supports Gigabit Ethernet, graphics, RS-232/RS-422, MIL-STD-1553, ARINC 429, as well as custom conduction-cooled PMC/XMC I/O through D38999 circular connectors.

Fan and Filter Units Prevent Hot Spots

Rittal’s TopTherm fan-and-filter units are a synthesis of radial and axial fan technologies that deliver a combination of high pressure stability and large volume air flows.

Unique to this fan technology, the air outlet direction is diagonal to the outside rather than in the fan’s axial direction. This approach favors an even distribution of air in the enclosure or housing, and avoids the formation of hot spots.

Electronics Cooling for Military Environments

Allen Vanguard’s Electronic Protection with Integrated Cooling (EPIC) is a customized E-cooling system that protects electronic systems from the severe heat and harsh operating environments found in military environments, including vehicle electronics. It complies with MIL-810-F (Shock and Vibration) for tracked and wheeled vehicles. The EPIC Micro Climate System (MCS) provides electronics cooling in ambient temperatures up to 170°F (77°C). It also protects against dust, sand, vibration, humidity and liquid threats. The system is compatible with vehicular and aircraft applications.

Source: Extreme Engineering Solutions

Fan and Filter Units Prevent Hot Spots

Source: Rittal

Electronics Cooling for Military Environments

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Nanotech Yields Major Advance in Heat Transfer, Cooling Technologies

Researchers at Oregon State University and the Pacific Northwest National Laboratory have discovered a new way to apply nanostructure coatings to make heat transfer far more efficient, with important potential applications to high-tech devices as well as the conventional heating and cooling industry.

These coatings can remove heat four times faster than the same materials before they are coated, using inexpensive materials and application procedures. The discovery has the potential to revolutionize cooling technology, experts say. The findings have just been announced in the International Journal of Heat and Mass Transfer, and a patent application has been filed.

For the configurations investigated, this approach achieves heat transfer approaching theoretical maximums, said Terry Hendricks, the project leader from the Pacific Northwest National Laboratory.

The improvement in heat transfer achieved by modifying surfaces at the nanoscale has possible applications in both micro- and macro-scale industrial systems, researchers said. The coatings produced a “heat transfer coefficient” 10 times higher than uncoated surfaces.

The journal publication this story is based on is available online at http://bit.ly/cBAKfE.

— Source: Oregon State University

Phoenix a Hot Spot for Data Centers

Metro Phoenix is becoming a haven for data centers, as one large local data center recently announced it would expand and another opened on June 18. Digital Realty Trust, a real-estate trust that specializes in data centers, said in March that a study showed 83 percent of large corporate data users plan data-center expansions over the next 12 to 14 months. Arizona is a perfect place for data centers for a number of reasons, experts say, including its cheap and redundant power sources and safe location. A study by Risk & Insurance magazine in late 2008 shows Phoenix is the second-safest metro area of more than 1 million people for the centers. The magazine noted that compared with other locations, the area has a low risk for terrorism and for natural disasters, such as hurricanes, earthquakes and winter storms. The area ranked in the medium category for severe thunderstorms and wildfires.

— Source: The Arizona Republic

ENERGY STAR Launches Data Center Energy Efficiency Initiatives

The U.S. Environmental Protection Agency has launched its Energy Star program for data centers, meaning companies can start applying today to see if their facility qualifies for an Energy Star logo. Data centers can now earn the Energy Star label seen on TVs, refrigerators and computer monitors. To qualify, data centers must be in the top 25 percent of their peers in energy efficiency, according to EPA’s energy performance scale.

In an effort to assist data center operators wishing to assess the energy efficiency of their facilities, eight leading organizations that set or use data center energy efficiency metrics met on Jan. 13 in Washington, DC. The outcome of the meeting is an agreement to three guiding principles for measuring energy efficiency in data centers at the present time. These guiding principles are meant to help the industry have a common understanding of energy efficiency metrics that can generate dialogue to improve data center efficiencies and reduce energy consumption. Each of the participating organizations has agreed to promote these guiding principals to their members and stakeholders in an effort to bring uniformity to the measurement of data center energy efficiency, while the dialogue continues to advance existing metrics.

— Source: Energy Star
Liquid Cooling Making a Comeback

Although it’s not without its challenges, liquid cooling has become the focus of recent research thanks to its efficiency.

As a start, chilled liquid cooling has been reintroduced into high end mainframes and densely packed servers. IBM believes such an approach has major benefits as it could cut data center energy consumption by up to 50 percent and allow the use of the collected thermal energy either for district heating or industrial applications, significantly improving the system’s green credentials.

At the beginning of May, with its partner the Swiss Federal Institute of Technology (ETH) Zurich, IBM introduced a new supercomputer, the Aquasar, an entirely new, water cooled machine that will also supply heat to university buildings.

A July article in New Electronics magazine explores this and other liquid cooling research that has gained new interest as electronic equipment generates more and more heat.

— Source: New Electronics

Data Center-in-a-Box Launched in India

Elliptical Mobile Solutions (EMS) has launched its full range of data center-in-a-box products. These vendor neutral, high-density, self-contained data centers include the R.A.S.E.R., a full-height (42U) MMDC, the C3.S.P.E.A.R., a half height (24U) MMDC and the S.P.E.A.R, also a half-height, armored (22U) MMDC. The Data Center-in-a-Box technology provides more than 50 percent savings in data center cooling costs due to EMS patented Closed Loop Cooling technology, enabling users to substantially reduce their overall energy consumption, according to EMS.

— Source: India Tech Online

Engineer Honored for Contributions to Thermal Research

Binghamton University faculty member Bahgat Sammakia received the 2010 ITherm Achievement Award during the 12th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems in honor of his contributions to electronics, thermal and thermomechanical research, as well as his service to the electronics thermal management community. Sammakia, director of the Small Scale Systems Integration and Packaging Center, a New York State Center of Excellence, also serves as BU’s executive director for economic development. Sammakia, a longtime IBM engineer, joined Binghamton’s faculty in 1998. He holds 14 U.S. patents and has published more than 150 technical papers in refereed journals and conference proceedings.

— Source: Binghamton University

Heat Conducting Graphene Could Cool Electronics

Multiple layers of graphene show strong heat conducting properties that can be harnessed in removing dissipated heat from electronic devices, a team of scientists from the University of California reported in a recently published paper in the journal Nature Materials. Having previously shown that graphene — a two-dimensional layer of carbon atoms packed in a honeycomb structure — behaves as a strong heat conductor, the group tested a solution in which multiple sheets of graphene embedded within silicon chips can dramatically improve the thermal characteristics, meaning lower temperatures and a concrete possibility for chip manufacturers to reach higher processing speeds with relative ease.

— Source: Nature Materials
International Heat Transfer Conference (IHTC-14)

- **WHEN:** Aug. 8-13
- **WHERE:** Omni Shoreham Hotel, Washington, D.C.
- **WHAT:** This year marks the first time IHTC will be held in the United States since 1986. The IHTC aims to provide a technical forum that includes keynote lectures, poster sessions, professional development courses, and a live exhibit of heat transfer equipment, services, and publications. In addition to the fundamentals of thermal phenomena and traditional thermal applications, the IHTC is expected to address the emerging domains of thermal transport in nano-materials, bio-systems, Power Generation, MEMS, Microsystems, information systems, energy conversion devices, aerospace and hostile environment systems.
- **INFORMATION:** [www.asmeconferences.org/IHTC14/](http://www.asmeconferences.org/IHTC14/)

2010 Thermal and Fluids Analysis Workshop

- **WHEN:** Aug. 16-20
- **WHERE:** NASA Johnson Space Center, Houston, Texas
- **WHAT:** Sponsored by the National Engineering Safety Center, this year’s Thermal and Fluids Analysis Workshop (TFAWS) will focus on the innovation of new technologies in the disciplines of Thermal and Fluids Analysis through cooperative efforts. The three technical areas of focus are Aerothermal, Passive Thermal Control, and Fluids/Active Thermal/Life Support. Members of government, industry, and academia will come together and participate in papers sessions, panels/short courses, software training, and vendor displays. Participants are encouraged to contribute their discipline expertise while integrating current or new technology ideas.
- **INFORMATION:** [http://tfaws.jsc.nasa.gov/](http://tfaws.jsc.nasa.gov/)

10th International Business & Technology Summit

- **WHEN:** Aug. 18-19
- **WHERE:** Natick, Mass.
- **WHAT:** The International Business & Technology Summit will be followed by a one-day course titled “Cooling Electronics without All that Hot Air,” delivered by Tony Kordyban. This year’s summit will cover a wide range of critical thermal management issues using hour-long lectures given by well-known and knowledgeable speakers. There will also be technical short presentations by suppliers of thermal management solutions. The topics covered in this year’s summit include: advanced cooling technologies, liquid cooling, cooling power electronics, thermal management of RF and microwave devices, thermal challenges in 3D packages, military and avionic thermal management, cooling of compact and consumer electronic systems and thermal issues and the component level.
- **INFORMATION:** [www.coolingzone.com/summit2010/](http://www.coolingzone.com/summit2010/)

25th European Photovoltaic Solar Energy Conference and Exhibition (25th EU PVSEC) / 5th World Conference on Photovoltaic Energy Conversion (WCPEC-5)

- **WHEN:** Sept. 6-10
- **WHERE:** Feria Valencia, Valencia, Spain
- **WHAT:** This World Conference on Photovoltaic Energy Conversion will bring together the three most important global scientific and strategic PV Conferences: the 25th European Photovoltaic Solar Energy Conference and Exhibition, the 36th US IEEE Photovoltaic Specialists Conference and the 20th Asia/Pacific PV Science and Engineering Conference. This PV solar gathering will constitute the world’s leading science-to-science, business-to-business and science-to-industry forum for the global PV Solar sector.
- **INFORMATION:** [www.photovoltaic-conference.com/](http://www.photovoltaic-conference.com/)

16th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)

- **WHEN:** Oct. 6-8
- **WHERE:** Novotel Barcelona City, Barcelona, Spain
- **WHAT:** THERMINIC Workshops are a series of events to discuss the essential thermal questions of microelectronic microstructures and electronic parts in general. This year the workshop will address in addition to the “traditional” thermal management problems, also stress and thermal-stress-related-reliability issues, both in micro- and optoelectronics fields. These issues, including various nanotechnology applications, are of significant importance and of high interest to the engineering community engaged in the field of thermal phenomena in “high-tech” systems.
- **INFORMATION:** [http://cmp.imag.fr/conferences/therminic/therminic2010/](http://cmp.imag.fr/conferences/therminic/therminic2010/)
**Thermal Management and Technology Symposium**

- **WHEN:** Oct. 19-20
- **WHERE:** Gaylord Texan, Dallas, Texas
- **WHAT:** Thermal Management and Technology Symposium highlights the latest advancements in thermal technology for product design, system development and process management. This event will feature presentations on the latest advancements in thermal management and thermal technology for electronics packaging and cooling, thermal process control, temperature sensing and control, thermal materials, systems design and management for optimizing thermal properties.
- **INFORMATION:** [www.thermalnews.com/conf_10/TN10_index.php](http://www.thermalnews.com/conf_10/TN10_index.php)

**11th Annual LEDs 2010**

- **WHEN:** Oct. 25-27
- **WHERE:** San Diego Convention Center & Hotel Solamar
- **WHAT:** For a decade, IntertechPira’s LEDs conference has been a meeting place for industry veterans and newcomers interested in getting into the industry. The 11th annual LEDs 2010 will include afternoon tracks focusing in depth on technology topics, speakers and panels representing the whole supply chain; timely technical content from nuts-and-bolts, of the LEDs themselves to application level talks, industrial trends and new product updates.
- **INFORMATION:** [http://www.ledsconference.com/Home.aspx](http://www.ledsconference.com/Home.aspx)

**2010 Materials Research Society (MRS) Fall Meeting**

**MRS Symposium: Magneto Calorics and Magnetic Cooling**

- **WHEN:** Nov. 29–Dec. 3
- **WHERE:** Boston, Mass.
- **WHAT:** Consisting of topical symposia, the MRS meeting offers materials researchers the opportunity to present their work, get information on up-to-the minute developments in their field, and network. In addition, the Materials Research Society has established the MRS Workshop Series, which offers highly focused and compelling subjects, designed to allow full attention to one topic over a two to three day period. Workshops generally allow for greater interaction between speakers and audience than is typical in a meeting symposium.
- **INFORMATION:** [www.mrs.org/meetings](http://www.mrs.org/meetings)

**PowerMEMS 2010**

The 10th International Workshop on Micro and Nanotechnology for Power Generation and Energy Conversion Applications

- **WHEN:** Nov. 30–Dec. 3
- **WHERE:** Leuven, Belgium
- **WHAT:** Technical topics of interest include, energy harvesting for remote sensors and Microsystems; thermoelectric and photovoltaic materials and systems; piezoelectric, electrostatic and electromagnetic conversion; energy management and microsystem integration; nanostructured materials for energy and thermal management; micro fuel cells and micro reactors for fuel processing; micro/nano catalysis, combustion, heat and mass transfer; micro thrusters and miniature propulsion Microsystems; biologically inspired energy conversion and cooling; micro heat engines for power generation and propulsion; and micro and nanofabrication for energy applications.
- **INFORMATION:** [www.powermems.org/](http://www.powermems.org/)

**Third International Conference on Thermal Issues in Emerging Technologies**

**Theory and Application - ThETA 3**

- **WHEN:** Dec. 19-22
- **WHERE:** Sofitel El Gaziarah, Cairo, Egypt
- **WHAT:** Emerging technologies in various domains, including Microelectronics, Nanotechnology, Smart Materials, Micro-Electro-Mechanical Systems, Biomedical Engineering, and New Energies, all raise issues related to thermal effects and interactions. Their importance is continuously increasing, tending to be a dominant factor in new technologies. Topics will include micro and nanoscale heat transfer, microfluidics, thermal modeling of electronic systems, temperature aware computer systems design, cooling of electronic systems and data centers, compact thermal models, thermo-mechanical effects, new and renewable energies, and more.
- **INFORMATION:** [www.thetaconf.org/index.htm](http://www.thetaconf.org/index.htm)
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